BIASING PWM SYSTEMS

Biasing PWM Systems

- Needed if:
  - 0 to 100V input, ±symmetric output
  - Bipolar input, half bridge amplifier
  - Single supply systems
- Reference Voltage
  - Common Mode Voltage limits
  - Allows ±swing of diff. amp relative to V_{REF}

When input, output and feedback voltages are all symmetric bipolar signals with respect to ground, no biasing is required.

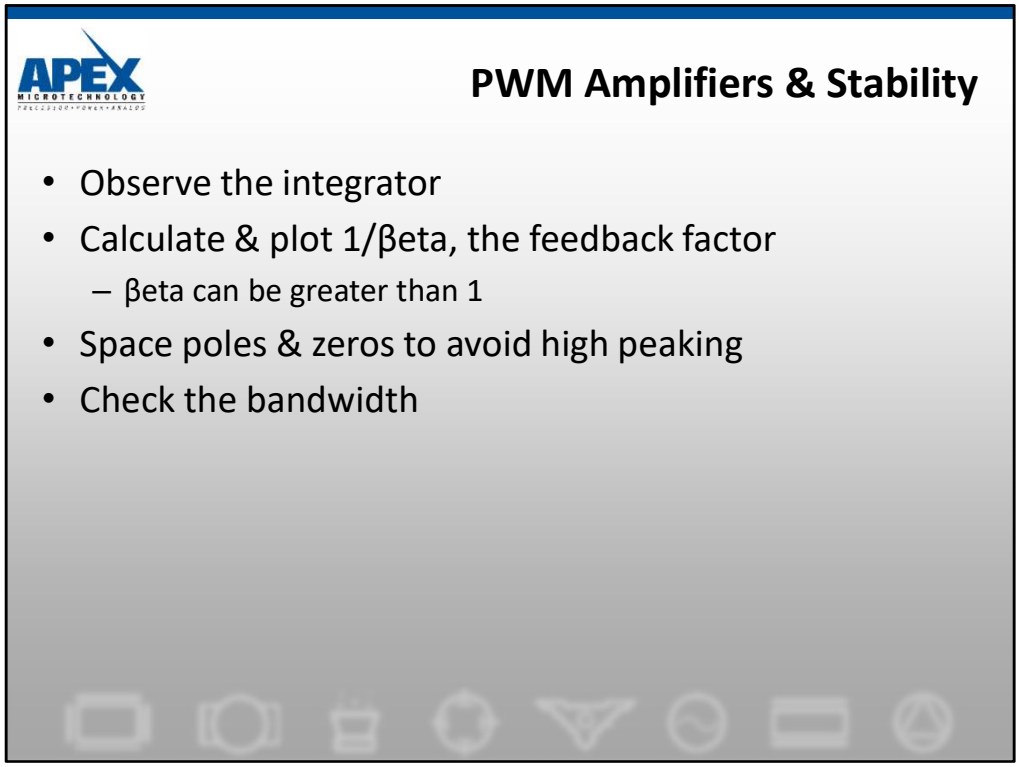
More frequently, one of the items in this slide will be the case and biasing (offsetting or level shifting) will be required. The key to setting up biasing is to remember the integrator slides where a stable operating point is achieved when all currents to the summing junction total zero.

Biasing PWM Systems

- Assume output where R_F current = 0
- Use transfer function to find V_{IN} & current
- If input current ≠ 0,
  - Pick a reference voltage
  - Calculate Rbias for equal and opposite current

In the case of full bridges, current in the feedback resistor is usually zero when the bridge output is zero. The transfer function is simply the relationship from input voltage to bridge output voltage.

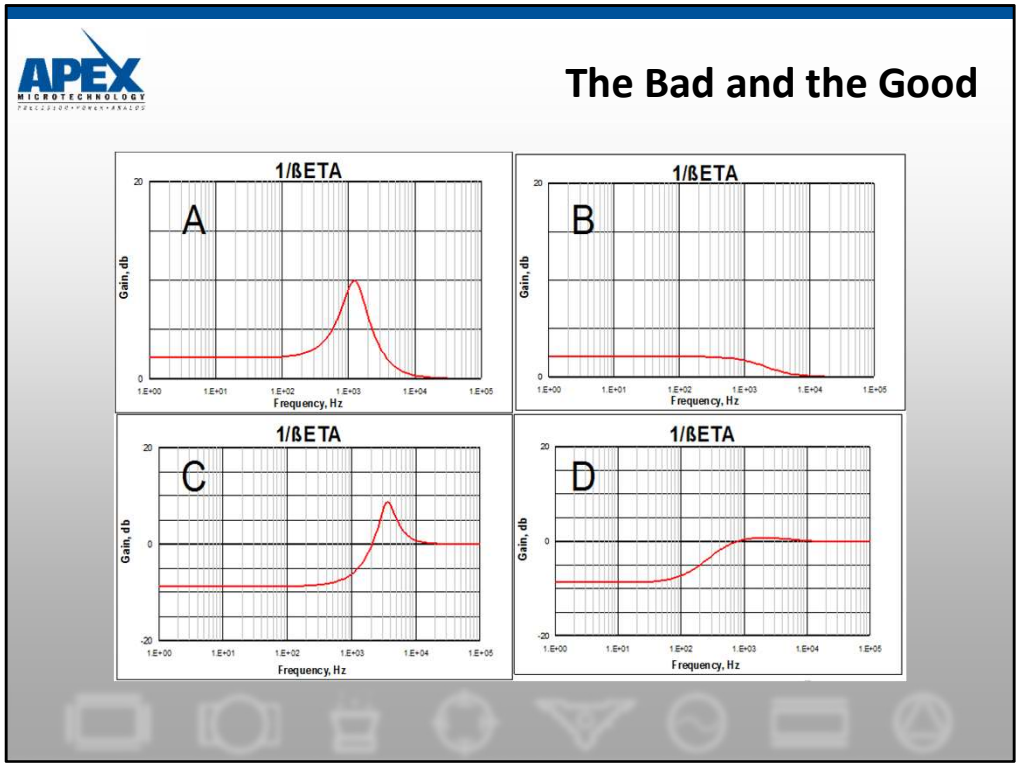
When feedback current is zero, the reference voltage and bias resistor need to feed the summing junction a current equal but opposite the current fed by the input signal and input resistor.



Linear design experience has taught many of us that as the number of stages or gain blocks in a loop increases, the probability of encountering a stability problem also increases. In a PWM system we typically have an integrator, the PWM power delivery block, a low pass feedback filter and often a feedback amplifier. This all implies that we need a technique to achieve a good design.

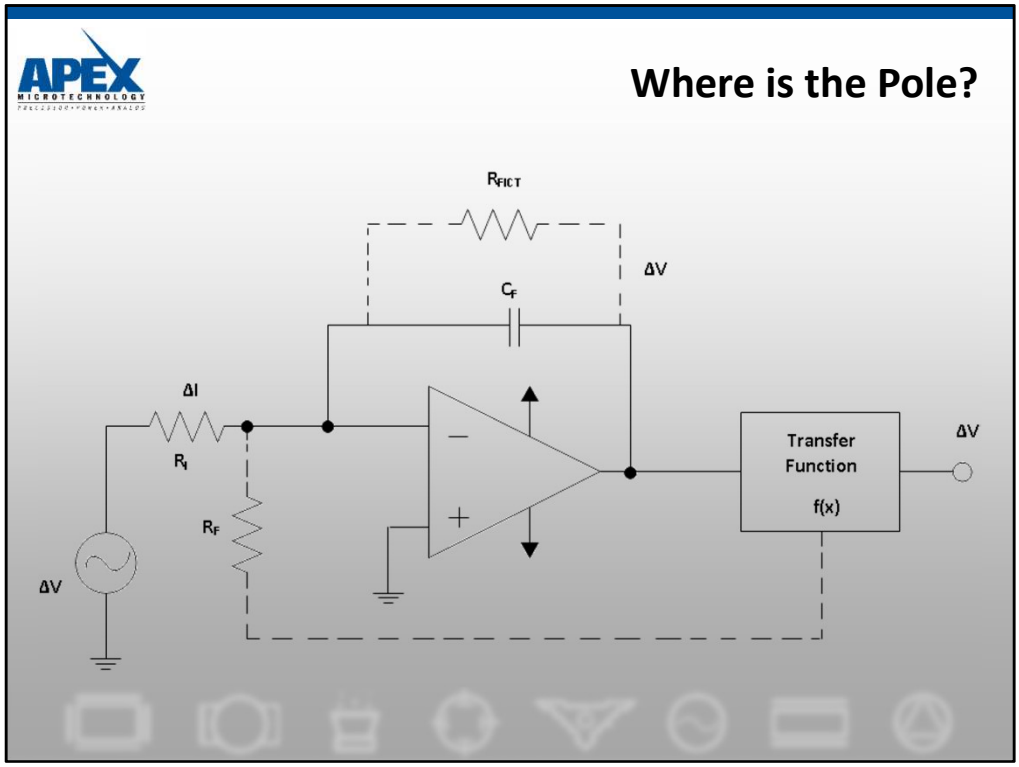
Our technique will be to calculate and plot 1/ßeta over frequency, and then minimize peaking. Assign an amplitude of one to the integrator output. Use the PWM transfer function to calculate the theoretical PWM output – ignore the fact that these are switching waveforms. Calculate around the feedback loop to the input of the integrator to find ßeta, the fraction of the output fed back. If there is a feedback path to the positive input, subtract this from the negative side feedback to find total feedback. Because there are gain stages in the feedback loop, it is possible to have a ßeta greater than one!

The major factor producing peaking is placement of the integrator pole too close to the poles in the feedback path. The integrator pole must be the dominant pole in the system. Setting the integrator pole frequency at 40% of the feedback pole frequency will provide good phase margins in low voltage circuits. With high voltage circuits, this percentage must decrease further.



Plots A and B examples of both peaking and non-peaking performance. Plot A resembles an op amp circuit with problems; low frequency 1/ßeta is positive, the peak spells trouble, and 0dB is approached at high frequency. Plot B is more what we want to see to insure stability; if bandwidth is not a concern, no peaking is desirable. When speed is a significant concern, some peaking will help, but at the expense of phase margin. For this case, peaking is defined as rise above the low frequency value.

Plots C and D are again bad and good, but for the case where low frequency 1/ßeta is negative. This will occur more often with the higher voltage amplifiers and it will be more difficult to eliminate all peaking without a severe penalty in bandwidth. The rise from the initial negative value to 0dB at high frequency is not part of the peaking we are looking for. For this case peaking is defined as only the rise above 0dB.

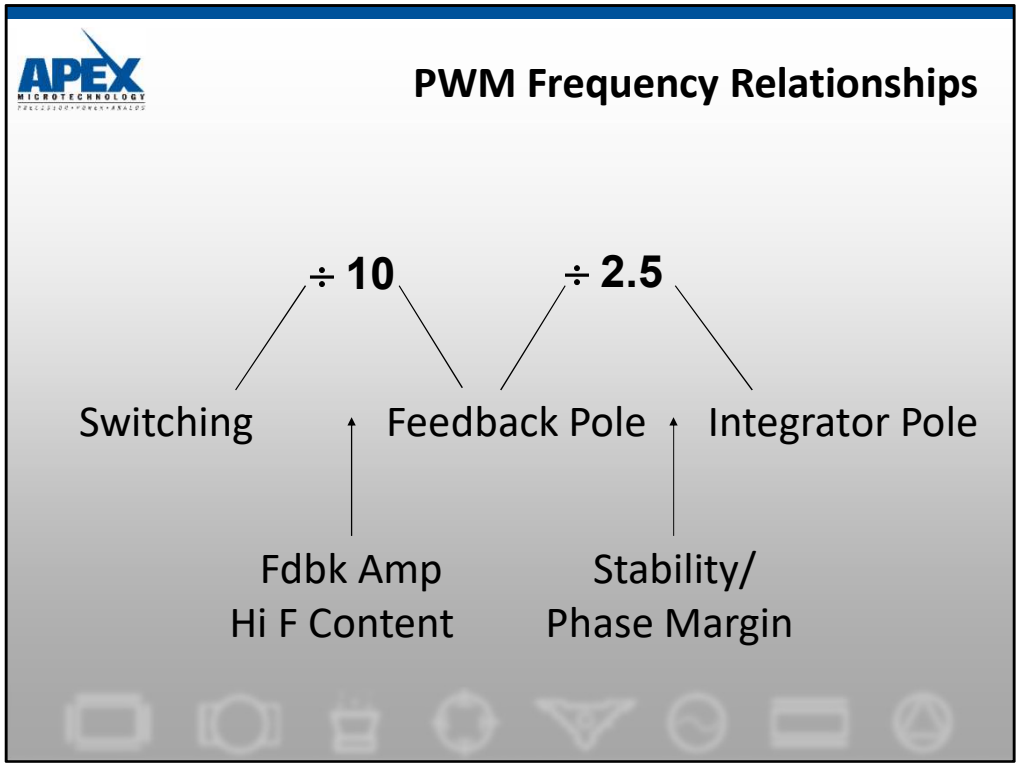


So, just where is the pole created by the integrator capacitor? As there is no resistor directly in parallel with this capacitor, the traditional calculation for an op amp roll off capacitor will not work. However, if such a resistor were in place (rather than our complex feedback loop), what would its value be? This fictitious value would result in the same change of integrator output voltage for a given change of input voltage, as occurs in the real system. To rephrase, if we know Δinput current to the integrator, Δoutput voltage of the integrator, then Ohms law dictates the effective feedback resistance must be ΔVOUT/ΔI IN. To answer these questions we need to know the input signal, the input resistor and how much the output of the integrator will move in response to the input signal.

To find this fictitious feedback resistor, assume a convenient input and use the given overall transfer function to find the PWM output voltage. Now divide by PWM gain to find movement of the integrator voltage.

$$R_{FICTITIOUS} = R_{IN} * \Delta integrator / \Delta input \quad (2)$$

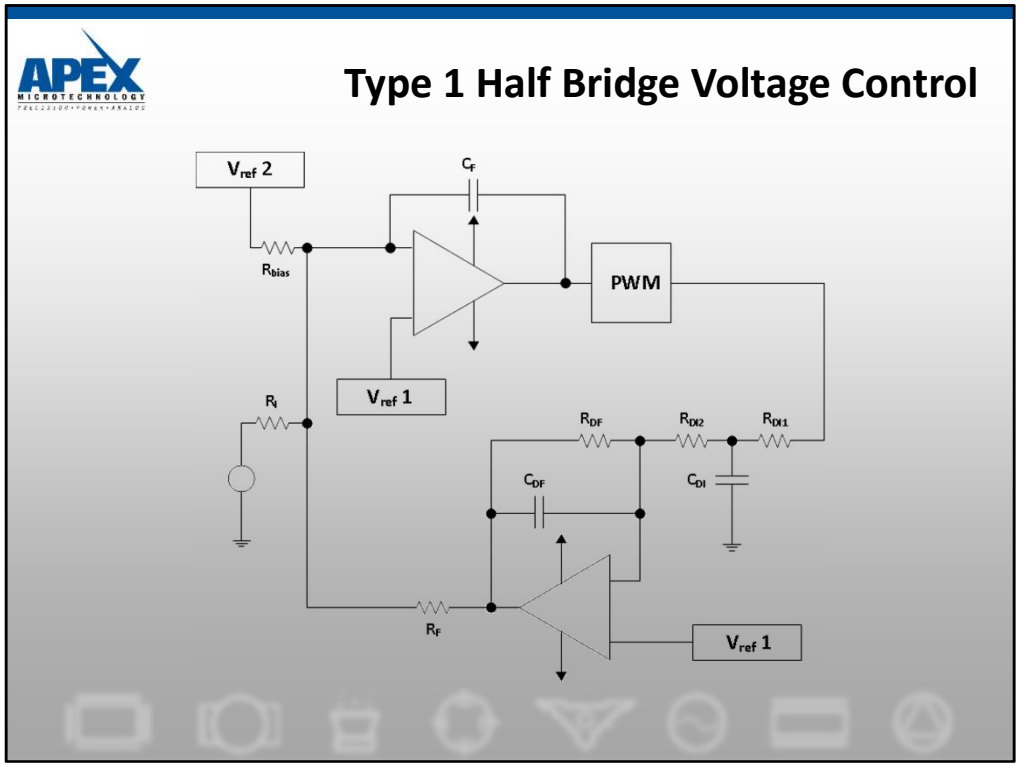
Using this fictitious feedback resistor, the pole frequency can be calculated just as if it were an op amp with parallel R-C feedback. When powering the SA01 (full bridge and 5V p-p ramp) on 75V, gain of the PWM block is 30. If the circuit is configured for a gain of 10 (say, ±5Vin, ±50Vout) and the input resistor is 5K, Δout =100, Δintegrator = 3.333, Δinput = 2, and the fictitious resistor is 1.67K. Even though the real RF may be 5KΩ, a 0.1µF capacitor produces a pole at 953Hz.



A reasonable starting place is to allow at least a decade between the switching frequency and the feedback pole frequency. This usually places the cutoff frequency of the power filter and the pole frequency of the feedback circuit at the same point.

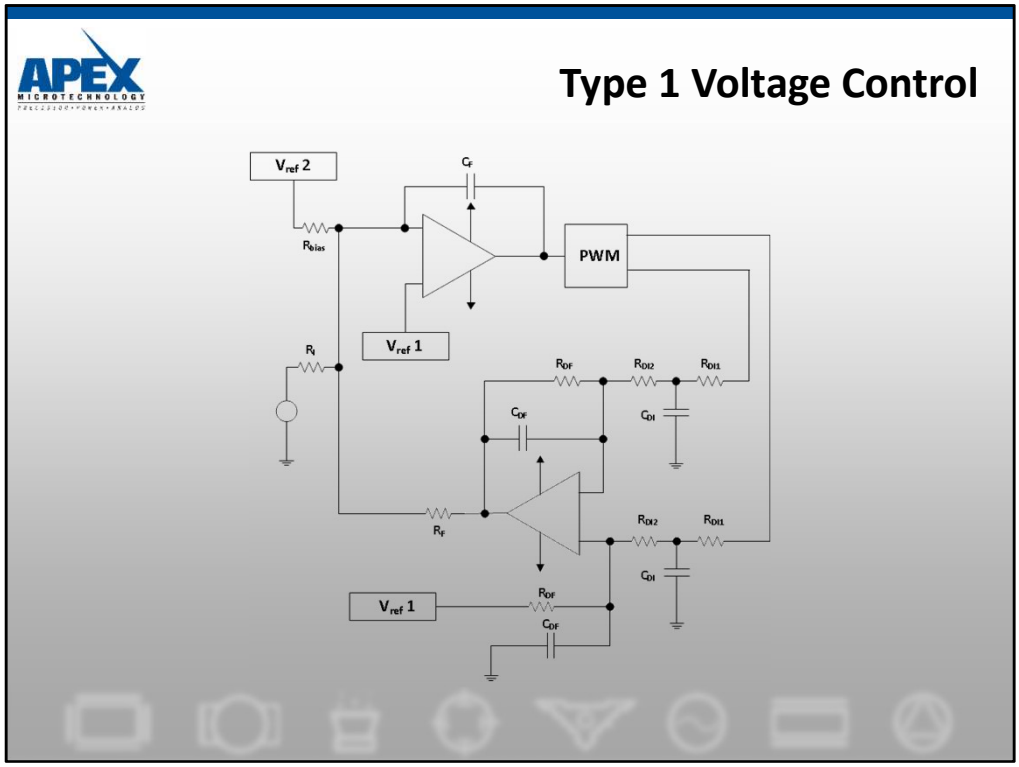
The low pass signal filter consists of one or more R-C pairs. If feedback is taken directly at the PWM output (by far the most common method), this filter sees a square wave input with peak-to-peak amplitude nearly equal to Vs. If feedback is taken after the power filter, phase shift of the power filter is added to the loop response. For this reason, a power filter inside the loop will be low Q and low attenuation.

The integrator pole frequency will be a fraction of feedback pole(s), the higher the supply voltage, the smaller the fraction that should be used.



Presently, Apex does not carry any more half-bridge PWM amplifiers in its products offerings; however, the slide is kept for explanatory purposes only

The voltage references shown are usually required when operating on single supplies, and may be required even when using dual supplies. Vref1 provides common mode headroom for single supply circuits and Vref2 handles biasing or level shift duties.



The Type 1 full bridge circuit requires a differential amplifier in the feedback path. Side-to-side component matching for the difference amplifier is VERY important. The impedance of Vref1 needs to be at least two orders of magnitude less than Rdf, AND needs to handle current in both directions. Vref2 may be positive or negative.

Even with the poles of the difference amplifier, it will be subjected to AC voltage at the switching frequency. These high frequency signals should be rejected, and even more importantly, they should not be allowed to create errors which look like voltage offset. Therefore, this op amp needs good high frequency common mode rejection. The LF353 data sheet indicates 80dB rejection at 100KHz, making it a good choice.

Gain of the difference amplifier is almost always less than unity. Swing capability, common mode range and PWM supply voltage place limitations on the maximum gain.

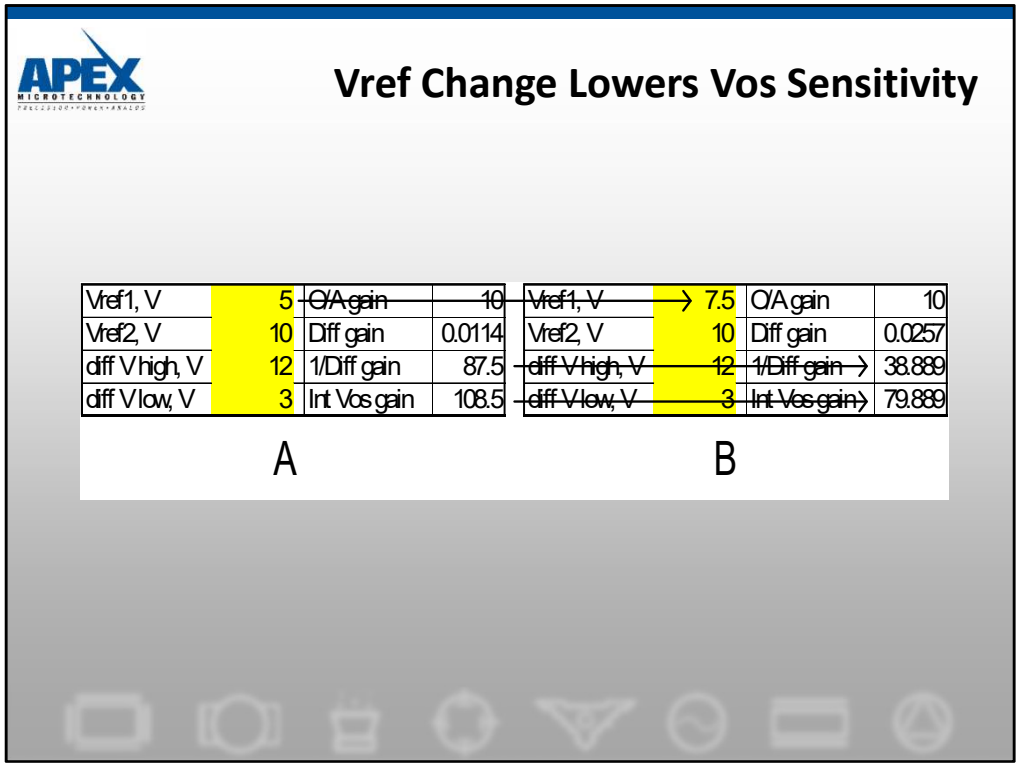
General Operating Levels #1

Desired Values:		Operating points:		Ideal operating:	
Zload	10	Vramp p-p	4	Rdi total KΩ	125
Vout high, V	110	Vin ma p-p	2	PWM gain	43.75
Vout low, V	10				
Vin high, V	10			Actual operating:	
Vin low, V	0			Eff PWM gain	43.061
		Vref1, V	10	O/A gain	10
Vs, V	175	Vref2, V	5	Diff gain	0.04
Ri KΩ	5	diff V high, V	12	1/Diff gain	25
Rdf KΩ	5	diff V low, V	3	Int Vos gain	15
Diff poles KHz	2	Suggestions		diff CMV hi, V	10
Int pole KHz	0.4	0.8		diff CMV lo, V	10
				diff out hi, V	10.4
	Actual	Suggestions		diff out lo, V	3.4
Rbias KΩ	-2.5	-2.5		Rdi leg mA	1.2692
Rf KΩ	2	2		Rdi1 watts	0.6738
Rdi2 KΩ	113.64	113.6363636		Rdi2 watts	0.1831
Rdi1 KΩ	11.364	11.36363636		Eff Rf	1.1429
Cdi nF	7.0028	7.002817496		Diff pole i KHz	2
Cdf nF	15.915	15.91549431		Diff pole f KHz	2
Cf nF	348.15	348.151438		Int pole KHz	0.4
Phase margin °	38.162			Vout hi, V	110
Peaking, dB	2.3068	F @ peak Hz	865.964	Vout lo, V	10

Here's the given data for this example: SA14 half bridge operating on 160 to 175VDC; Switching frequency = 22.5KHz ; VRAMPp-p = 4V; Vcc = 15V; Input signal = 0 to 10V; System does not have a negative supply; Output = 10 to 110V, up to 10Hz
***SA14 is not available, but slide is kept for example purposes**

The topology is Type 1 half bridge and initial data entry into Power Design is shown. The op amp is LF353. That data sheet indicates worst case common mode voltage range of 4V from the rails and minimum output swing of 3V from the rails for a 10KΩ load. The 3V restriction was entered as diff amp high and low limits because common mode voltage for a half bridge will be VREF1. Knowing voltage references for 15V supplies are readily available with 10V outputs and that setting VREF1 close to the upper diff amp voltage limit maximizes its swing capability, 10V was entered for VREF1. It was assumed a lower VREF2 could be easily generated. The 5KΩ values for Ri and Rdf seemed a good starting point. Diff amp poles are often placed a decade below FSW, but in this case they are half that because we have no bandwidth problem and lower pole frequencies mean less high frequency energy fed to the diff amp. The integrator was also set in a conservative manner. The Load Green Suggestions button was used.

Right away, we have a warning in the form of a negative value bias resistor (red). If you keep these in stock, skip to the next slide. The rest of us will make a note to switch our reference voltages. To the right, we find our smaller diff amp input resistor getting a little warm. Simply changing the diff amp feedback resistor can scale these input resistors. Increasing these resistors will also decrease the two diff amp capacitors.



In section A, we find that the switched voltage references will work (after loading green suggestions), but because the resulting diff amp swing is considerably smaller than the available range, our DC error budget is being inflated. Output error due to the voltage offset contribution of each op amp can be calculated with the gain values in the two lower right cells. By changing VREF1 to 7.5V (and loading green suggestions), we reduce the effect of integrator offset about 25% and the effect of the diff amp offset is lowered better than 2:1. There's nothing unique to PWMs here, just DC op amp circuit solutions.

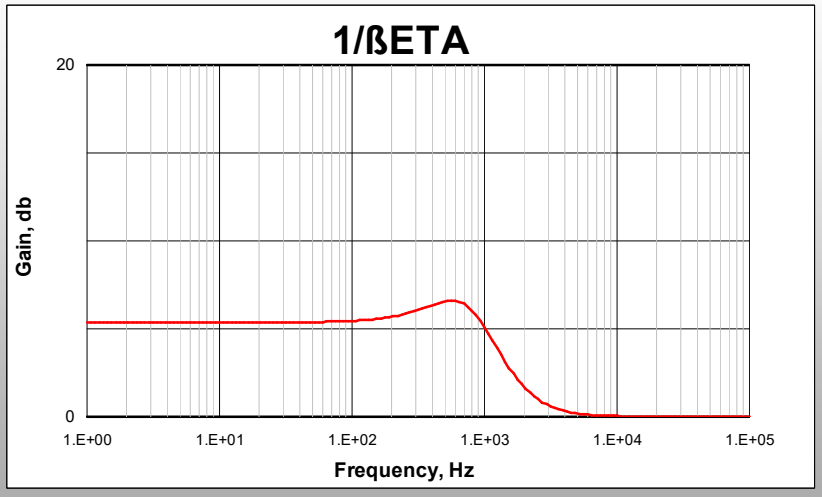
Be aware that while not shown here, all the suggested resistor and capacitor values change when the reference voltages changed.

Standard Values Finalize Design

Desired Values:			Operating points:			Ideal operating:	
Zload	10		Vramp p-p	4		Rdi total KΩ	396.67
Vout high, V	110		Vin ma p-p	0.66667		PWM gain	43.75
Vout low, V	10						
Vin high, V	10					Actual operating:	
Vin low, V	0					Eff PWM gain	43.061
			Vref1, V	7.5		O/A gain	9.938
Vs, V	175		Vref2, V	10		Diff gain	0.0257
Ri KΩ	15		diff V high, V	12		1/Diff gain	38.922
Rdf KΩ	10.2		diff V low, V	3		Int Vos gain	79.851
Diff poles KHz	2		Suggestions			diff CMV hi, V	7.5
Int pole KHz	0.4		0.8			diff CMV lo, V	7.5
						diff out hi, V	7.6927
	Actual		Suggestions			diff out lo, V	3.1965
Rbias KΩ	4.81		4.838709677			Rdi leg mA	0.4113
Rf KΩ	3.83		3.857142857			Rdi1 watts	0.2127
Rdi2 KΩ	361		360.6060606			Rdi2 watts	0.0611
Rdi1 KΩ	36		36.06060606			Eff Rf	3.4073
Cdi nF	2.2		2.210485321			Diff pole i KHz	2.0095
Cdf nF	10		7.801712897			Diff pole f KHz	1.5603
Cf nF	100		116.7747883			Int pole KHz	0.4671
Phase margin °	43.324					Vout hi, V	109.82
Peaking, dB	1.2463		F @ peak Hz	562.341		Vout lo, V	10.444

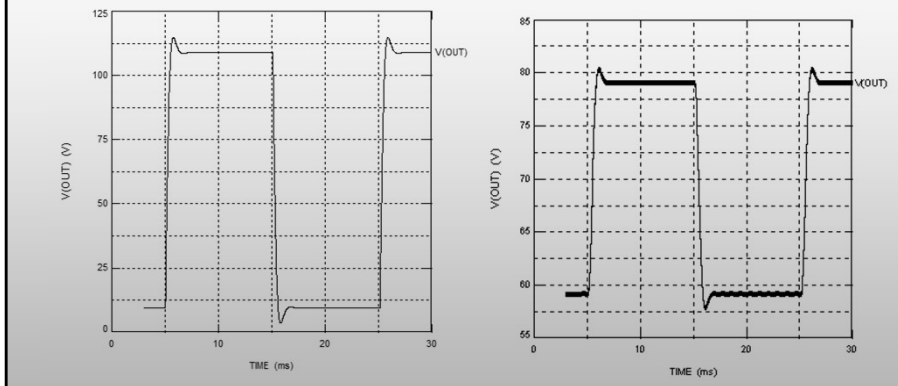
Here are the results of the other changes and working with standard value charts a little. There are many component combinations that could yield DC output accuracy within a few percent and provide adequate phase margin. This design will take advantage of the fact that the smaller diff amp input resistor can be a 5%, ½W type and still only affect gain by about 0.5%. Offset adjustment could be accomplished by varying either reference voltage or by adjusting the bias resistor. It is also possible to include a gain adjustment with the input resistor, the main feedback resistor, the diff amp feed back resistor, or its input resistors. Note that when using a full bridge amplifier, the feedback amplifier is fully differential and gain adjustment is practical in this stage only with difference amplifier circuits having a dedicated single resistor gain adjustment.

Standard Values Finalize Design

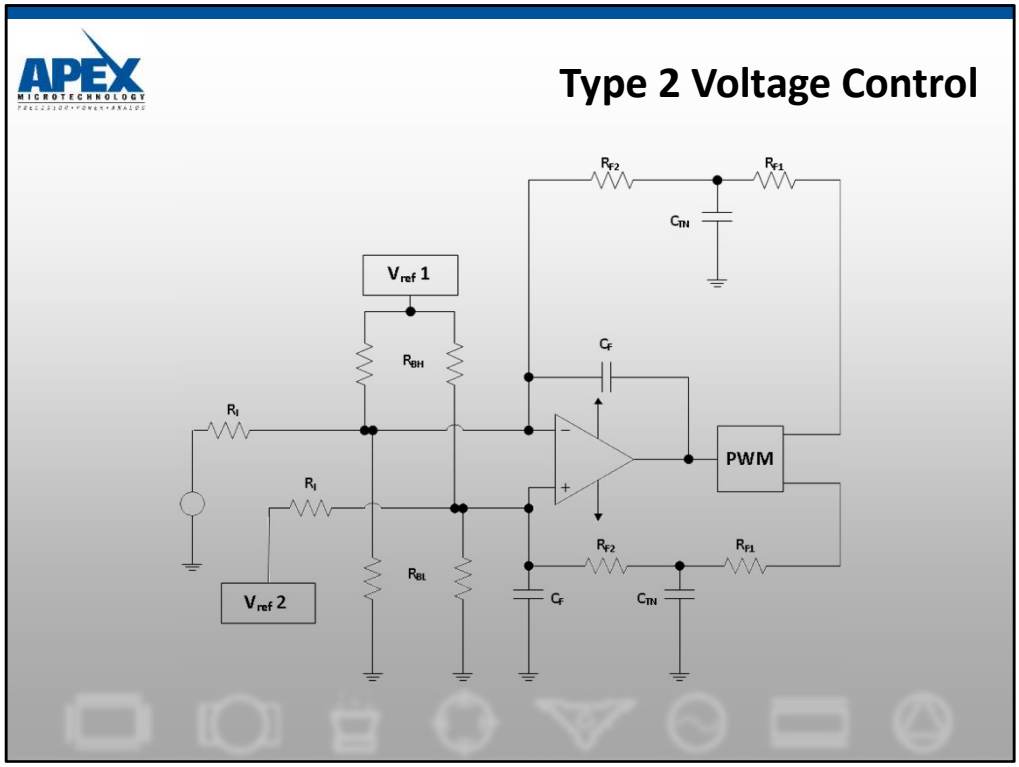


Our circuit is quite well behaved. The 1.25dB peaking corresponds to about 43° phase margin.

Standard Values Finalize Design

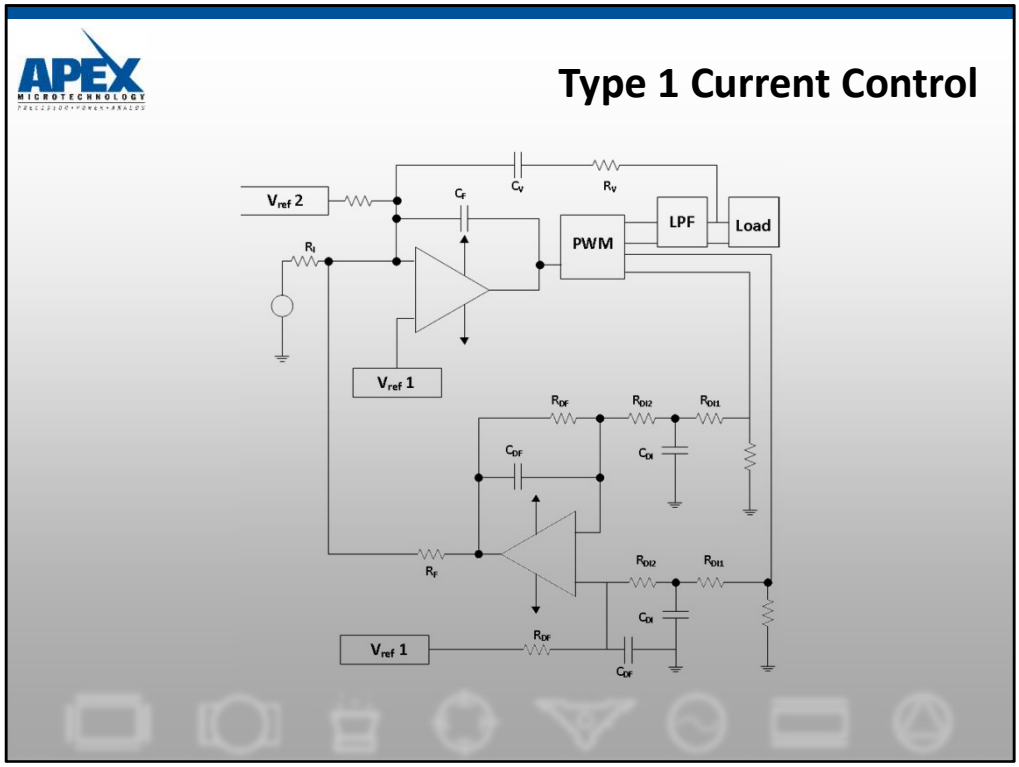


Both of these Spice model simulations agree with Power Design in predicting a stable circuit. On the left is the output of a state average Spice model simulation which took 8 seconds on a 759MHz PC. With this speed, it is painless to run a variety of component values. On the right we see output from pulse-by-pulse macro model requiring 45 minutes to run. Simulation times will vary substantially with machines, Spice platforms and run options. In any event, you will want to zero in closely on low frequency performance prior to attempting to examine switching performance.



The simple voltage control circuit is shown as inverting, but non-inverting or full differential operation is possible as long as common mode voltage for the op amp is analyzed. Just as in the four resistor op amp difference circuit, accuracy concerns demand that the resistors and capacitors on the two sides be matched.

Example 1 in AN41 covers this circuit in detail.



Schematically there are two differences between this current control circuit and the Type 1 voltage control circuit: The difference amplifier connects not to the outputs, but to the current sense pins of the PWM amplifier; and there is an additional voltage feedback path at the top of the schematic.

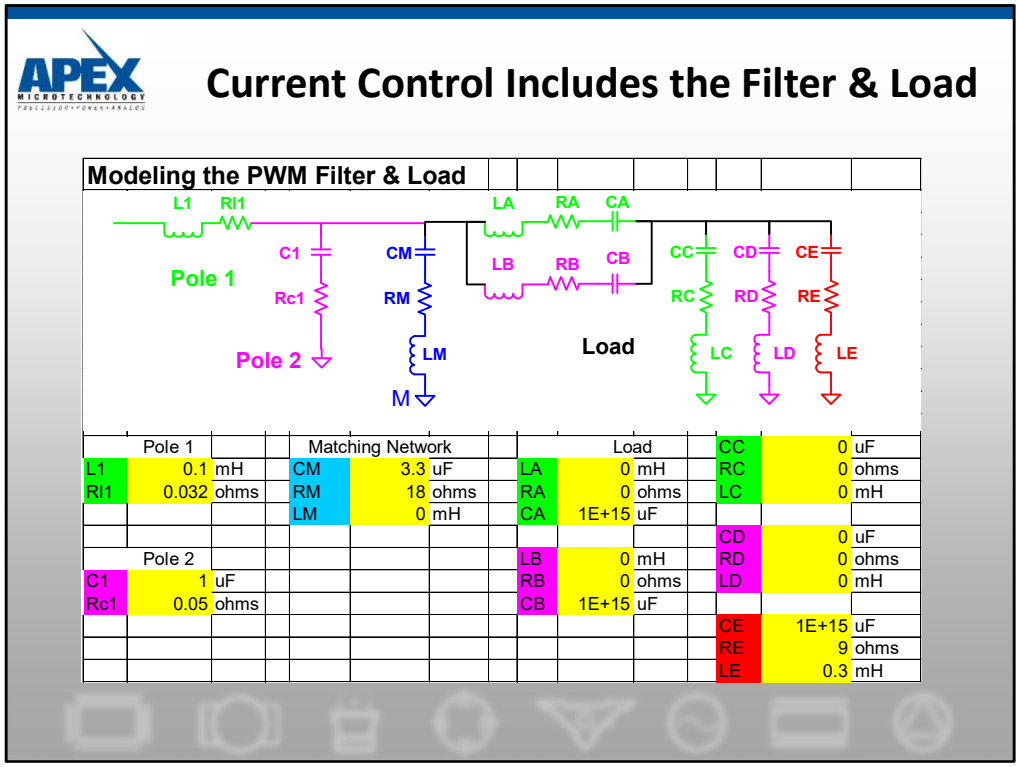
Operationally, the filter, the matching network and the load are INSIDE the feedback loop and therefore become a significant element of stability analysis. Matching networks are often set to a higher than textbook impedance values (or omitted) because their current is included as part of the controlled output, but this current is not delivered to the load. As the filter contributes negatively in the stability analysis, it is often far from the textbook filter (designed to only knock off sharp edges), and sometimes is omitted altogether, leaving the load to do all the filtering.

If the load contains moving parts, the mechanical factors need to be equated to electrical parameters prior to analyzing the system.

When given application requirements are only in terms of output current and load impedance, the first stop is usually the linear Power sheet, where these terms can be entered to easily find drive voltage requirements (output voltage will be correct no matter what supply voltage or amplifier is specified).

The next design step is usually the PWM Filters sheet where the matching network and filter are designed and then sent to the PWM Power sheet for check and modification.

Current Control Includes the Filter & Load

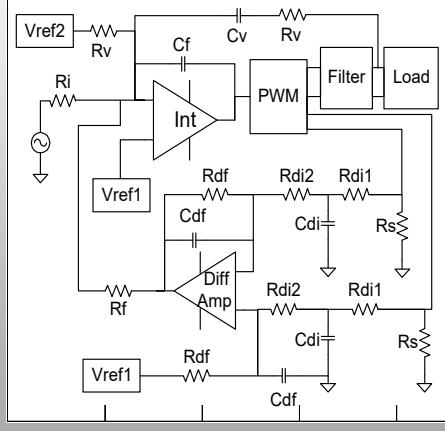


	Pole 1			Matching Network				Load			
L1	0.1	mH	CM	3.3	uF	LA	0	mH	CC	0	uF
RI1	0.032	ohms	RM	18	ohms	RA	0	ohms	RC	0	ohms
			LM	0	mH	CA	1E+15	uF	LC	0	mH
									CD	0	uF
	Pole 2					LB	0	mH	RD	0	ohms
C1	1	uF				RB	0	ohms	LD	0	mH
Rc1	0.05	ohms				CB	1E+15	uF			
									CE	1E+15	uF
									RE	9	ohms
									LE	0.3	mH

Here we see the filter/matching network/load definition area of the Power Design PWM Stability sheet. This is “must have” data for current control. You have the option of entering the data one element at a time, but the “Extract” command button grabs values from the PWM Power sheet- - If you used that for checking voltage mode peaking. If you started in the PWM Filters sheet, the load inductance will be in the lower right cell.

Setup for Sense Pin Control

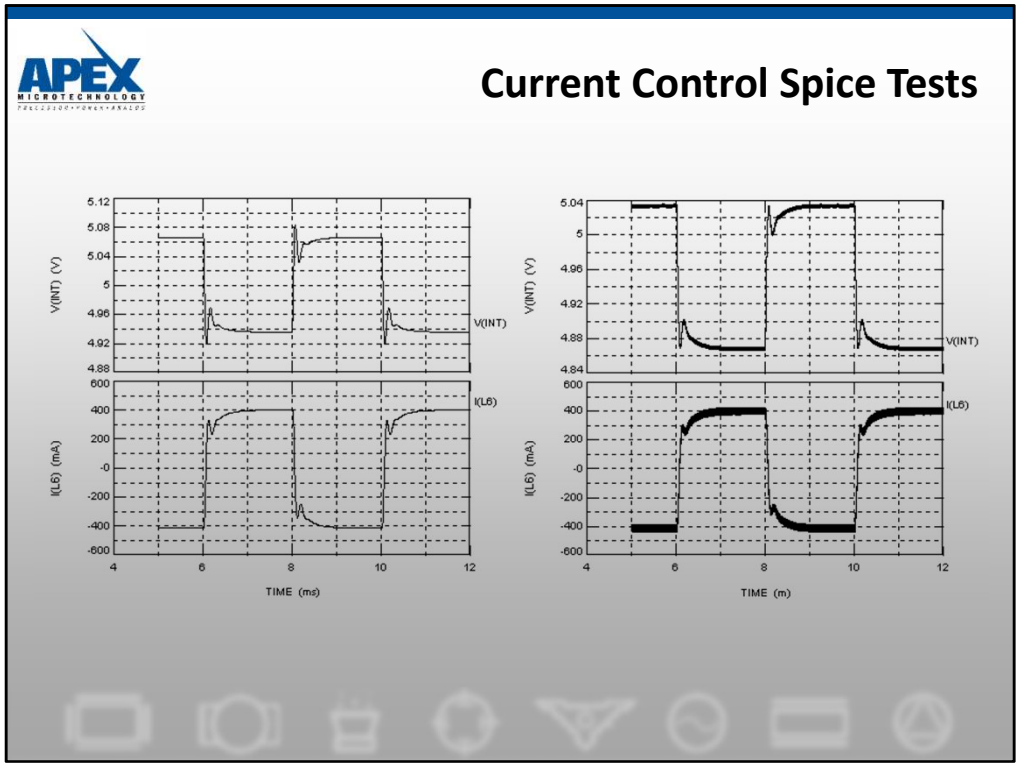
					Desired Values:		Operating points:	
Type I1	Readme	SA12			Iout high, A	10.2	Vramp p-p	4
					Iout low, A	-10.2	PWM gain	60
					Vin high, V	7.5		
					Vin low, V	2.5	Vref1, V	7.5
					Vs	120	Vref2, V	0
					Ri KΩ	1	diff V high, V	12
					Rs Ω	0.1	diff V low, V	3
					Rdf KΩ	10		
					Diff poles KHz	20	Suggestions	
					Int pole KHz	5	8	
						Actual		
					Rbias KΩ	9.3	-3	
					Rf KΩ	1	1.8	
					Rdi2 KΩ	3.3	3.709090909	
					Rdi1 KΩ	0.33	0.78	
					Cdi nF	100	24.11438532	
					Cdf nF	3.3	0.795774715	



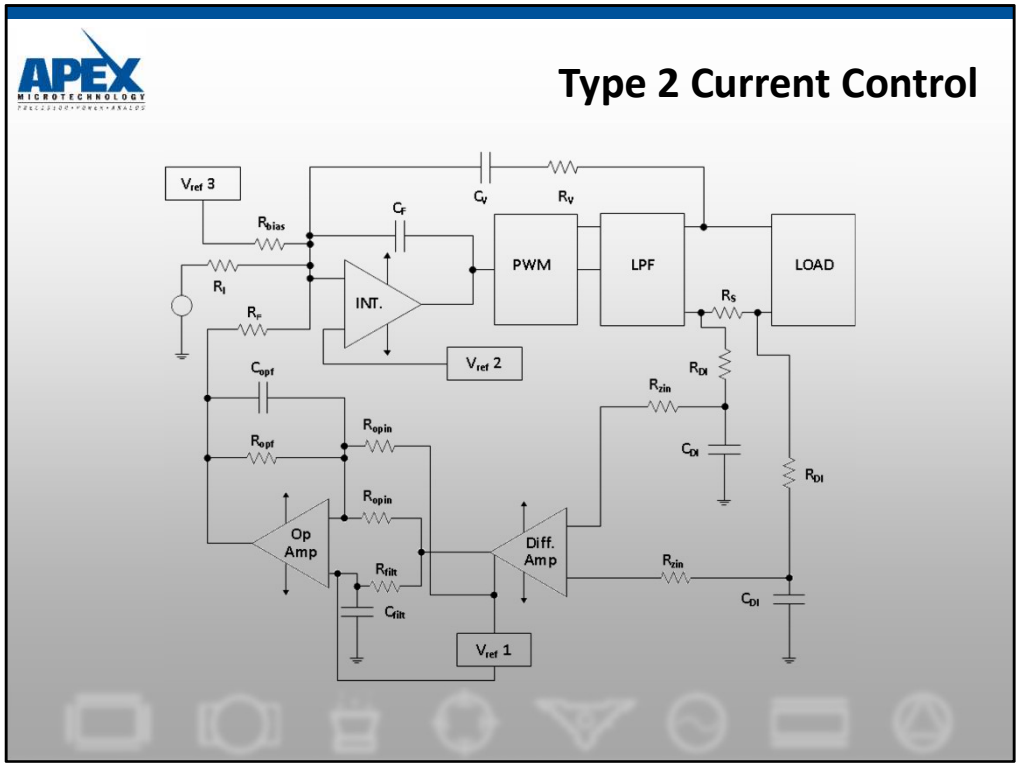
By now we know the outputs, inputs and the supply. Choose the input resistor high enough for the signal source to drive, and low enough to avoid parasitic problems- -1K to 10K is common. There are two lines of logic on selecting sense resistor values: a) develop 100mV on the Ilimit pin at maximum output current (the typical value used to activate current limit, or 2) develop 1V on the Isense pin at maximum output current (above 1V may affect control of the output switch). Option 2 results in better accuracy and wider bandwidth.

The acceptable range of values for the difference amplifier feedback resistor is wide. Lower values will require larger roll off capacitors, higher values call for smaller capacitors and can allow too much influence by parasitics. You be the judge how large to go with the capacitors, but let me suggest they never go below 100pF.

The ideal place for Vref1 is usually the center of the difference amplifier input and output limitations. If required, Vref2 should be several volts away from Vref1. If a negative value in red appears as a suggestion, switch Vref2 polarity with respect to Vref1.



Here are the state average and pulse-by-pulse spice runs on our example. If we were to lower impedances of Rv and Cv, the leading edges of the square wave will become more rounded. Increasing those impedances will sharpen up the leading edges, at the expense of phase margin.



If the PWM amplifier has only one sense pin or if current in the filter or match network are adversely affecting output accuracy, the Type 2 current control circuit may be best. Notice that phase shift introduced by the filter is now INSIDE the feedback loop. Filters in this configuration are usually of low order and often have a cutoff frequency at or even above the switching frequency (the load is doing most of the filtering).

The difference amplifier is often a gain of one, giving rise to the need of an op amp gain stage. This stage is not usually included if the difference amplifier can provide enough gain. When used, it may be inverting or non-inverting (diff amp inputs can easily be switched to provide correct phase feedback).

The rest of the circuit is similar to Type 1 and spreadsheet comments will guide you through the design process. Note that the input voltage to the difference amplifier will be as high as the supply voltage.

Current Out Stabilizing Steps

- Filter: no more than 10dB Vmode peaking
- Enter Filter/Load-except NO inductance
- Stabilize with up to 10dB peaking
  - Need high values for Cv & Rv
- Re-enter load inductance
- Selected Rv and Cv
- Check with Spice and the bench

Vmode peaking is in the PWM Power sheet.

Move to the PWM Stability sheet.

Stabilize with no inductance & no voltage feedback network.

Re-enter inductance & stabilize with the voltage feedback network.

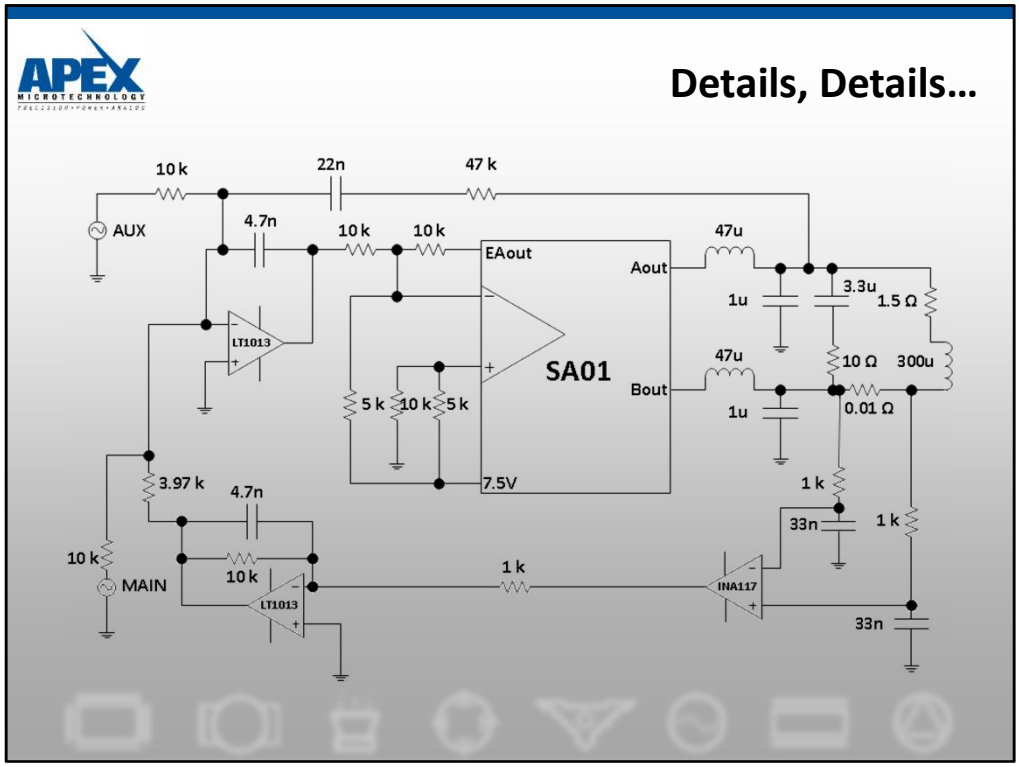
Check and revise as needed.

Diff Amp: Make or Buy?

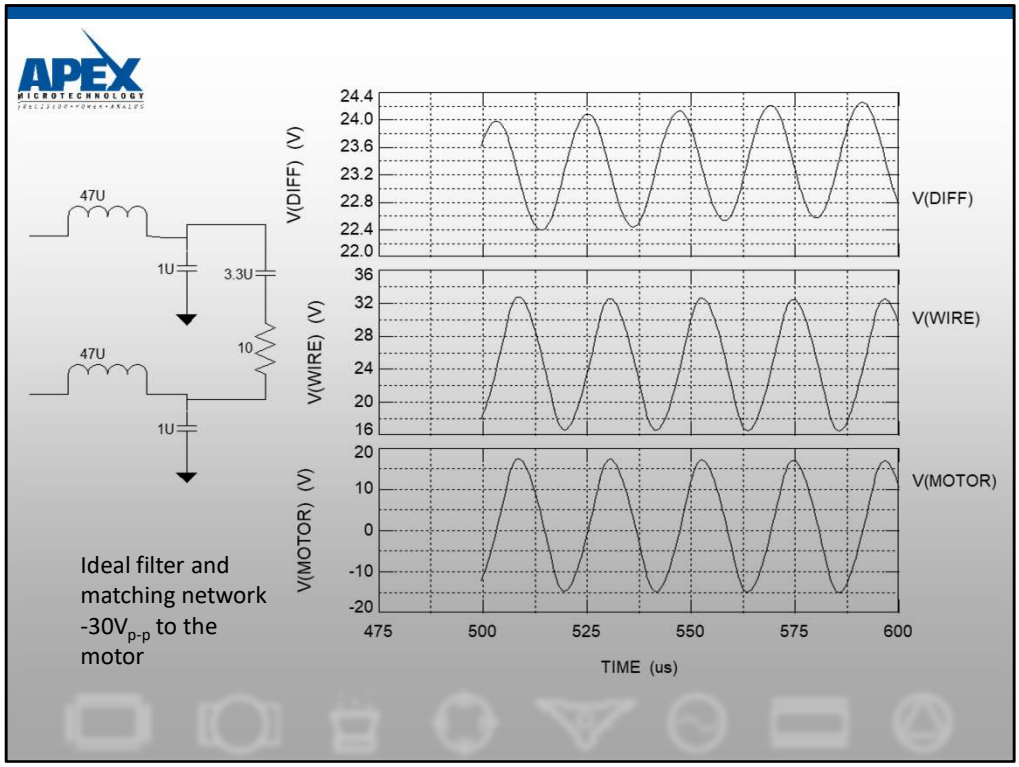
- Vdifferential = 1% of VS
- Vcommon mode = up to VS
  - Need to reject this common voltage
- 80dB; 1/10,000; 10mV per 100V
- If you make your own
  - Requires 0.01% side to side resistor ratio match

The required accuracy levels and circuit efficiency both play a role in this decision. Efficiency concerns ask for a sense resistor as small as possible- -meaning a small differential voltage. However, difference amplifier input errors (voltage offset and common mode rejection) must be small compared to the sense voltage to achieve high accuracy.

Here are a few numbers to illustrate the importance of common mode rejection. Assume Vs=100V, sense voltage=1V and CMRR=80dB. The actual common mode error at 100V swing is 10mV. This is a 1% error compared to the sense voltage. Resistor match required to achieve 80dB is 0.01%. These match requirements speak positively for the buy option for the diff amp.



This is an example from Application Note 41, where biasing and stability are covered. Four filter/match network options are covered, which all produce similar results with the square wave stability test. The next four slides are concerned with system RFI.



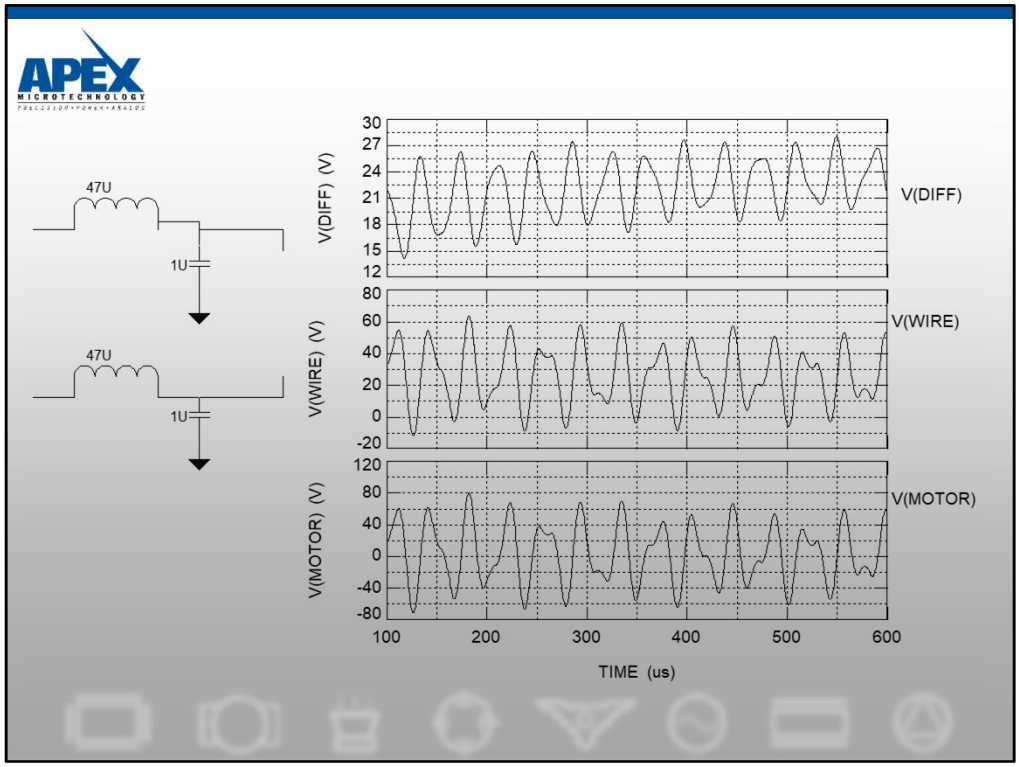
All the simulations are at zero drive current (50/50 modulation).

In this “best” design, all waveforms are basically a sine at the switching frequency of 42kHz.

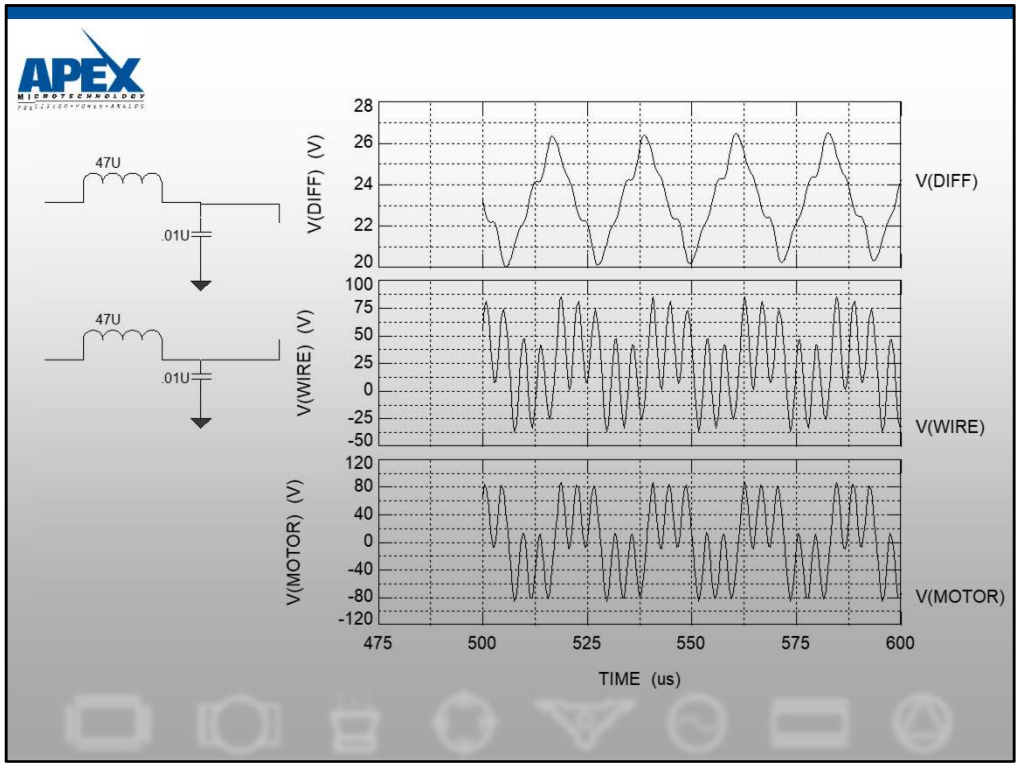
At the top is the common mode voltage applied to the diff amp input pins.

In the middle we see voltage with respect to ground on the wires connecting the amplifier to the motor; read this as transmission antenna.

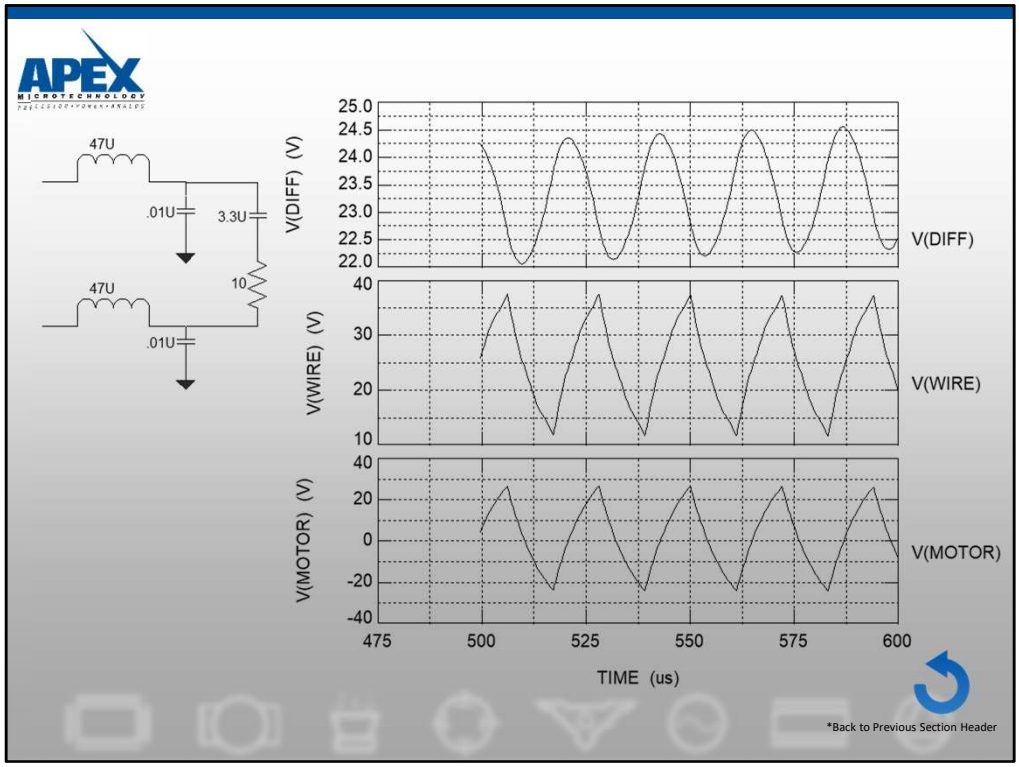
On the bottom is the voltage applied to the motor



In this option, the matching network was removed. Note the time scale has changed 4x. There is now major signal content at about 25kHz. While it is difficult to say what the RMS values are, a good guess is that they all increased a factor of 2.5. This might be a good time to check motor temperature.



The matching network is still gone, and the filter capacitors have been reduced significantly. Common mode voltage seen by the diff amp is mostly a triangle and peak amplitude is up by a factor of about four. Voltage on the transmission line and across the motor has gone up and now has a significant content at about 220kHz!



Using an undersized filter capacitor with the matching network results in wire and motor waveforms with higher than optimum amplitude and worse yet, they contain considerable high frequency energy (read this as a radiation problem).