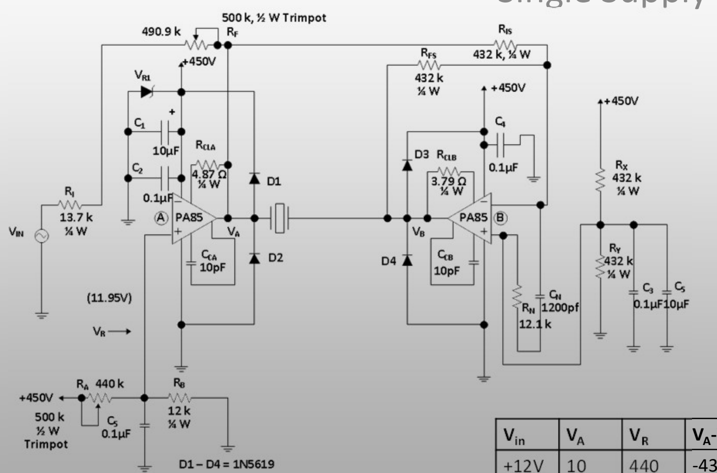
PIEZO DRIVE APPLICATIONS

860 Vpp Piezo Drive

Single Supply Bridge



V_{in}	V_A	V_R	V_A-V_R
+12V	10	440	-430
+6V	225	225	0
0V	440	10	+430

1. Vout = VA-VB

   Max Vout = Vs-V_{SATA} – V_{SATB}

2. Gain = $Vout_{p-p}$ /Vin_{p-p} = $(VA-VB)_{p-p}$/Vin_{p-p}

   $860V_{p-p}/12V_{p-p}$ = 71.67

   Gain = 2 RF/RI since we have a bridge configuration. That is the voltage gain across the load is twice that of the primary amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +225V.

   Therefore RF/RI = 71.67/2 = 35.833

3. Offset:

   $$VA-VB = Vs\,(2(1+RF/RI)(\frac{RB}{RA+RB})-1) - 2\,(RF/RI)\,Vin$$

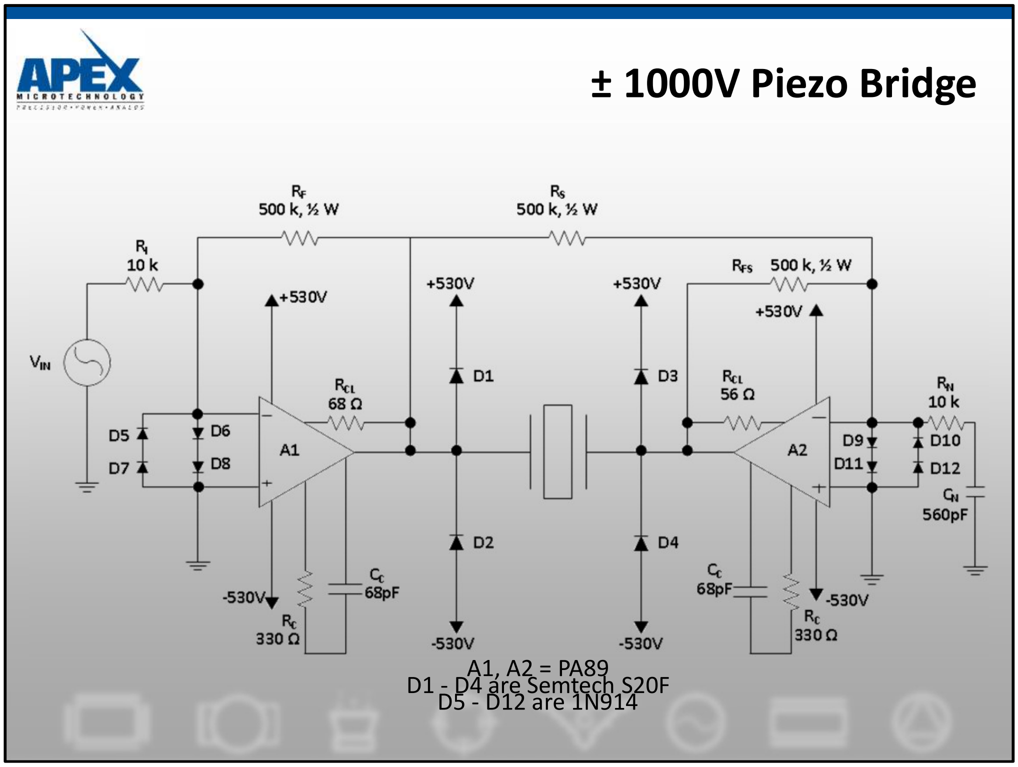
   When Vin= 0 then VA-VB = +430V

   Using RF/RI = 35.833 and solving above yields RA = 36.669RB

   Choosing RB = 12K implies RA = 440K

4. Check for commong mode voltage compliance: 11.95 V > 10V; OK.

Ref. AN25



Piezo users appear to never have enough voltage. As soon as it was introduced the PA89 found its way into bridge circuits to drive piezos at +/1100V and beyond.

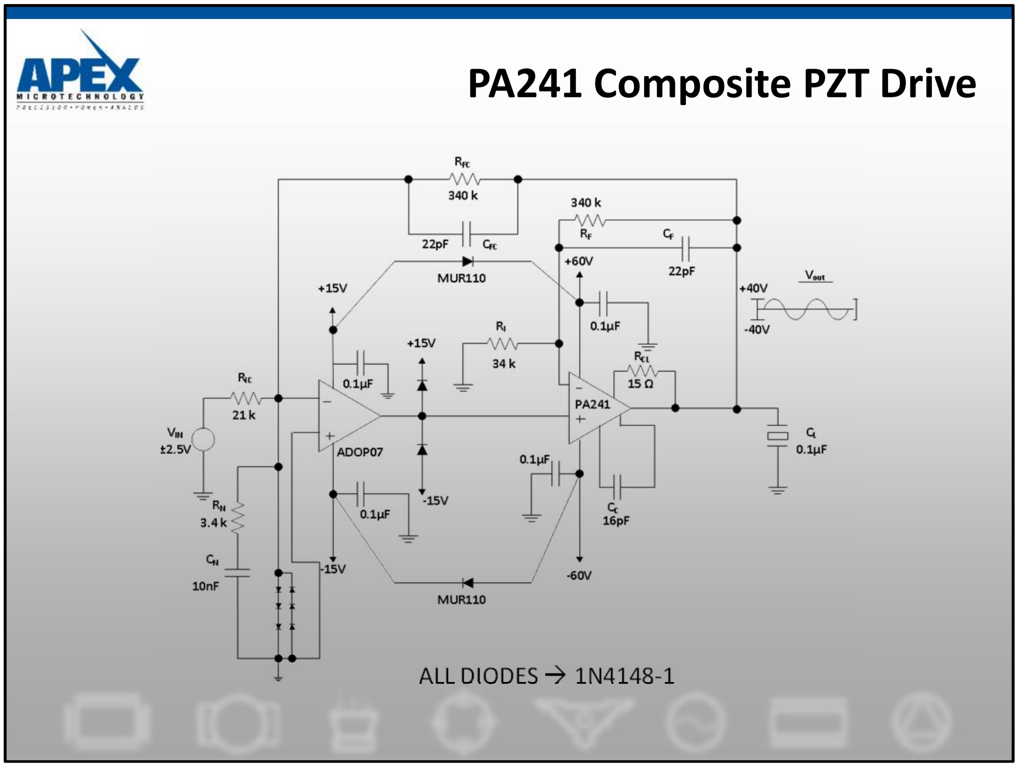
In this application we use the dual supply bridge configuration to deliver up to almost twice the supply voltage of 530V across the load. A1 operates in a gain of 50 to translate the +/–10Vinput to +/–500V out of A1. A2 then inverts this output to add an additional –/+500V across the Piezo to yield a net +/–1000V.

A2 uses noise gain compensation to allow its Vo/Vin transfer function to remain at –1, though its compensation capacitor Cc is set for a gain of 50. The noise gain will allow AC stability as well as a balanced bridge since both amplifiers are now compensated identically for the same slew rate.

Input protection diodes, output flyback diodes and proper component selection enhance reliability. Remember to select Cc capacitors with a voltage rating of at least 1100V, RI, RF, RIS, and RFS with proper power dissipation and voltage coefficient of resistance, and D1 - D4 with a PIV of at least 1100V.

As a final note remember to check the amplifiers for AC stability due to capacitive loading depending upon the capacitance of the piezo being driven.

Ref. AN25



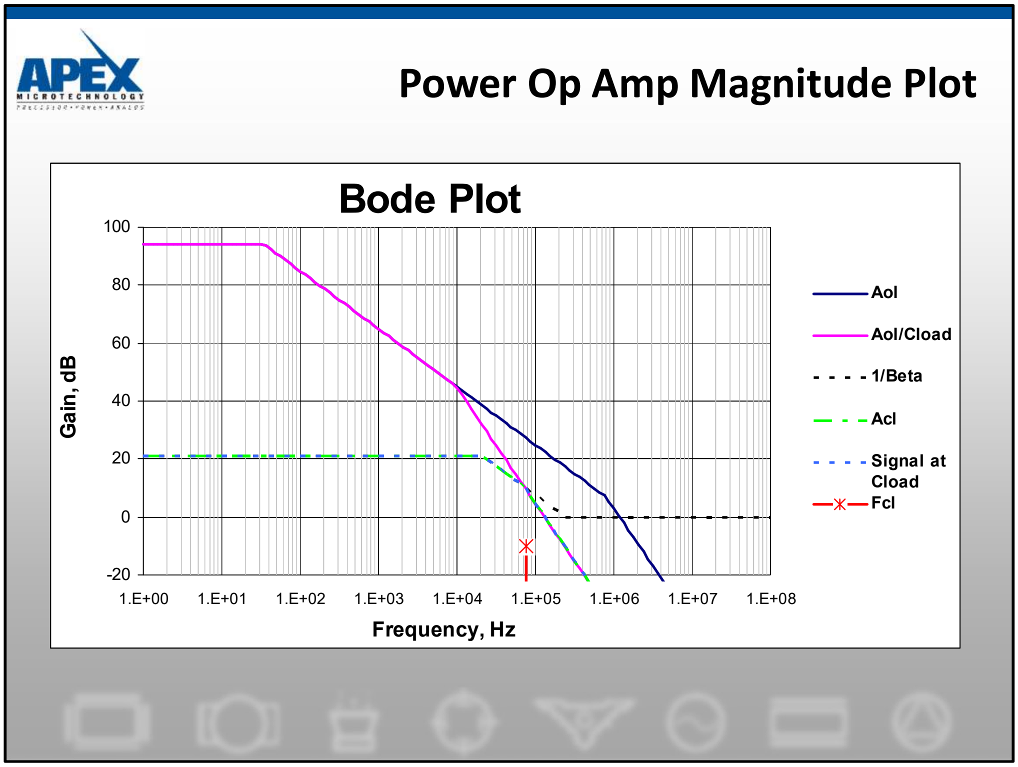
This circuit is included as an example in Power Design.xls. It is different from most power op amps in that current limit from positive side to negative side does not match well at all.

We will start by stabilizing the power stage, then the composite. Then we will examine current limit and frequency limitations imposed by this current limit.

1N4148 diodes on the input of the OP07 provide differential and common mode over voltage protection for transients through Cfc. Diodes on the output of the OP07 prevent over voltage transients that can occur through Cf,through the PA241 input protection diodes to the OP07 output through the PA241 internal input protection diodes.

Fast recovery diodes between pairs of supplies ensure that the PA241 input stage is protected from over voltage in the event the ±15V supplies are up before the high voltage supplies.

Ref. AN19,AN25



In any composite amplifier, make sure the power output stage is stable first. Any of the techniques we learned earlier can be used.

Ref. AN19, AN25

Composite Amplifier Set-up

Composite Circuits

38 Goto Main Circuit

MODEL	OP07	READ ME			
Aol =	135	dB	Pole 1 =	0.1	Hz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz
Rin	21	Kohms	Rn	3.4	Kohms
Rf	340	Kohms	Cn	10	nF
Cf	22	pF	Using Look-Up data		
Notes:					

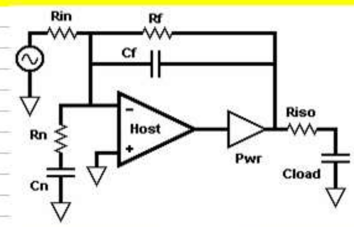
Estimated Closure Frequency =	56.23413 KHz
Suggested maximum bandwidth	5.623413 KHz
Estimated Closure Rate =	20.0 dB/decade
Estimated Phase Margin =	50.625 Degrees

Load Host Data

R-C Pole Calculator:

3.4	Kohms	47	Kohms
5	KHz	10	nF
9.36206	nF	0.338627538	KHz

1/Beta (DC)	24.7	dB
Noise Gain	16.7	dB
Pole Noise Gain	4.681027677	KHz
Zero Noise Gain	0.68665214	KHz
Pole Cf/Rf	21.27739871	KHz
Zero Rf/Cf	2493.508487	KHz

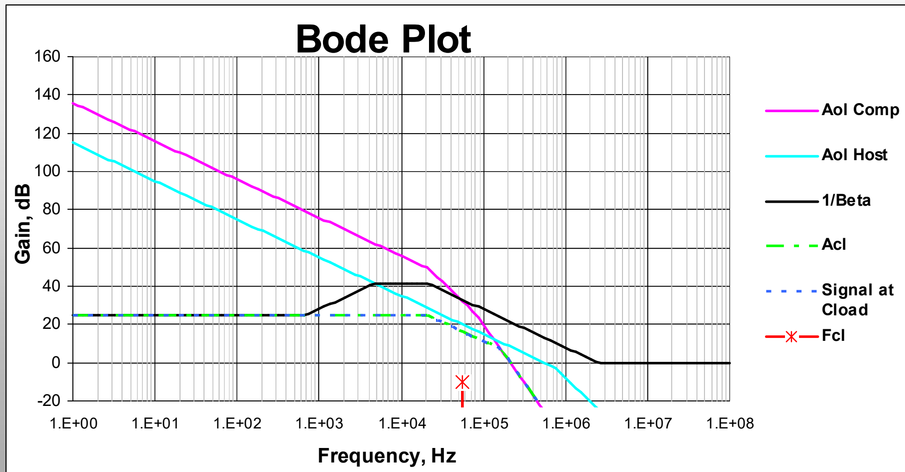


30 Print Data, Bode & Phase

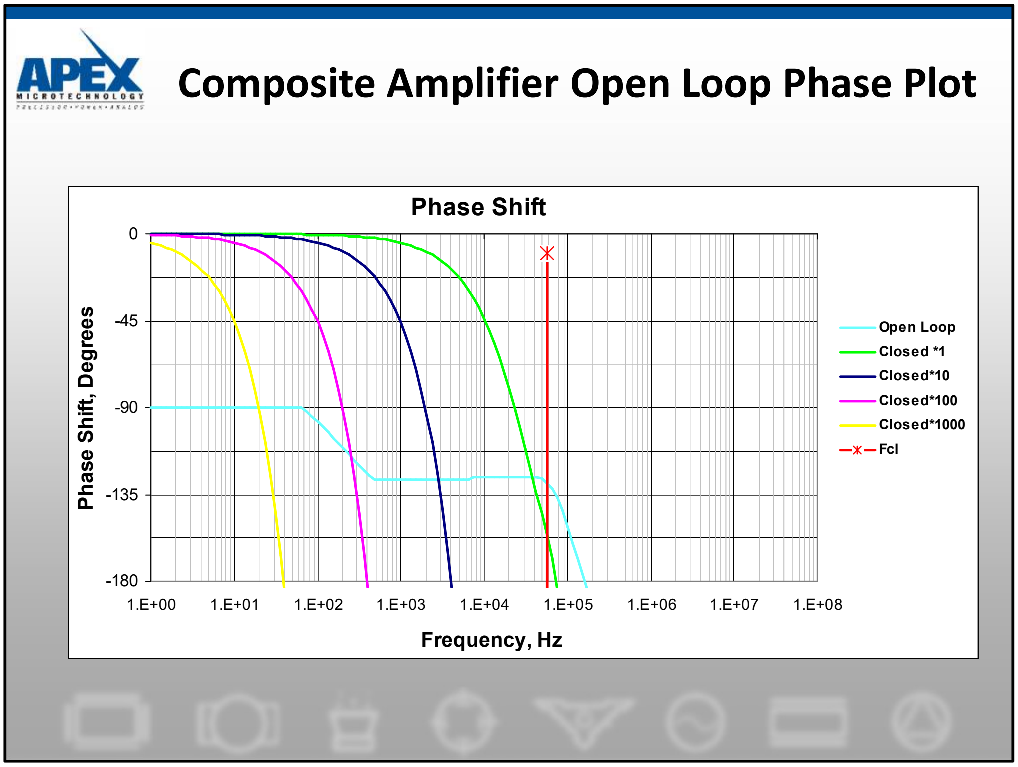
31 Print Data, Bode, Phase & Parts

Ref. AN19, AN25, AN38

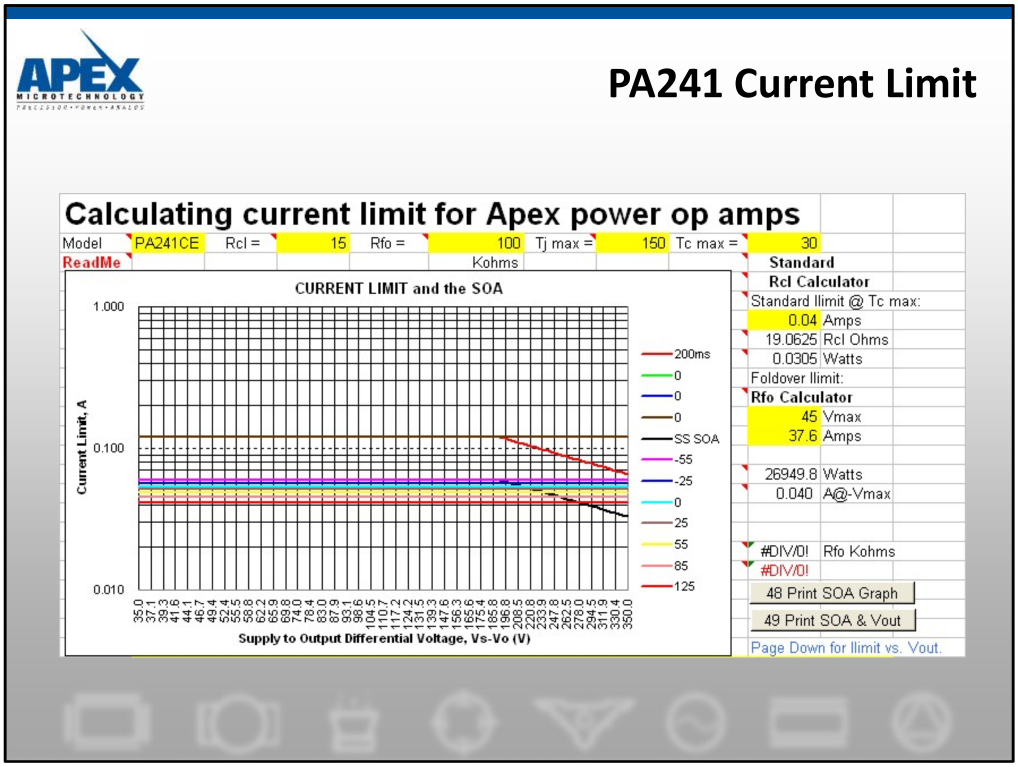
Composite Amplifier Magnitude Plot



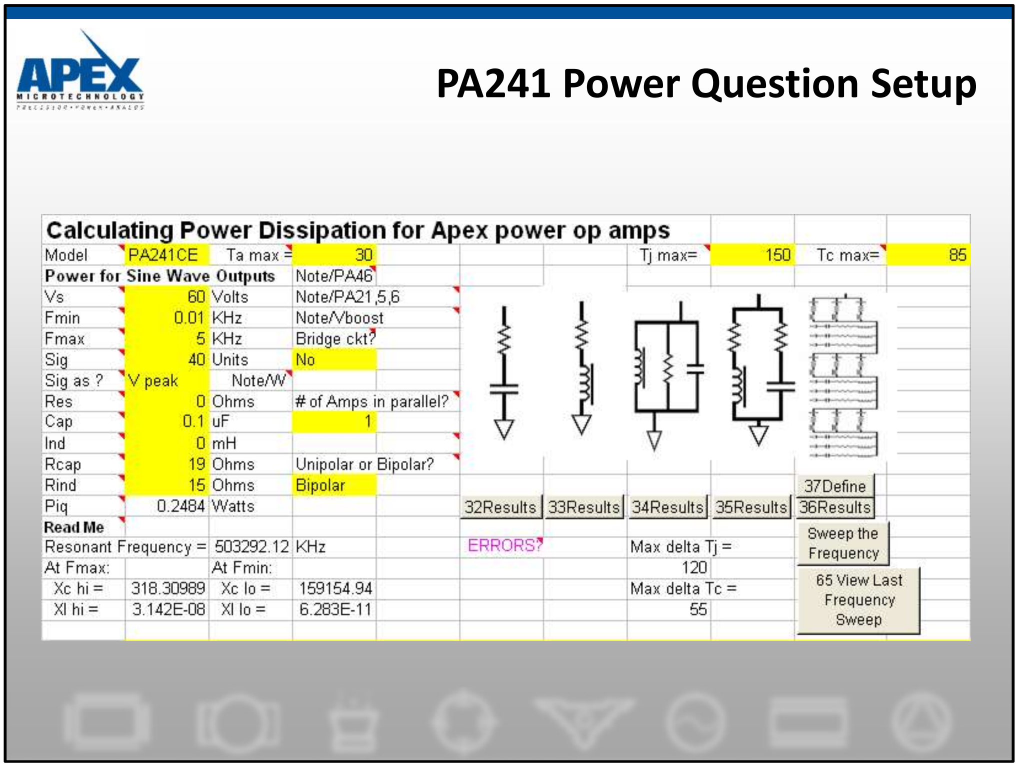
Ref. AN19, AN25, AN38



Ref. AN19, AN25, AN38



The amplifier selection, load and voltages have all been given. The only frequency that matters is the maximum (no current into a C load at DC). Our stability analysis suggested a maximum of about 10KHz (the Rf-Cf pole frequency).
Ref. AN37



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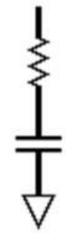
Ref. AN37

Speed is Limited by Iout

	At Fmin:	At Fmax:		At Fmin:	At Fmax:		
Z in Ohms	159154.94	318.30989		Maximum AC Pint			
Phase angle	-90.00	-90.00		60	60	Vpk	
RMS Amperes	0.0001777	0.0888577		42.426407	42.426407	Vrms	
Peak Amperes	0.0002513	0.1256637		0.0002666	0.1332865	Arms	
RMS Volts	28.284271	28.284271		0.0113097	5.6548668	Wrms	
Peak Volts	40	40		7.108E-15	1.777E-09	Wtrue	
RMS Power	0.0050265	2.5132741		0.0143997	7.1998695	Pin	
Peak Power	0.0100531	5.0265482					
Power factor	0.000	0.000		Minimum HS:		9.89	°C/W
Input power	0.01	4.80					
True power	0.00	0.00		Actual HS:		5.2	°C/W
Percent Efficiency =	1.95	49.78		Results in Tjmax =		92.68	°C
Vpk capability =	51.65	40.23		Results in Tcmax =		61.2995407	°C
Op amp internal dissipation:							
Input power	0.01	4.80					1
Dissipation RMS	0.0095998	4.80	38 Data Input				0
Dissipation Peak	0.02	8.76		CURRENT TOO HIGH!			0
Total in heatsink	0.27	5.05	39 Print Results	HS/Tcase	HS/Tj	Larger	1
WC watts & Rth	5.048313	6.5		9.8947286	16.55461	9.89472857	
Readme							



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255mA would be required to drive the .1µF load at 10Kz! Notice the “CURRENT TOO HIGH!” flag at the lower right. This is based on data sheet maximum, not the current limit resistor used. Since this is 10x our capability, 1KHz will be the limit with a 75Ω current limit resistor. When this is plugged in, we will find normal operation with no heatsink is possible. To analyze fault conditions, find the lowest impedance to be encountered, assume the current limit (47mA in this case) is driven into the load and calculate the output voltage. Subtract this from the supply voltage, compare to the SOA of the amplifier and calculate a larger heatsink as required.

Ref. AN37