Printed Circuit Board Layout for Linear Switching Amplifiers

SECTION I: PURPOSE

The purpose of this application note is to provide engineering development teams with a series of best practices to use in designing printed circuit boards (PCB) for the evaluation of power linear and switching amplifiers. If five people are polled about the proper techniques for laying out such a circuit board, there might be as many as ten opinions. When taken into consideration, most concerns do actually matter; with the unknown factor being how significant is their contribution. An engineer knows that on some level, all parasitics impress upon a circuit. With that said, this application note is written to facilitate cohesiveness between the engineers working on the project. When viewed from a team perspective, the race to the end can be better controlled to result in fewer changes, a reduction in errors, a reduction in cost, and the removal of the need to debug or to re-spin. This in turn reduces time to market. It is key to remember just how often the existing intellectual property can be re-used and instantiated into the next generation design. A successful design saves money now and also saves money down the road. If this methodology is adopted, it will help to ensure success and increase the design team's effectiveness and productivity.

Best case practices of a layout cannot be discussed without consideration of the progression of the PCB's design. Ideal practices can be put in place to mitigate error and alleviate time lost to debugging. This process begins before schematic capture and originates with the concept of the circuit. This circuit is intended to be a solution to a challenge generally revolving around some sort of power conversion, some sort of control circuitry, and some sort of communication. When engineering a circuit solution, the engineer must weigh ideal versus practical considerations. With the identification of a practical solution, the engineer begins to identify the concessions that bound the application. The focus of this document will be to explore a specific set of concerns and how a proper layout can help to control, and positively influence, key parameters of a design. The layout can help ensure proper operation and stability of the circuit. Furthermore, proper consideration can help to ensure the circuit is able to survive sustained usage. The layout must take into account the mechanical and thermal stresses caused by the electrical circuit and the respective components. Under certain conditions a completely acceptable design can self-destruct, and as such, the manufacturability of the PCB should remain in the back of the circuit designer's mind. In addition, the designer must always be concerned with noise, whether it is radiated from within the circuitry or conducted. If this school of thought is accepted and time is taken to implement certain layout principles, the result will be a consistent savings of time and money, while expertly engineering a robust design.

Most application notes briefly touch on the design of the circuit and its chain of custody. Ideally, a single electrical engineer (EE) would develop the circuit and generate the layout. There is no need to highlight the absurdity of that statement. In actuality, the circuit design is done by an EE (whether the EE be digital, analog, systems, or applications engineer) and then reviewed by colleagues, usually resulting in hasty additions. The PCB designer then takes their cue from the EE and begins the layout. Down the road the EE makes some edits or fails to tell the PCB designer some piece of information and but now the designer has already done the placement and routing. This forces a component push and trace to be bumped. Some say this is just the way it goes, but this is not accurate. The back and forth, and the unintended consequences of the push and bump method, can be removed with the implementation of some specific procedures. This aids in synergy and creates cohesion within the team. A design is not a hot potato. It should be a baton. This document is broken into several sections: the big picture, the schematic capture and the layout itself.

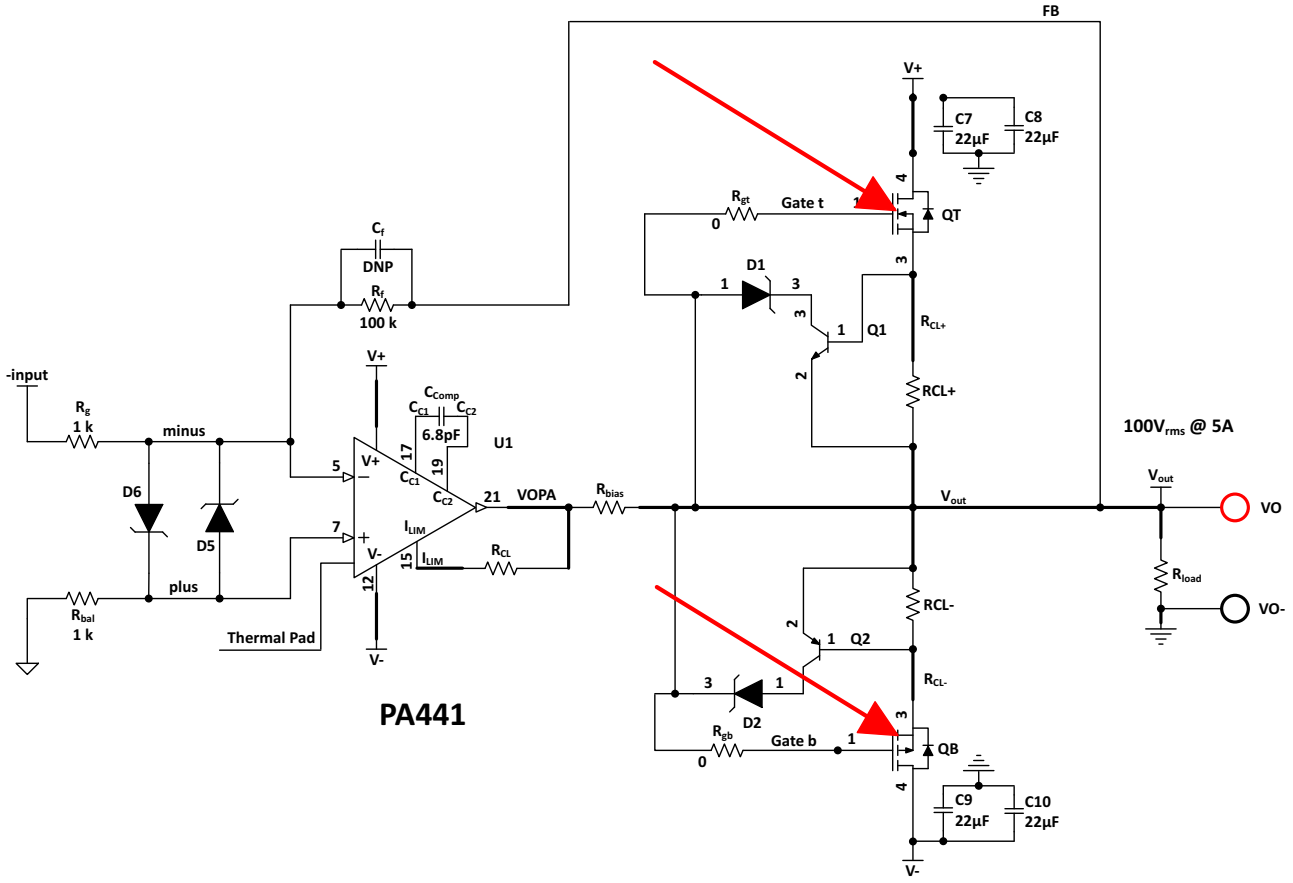
SECTION II: THE BIG PICTURE

The “big picture” can be described as a list of specific concerns that should be understood by the team when engineering a solution. This requires an understanding of the discrete components being used; the tolerances of the passives; and what takes place period by period. It is critical to determine what takes place instantaneously and during crossover, transitioning or switching cycles. The identification of the high current paths and what components are in the on-state is paramount. The DC operating points are not trivial; many designs have been degraded due to an oversight of DC performance. The voltage ratings must be identified, in addition to the nominal current, the peak current and power dissipation. A common practice is to set the current limit to 120% of nominal. The limit will vary over temperature. The following is a series of recommended *Best Practices.*

BEST PRACTICE: IDENTIFY THE HIGH CURRENT PATHS AND LOOPS

The MOSFETs, BJTs and diodes are easily identifiable. From this point, the high current paths can be identified. These are transitioning loops that need to be minimized. It is important to identify the duty cycles/periods and to understand the on time and the off time. Take care to understand the effects of parasitic inductance on these paths.

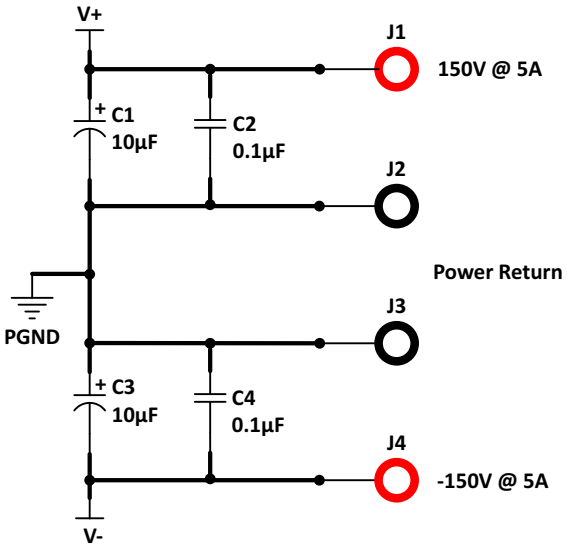
Figure 1:



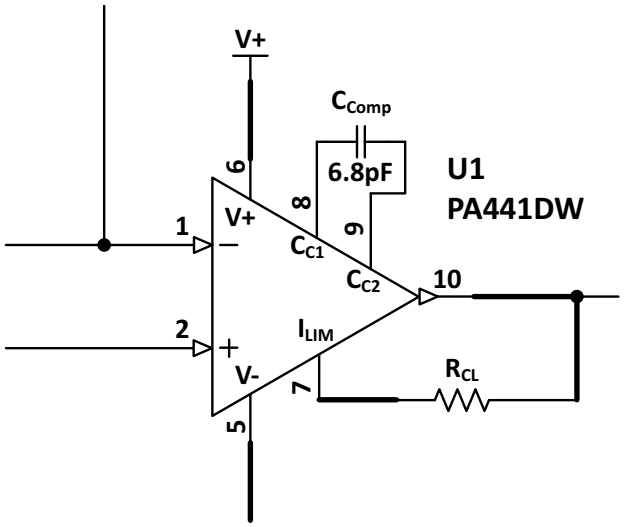
BEST PRACTICE: BE DELIBERATE IN CHOOSING THE CAPACITORS FOR THE DESIGN

These selections are frequency dependent/layout sensitive and the said value is never its true value. Take the time to choose the capacitor based on the electrical function it will support.

Figure 2:



Use electrolytic to supply charge, Use ceramic for filtering



Compensation should be high quality and rated for the entire differential supply voltage

With the increasing voltage range of surface mount ceramic capacitors (7kV), high quality ceramic can be used to decrease the distance of the compensation capacitor to the pins.

BEST PRACTICE: RESISTORS ARE A SOURCE OF ERROR, NOISE AND LOSSES

Some resistors matter and some are just resistors. Over time, an understanding of which resistors truly matter will develop. For example, is it a current sense or a current limit resistor? Is it a resistor that sets a frequency or sets a clock? Is it simply a divider? Each resistor has its own characteristics.

Figure 3: Axial Versus SMT

Current Sense, Moisture Resistant, Non-Inductive, Non-Magnetic

AEC-Q, Current Sense, Moisture Resistant, Pulse Withstanding, Low Inductance

BEST PRACTICE:IDENTIFY THE NOISY SIGNALS IN THE CIRCUIT

Identify switching noise, radiated noise and high power returns. It is imperative to identify the on time and off time of the transistors. Locate the gates, the clock and the digital signals. Once complete, the next step in the design process is the placement of the components. This can be a source of many errors and should be done methodically. If a component is added during a design review, take the time to add and edit, do not just cram, bump and push the part in a negligent fashion. At this point, be certain time has been taken to identify the high current loops and the high speed transitions. The high current loops are the critical nodes that must be engineered to be low impedance. A semi-copper trace is an impedance that is fluctuating (consider thermal expansion). Take time to get familiar with current density theory and its geometrical deterministic property. Let us discuss the benefit of low resistive planes/pours. The routing and placement of the capacitor can destroy the benefit of its usage. Length increases resistance while an expanded cross section will diminish resistance. As the magnetic field around a conductor fluctuates, so does the induced voltage on the signal. The one sure way to combat inductance is to shorten the trace.

$$V = L\frac{di}{dt} \qquad 1V = 5nH\frac{2A}{10ns}$$

BEST PRACTICE: ENSURE THE PCB IS MANUFACTURED TO WITHSTAND SUSTAINED TESTING AND USAGE

The engineer must consider the stack up and the manufacturability of the design. Consider the pick and place machine. Think of the board flex. Will there be a need for strain relief due to cabling? Take the time to consider heat sinking and stand offs. Be meticulous and think about re-work and testing. Take the time to define the stack up. What is the copper weight/thickness? What are the minimum and maximum via sizes? What layers are the power planes? What layers are the solid returns or the quiet signal grounds? What layer will I be routing on? Take some time to learn about copper and its weight/thickness. What is the expected efficiency of the design? Where are the losses? What is the ambient temperature? What are the minimum and the maximum trace widths? What is the spacing for the weight/thickness chosen?

BEST PRACTICE: OPTIMIZE THE STACK UP FOR SHIELDING AND HEAT SINKING

L1 Power Plane and High Power Components
L2 Power Planes repeated (thermal consideration)
L3 Solid ground (shielding to protect small signals)
L4 Small signal components and sensitive traces

Figure 4:

BEST PRACTICE:DO NOT FORGET CIRCUIT PROTECTION, ADD EXTRA LAND PATTERNS

Is a series diode needed? Perhaps a 3.3ohm for input protection for the semiconductors? Does the circuit need a snubber? Whether for input, flyback, or switching spikes? Add a gate resistor and maybe a diode to help turn off the MOSFETs. Is the amplifier adequately protected? Is the current limit resistor Kelvin sense? Does it need a noise filter?

Figure 5:

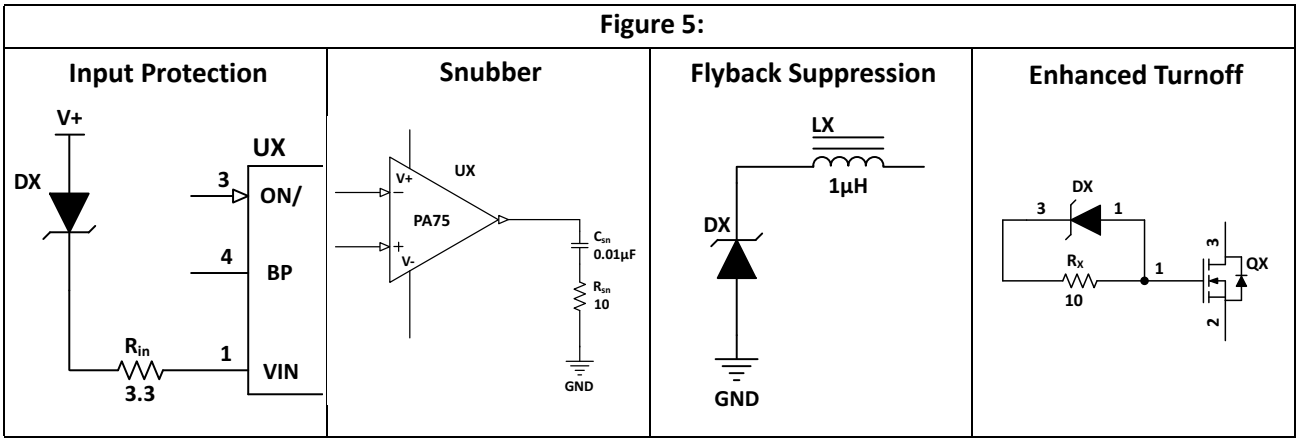
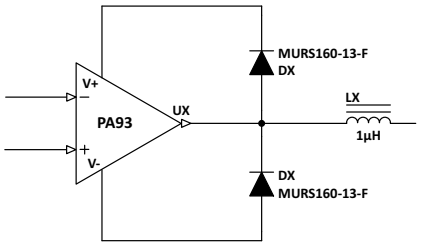
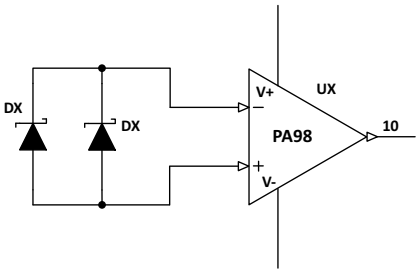
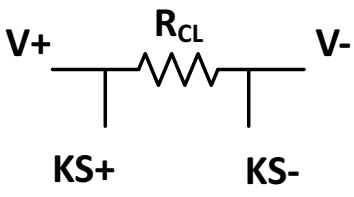


Figure 6:

Rail to Rail Protection	Input Protection	Kelvin Sense
		

SECTION III SCHEMATIC CAPTURE

Some designs are complex and some can be created in the mind. The scope of this article is intended for complex designs. Take for example the need to excite a transducer, move a motor or to convert AC to DC or DC to DC. The origin of the design is the need to provide a company with a solution. Many times this starts with a previous design and migrates to latest and greatest. A design should start in MATLab, Excel or Math-Cad. The calculations are usually done in conjunction with reading of the data sheet. Once the correct values have been calculated it is time for a simulation. During simulation it is time to start thinking about how to debug the circuit board.

BEST PRACTICE: DO I HAVE ALL THE HOOKS IN PLACE TO PROBE?

BEST PRACTICE: MAKE TIME TO READ THE PRODUCT DATA SHEET

This is where the majority of errors can be caught. “There is never time to do it right, but there is time to do it twice.”

BEST PRACTICE:TAKE TIME TO SIMULATE THE DESIGN.

The schematic is a visual representation of a printed circuit board; therefore, it should represent the circuit board. Be certain to think through the flow of signal connections. It is good practice to use a top page for the block level diagram. When designing a system, the ability to clearly see the solution is far more important than how many pages it covers.

BEST PRACTICE:BEGIN WORKING LEFT TO RIGHT

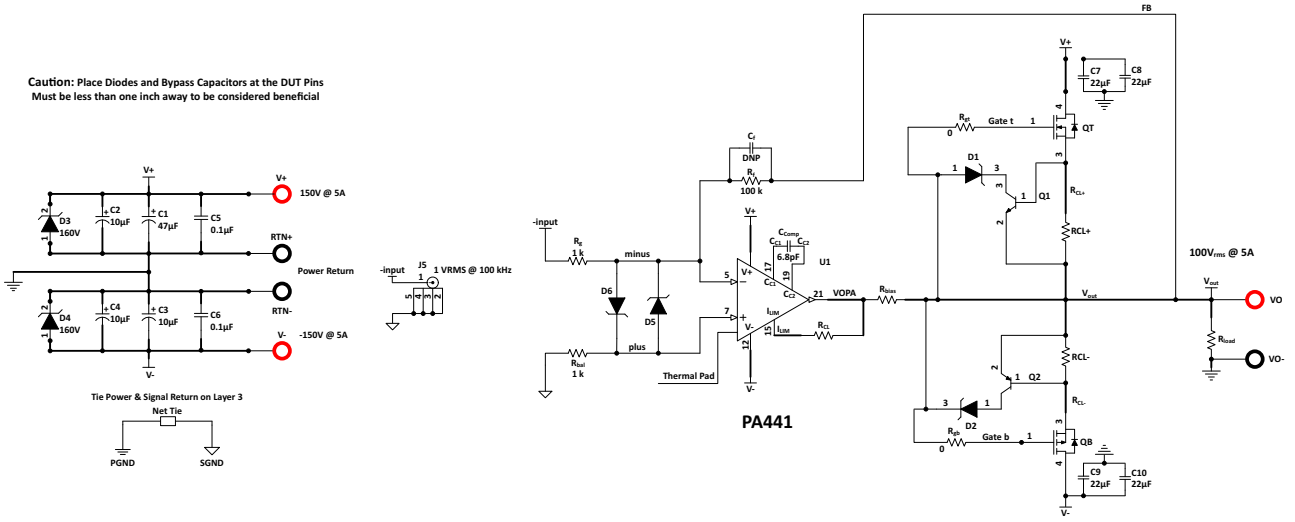
This is an industry standard. Control the flow of the schematic inputs and outputs. The schematic page enables all who view it to understand the function of the circuit. The details need to be easily viewed and understood. As any engineer knows, the schematic may be used to debug the PCB or to repair the board months or years later. The bill of materials (BOM) is a generated output that can wreak tremendous havoc with the efficiency and effectiveness of the design. Some designs will utilize variants. So it is important to utilize the tools provided by the software. This will ensure the correct instance of the design is populated and works correctly.

BEST PRACTICE: THE BOM IS GENERATED BY THE SCHEMATIC.

Do not use the common practice of slapping down components as place holders and calculating them later. All values should be calculated in the design of the circuit/solution using Excel, MATLAB or Mathcad. A

perfectly generated BOM will also save time. It is the engineer's responsibility to ensure the PCB is assembled correctly. Pay now or pay later. Either way it will take time – time to configure the bill of materials or time to debug a board.

Figure 7:



For Example: VIN, VOUT, Frequency, IOUT, Current limit, Pulse duration, power, soft start, UVLO, OVLO, ENABLE

BEST PRACTICE: AN ENGINEER SHOULD BE ABLE TO LOOK AT A SCHEMATIC AND KNOW EXACTLY WHAT SIGNALS ARE BEING APPLIED AND EXPECTED

When placing components on the schematic, ensure the proximity is in relation to their importance. Take the time to read the PCB data sheet. A well written data sheet will highlight critical components. This is one of the areas were the data sheet highlights potential mistakes. Also, experience will teach the engineer what components truly matter. Design reviews can inhibit the need to re-spin a board due to an oversight. The idea is to assign hierarchy to components and their location to its parent component. Every component does not need to be right up against the device. For example, here are two extremes: the compensation capacitor versus an enable divider. When wiring these components, label the nets. This will enable the PCB designer to know exactly which components are paramount when doing the placement. This is the time to adjust the thickness of the wire on the schematic. It's as simple as a right click. This will enable all who look at the wire to know to widen the trace. This is also another good place to insert text to show for example "5Vout @ 20A." Now it is clear this will be a copper pour. Also, when labeling nets, the digital signal paths illuminate themselves to the PCB designer. Now the PCB designer will have to identify a digital signal portion of the printed circuit board.

BEST PRACTICE: CREATE A SECTION OF THE PCB FOR ALL DIGITAL SIGNALS TO ENSURE AN INPUT DO NOT CROSS AN OUTPUT, DO NOT RUN A CLOCKING TRACE OVER A HIGH IMPEDANCE NODE

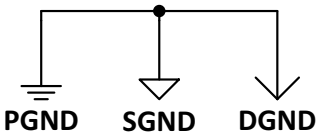
As was mentioned earlier, when wiring the schematic, it is important to note the loops. If the wire size is adjusted to indicate the current carrying loops, the small signal components are now easily discernible to the PCB designer. This will also help to determine the stack up. How many planes does this design need? What areas need to be shielded, mimicked? Which areas require thermal relief? Asking and answering these critical questions will ensure the PCB can survive sustained usage.

Clearly identify the return paths by using the ground symbols respective to their identities. Use the three symbols and explicitly tie them together in an exact location. Do not leave it up to the convenience or the

polygon/plane tool. Some tools allow the selection of a location for a short. This is a convenient way to tie analog and power ground together. Exceptions can be made for a short in a specific location of the chosen layer. Another trick is to tie the grounds together last, this will ensure control and fidelity of the signals. As simple as this sounds, this is the one step where the majority of the grief can be eradicated.

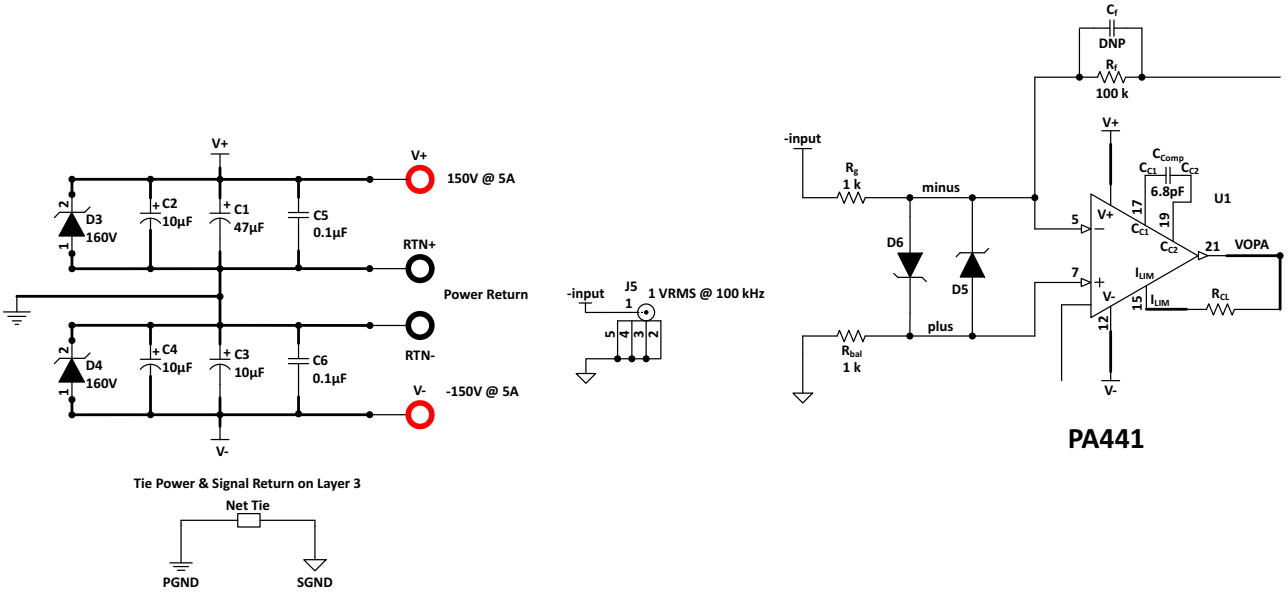
Figure 8:

Tie Power, Signal, & Digital Returns on L3



As stated previously, care must be taken to ensure the return paths are separated. But why? First define ground as the return path. Also define the return path as a reference point. This reference point has an impedance; therefore, with current flowing, a voltage drop is created. This is another simple concept that wreaks havoc with circuitry. So by separating high current returns from the small signal return, less noise and variation is introduced into the design. This leaves the digital return path. The idea is to separate fast digital switching from the small signal circuitry. These high speed clocking signals can couple and induce spikes onto adjacent signals.

Figure 9:



BEST PRACTICE: USE THE RETURN SYMBOLS TO ENSURE ALL COMPONENTS HAVE THE CORRECT RETURN SYMBOL AND ARE CONNECTED BY DESIGN WITH DELIBERATE FORETHOUGHT AND INTENTION

There is one step between the schematic capture and the printed circuit board layout. Each design is different, but many times the design rules are the same. The design rules must be considered early in the schematic conception. Many items concerning the physical properties of the board should be conceptualized during the schematic capture.

BEST PRACTICE: TAKE THE TIME TO SET UP DESIGN RULES AND USE THEM

Save all design rules to a file. This will allow the rapid import of rules for specific cases. Many times these items are not considered until late into the design process. When left to the last minute, this will force the components to be pushed and bumped to meet fabrication rules. Use the schematic as a blueprint for proper routing. Use the top level sheet to indicate the stack up. Use text to indicate the critical trace route. Use the schematic features to create rules for trace width. This is the time to be using trace width calculator tools. High voltage solutions require special attention to conductor spacing, trace width, isolation, creepage, and clearance. If unfamiliar with flashover or tracking, now is the time to read about it. Even when defining low voltage and low current designs rules, ensure the minimum space is clearly defined. This is usually defined by the solution density and copper weight/thickness of the printed circuit board. This in turn defines the cost of the board.

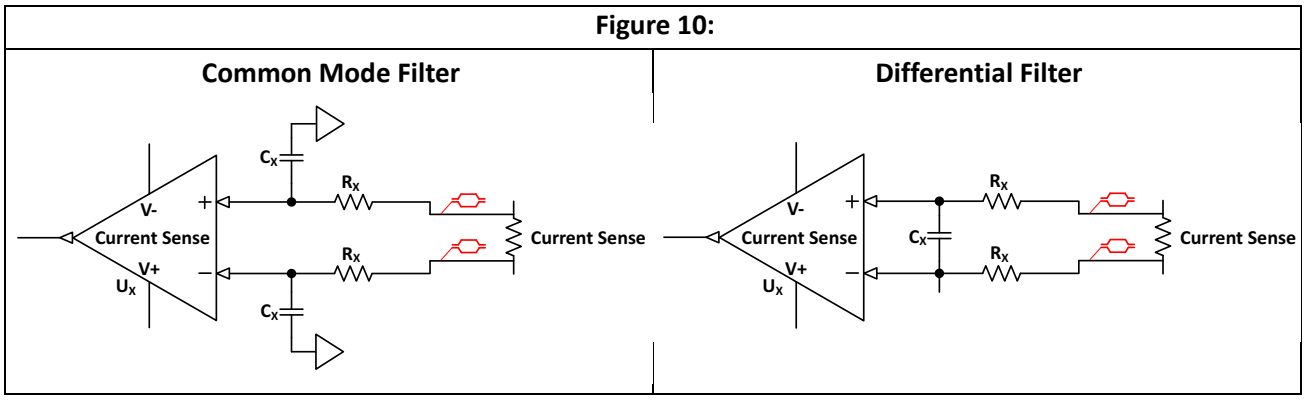
BEST PRACTICE: PROTECT NOISE SENSITIVE TRACES

Ensure noise sensitive traces are routed away from noisy components and signals. Some examples are sense lines and feedback traces. Take the time to model schematic symbols to allow for Kelvin sensing of current limit circuitry.

BEST PRACTICE: USE A DIFFERENTIAL PAIR TOOL

Indicate the following signals as differential pair high speed signals (plus and minus), current limit Kelvin sense, high gate, switch (PWM signal), low gate and ground, current sense positive, and current sense negative.

Figure 10:



SECTION IV PRINTED CIRCUIT BOARD

Thus far the schematic has been clearly defined. The stack up has been agreed upon and the layer assignment is set. The team has reviewed the integrity of the design. The critical loops have been identified and the standard practices have been adhered to. It is time to begin the placement. The simplistic view is to start with each DUT and begin placing the paramount components near their respective pins. Once the critical components have been identified, ensure the proximity is very close to the device. The remaining components are less important but not paltry and normally provide a DC signal.

When considering the stack up and placement, the ambient temperature and the temperature rise should always be of concern. What is the virtue of a completed design that simply suffers from thermal runaway? Here is a look at a simple four layer design.

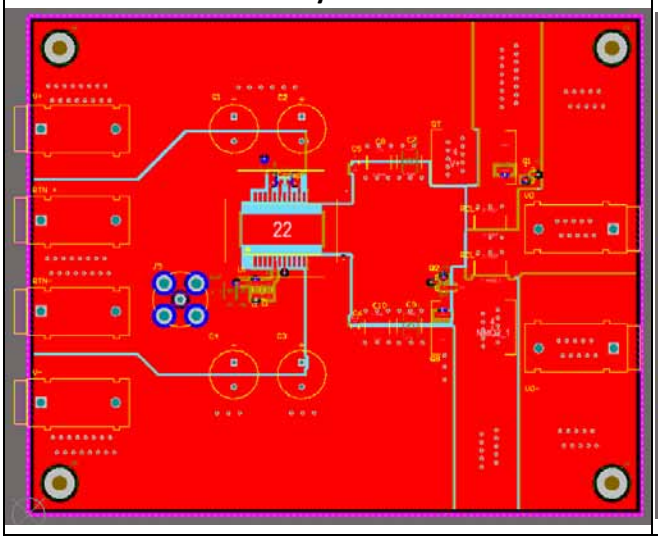
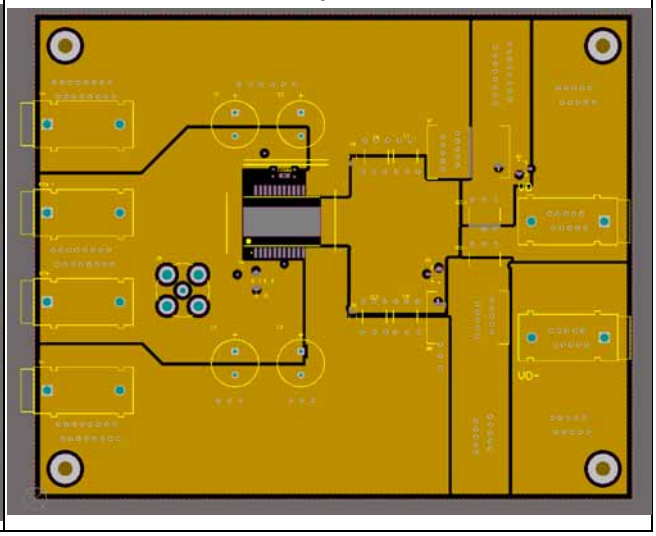
Identify the power components. They will be placed on top in a tight loop. Preferably the power ground wraps around to meet the power ground out. This is simply a matter of placing the capacitors in the correct orientation so the copper pours flow nicely together. The top two layers should have adequate copper to

allow for power dissipation and the power delivery. Layer three is a solid ground plane shielding the small signal components, the small signal traces and anything not carrying current. These signals are routed on the bottom layer to protect from the radiated noise of the top two layers. Layer four components must be placed in order for the signals to be routed cleanly with enough space to avoid coupling.

BEST PRACTICE: NEVER BOUNCE A TRACE (PLACING A TRACE UP AND OVER AN OBJECT THROUGH A VIA) BECAUSE THERE IS NOT A DIRECT PATH.

To bounce a trace means that either the placement is incorrect or the routing is less than acceptable. When possible, use solid copper pours to deliver or radiate power. A power plane ensures adequate thermal relief. This is the time to determine via placement and size. The power planes accommodate the necessary current carrying capability and power distribution. Planes also provide extra heat sinking for power dissipation. The added geometry reduces inductance. Ensure the design has adequate spacing to meet high voltage requirements.

Figure 11:

Layer 1	Layer2
	

Some engineers are forced to choose components that are on an approved vendor list. Some engineers choose components because that is the part number on the previous revision. Not all, but some engineers, take for granted the quality of the passives. When asked “does the BOM really matter?” The answer should be a resounding “YES!” Many designs have failed because of an incorrect rating of a passive. On some level, every component can interfere with a robust solution. The following is a comprehensive, but not perfect list of parameters to identify.

Questions to ask: what is the equivalent series resistance? What is the equivalent series inductance? What is the leakage current? Let us examine the statement, “but it’s just a resistor.” It is important to understand the consequences of low and high inductive resistors. What is the makeup of the resistor? Is it wire wound? Is it a current sense resistor? And if so, is it inductive? What is the power rating? What is the temperature coefficient and tolerance? If it is a current sense resistor, what is the recommended land pattern? Yes, it does matter. Has it been taken into account the current density and thermal EMF? Every connection made with dissimilar metal creates an unwanted thermocouple.

Here’s an examination of the statement “but it’s just a capacitor.” It is imperative to understand the function of each particular capacitor. The job of the capacitor is to supply charge, to filter and to stabilize a volt-

age. The ideal capacitance of a capacitor is never the true value. A word of caution: a capacitor will de-rate over frequency, time and temperature. If it is subject to overheating, to an over voltage event, or even over current, the best practice is to remove and replace it. Starting with the bulk capacitor, whether on the supply lines and or the output, this capacitor is used to supply charge to the load. It is paramount to identify the voltage rating (tantalum vs. liquid - be sure to note the indicator). Another specification that can work for or against is the equivalent series inductance. When verifying the voltage rating, check the ripple current rating as well. An overly general statement is that ceramic capacitors are used to stabilize a voltage or filter a signal. When choosing a ceramic it is necessary to start with the signal, the frequency and the ambient temperature. Ensure the team is on the same page when selecting the correct component. If the capacitor is needed to filter, it should have low inductance. As a general rule, the construction of a capacitor should be understood along with the dielectric and termination type. The use of specialized low inductance capacitors such as X2Y can reduce inductance and help to filter signals.

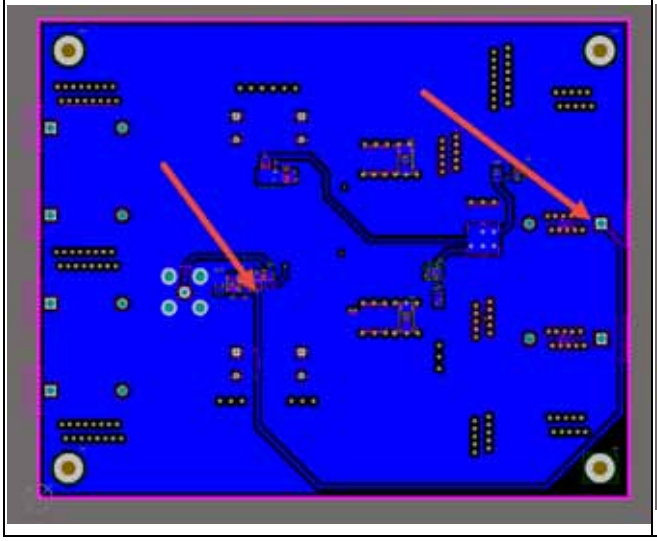
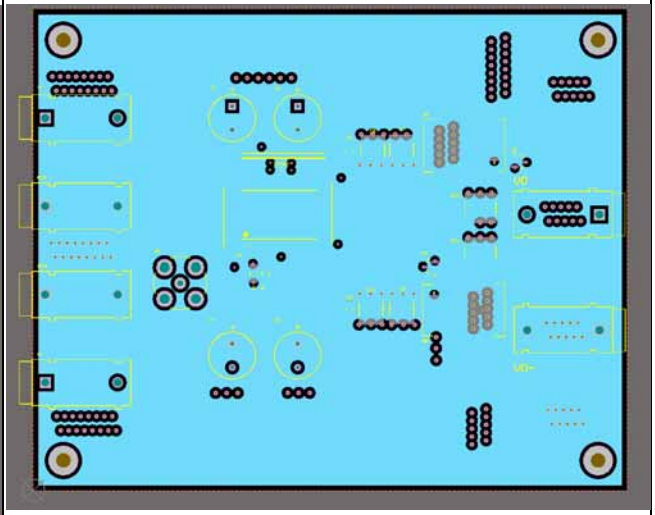
BEST PRACTICE: DO NOT PLACE CAPACITORS NEAR THE EDGE OF THE PCB

Printed circuit boards are subject to flex and thermal stress. The termination ends of capacitors have been known to crack due to fluctuation in the printed circuit board when placed close to the edges.

As mentioned multiple times, one of the most important aspects of layout is placement. This is done to minimize loops and ensure the correct ground scheme. Large loops can cause very large voltage spikes. The input and output signals should never cross. Place decoupling or timing capacitors next to their respective pins. Ensure that the compensation components are placed directly at the pins. Ensure the capacitor is rated for the full differential voltage seen across the supplies. Identify key resistors and place them in close proximity to the pins. Some examples are synchronization, current limit and timing signals. If there are MOSFETS, ensure the placement allows for gate traces to be short and wide. The path to the inductors should be short and wide as well. Ensure the feedback resistors and integration capacitors are right next to the part. Ensure the digital portion of the circuit is identified and strategically placed. This should not cross or couple with other switching routes.

BEST PRACTICE:THE FEEDBACK TRACE SHOULD BE NOISE FREE

Figure 12:

Feedback Trace	Solid Return Shield
	

It is common practice to have the feedback trace on a small signal layer adjacent to a ground plane. While a via may seem to be a simple hole in a printed circuit board, their use and their structure are extremely complex. The via size and annular ring should be determined by the current through the conductor. The restrictions of size are pre-determined by the capability of the board house. The size and quantity should be engineered. Vias are used to move connections from one layer to another. A power via should have an adjacent via in order to minimize the inductance which reduces the length of the loop. For some signals it can be necessary to have two vias per pad. Vias also allow for thermal relief and the ability to more efficiently conduct current on multiple layers. Having too many vias defeats the purpose. An industry colloquialism refers to this as turning a PCB into "Swiss cheese." The PCB construction contributes to the parasitic contribution of the via. The inductance of the via is comprised of the height of the PCB and the diameter of the via. The capacitance of the via includes the hole and the anti-pad, the height and the material (relative permittivity) of the PCB. It is not necessary to commit these formulas to memory; however, an understanding of how the value is calculated can be beneficial.

Via Inductance

$$L_{via} = 2h\left[\ln\left(\frac{4h}{d}\right) + 1\right]nH$$

Via Capacitance

$$C_{via} = \frac{\varepsilon_r \cdot TD_1}{D_2 - D_1}pF$$

h = Length of the via d = Diameter of the via L= Via inductance	D_2 = Diameter of clearance hole D1 = Diameter of pad around via T = Thickness of the PCB ε_r = Relative permittivity C = capacitance
Note: Dimension in Centimeters	

SECTION V CONCLUSION

An engineer takes a concept and creates a printed circuit board. Mathcad, spice, component tolerances, temperature variation, noise and environmental conditions are dropped into a bucket with the expectations that a long term solution to a complex problem will result. Some of the previously mentioned items cannot be controlled. What can be controlled are the method and the principles of the design procedure. When the design team builds cohesion and synergy, the end product will always be better than if one person throws a design at another person and expects them to finish it while the other person runs off to fight the next fire. Implementing the correct mindset for the schematic, from capture to layout, is an upfront cost that can easily pay for itself. Take the time to put in place the best case design principles and ensure that all lessons learned are incorporated. The schematic capture paints the picture and sets the standard for the design. Take the time to envision the printed circuit board from the inception of the schematic. Ensure the design rules and principles are in place. This will save the team money, time and provide increased productivity. One of the best rewards of implementing best case design principles is that they often alleviate or even mitigate issues that were not conceptualizing.

Figure 13: PA441 with Current Buffer

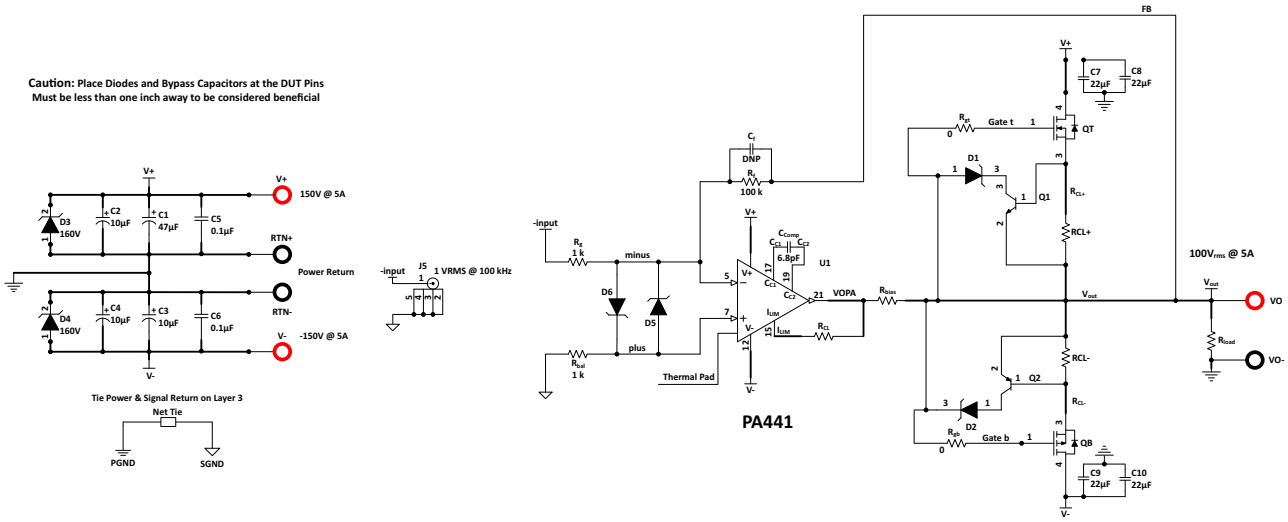


Figure 14: 3D Image

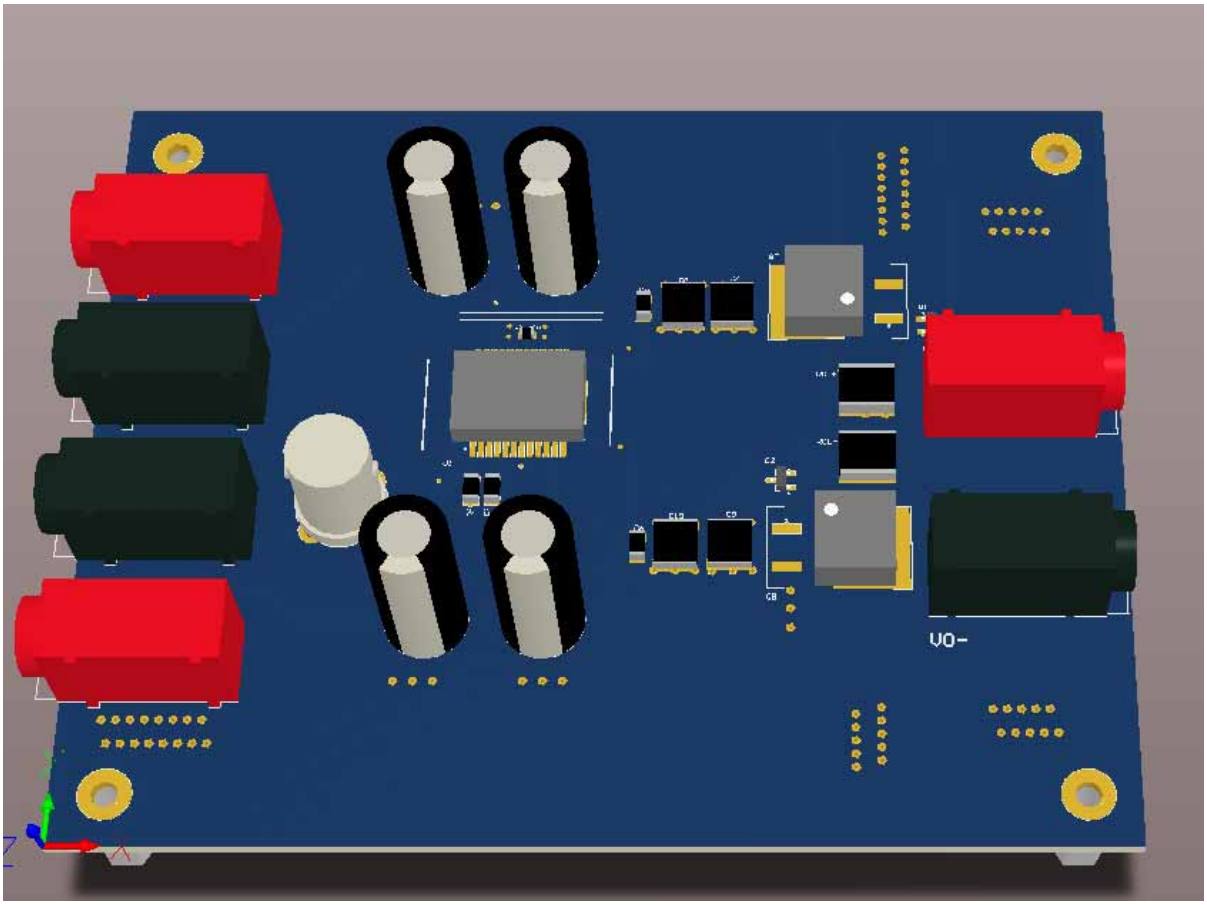


Figure 15: Layer 1, Power

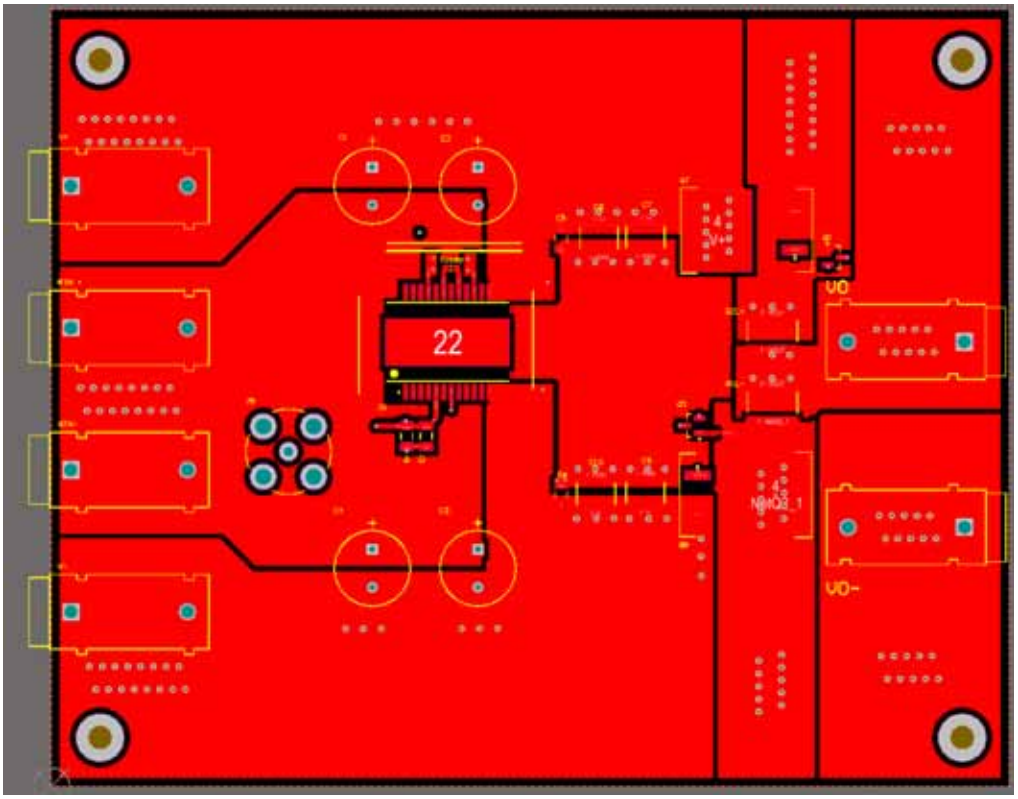


Figure 16: Layer 2, Power

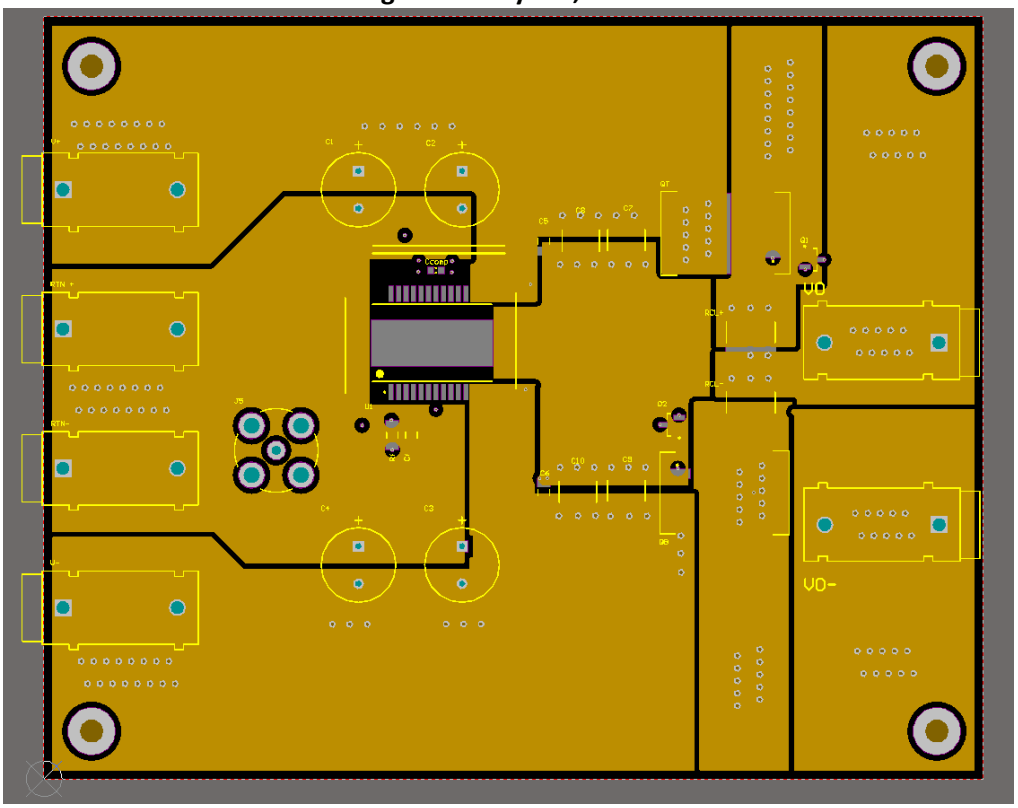


Figure 17: Layer 3, Solid Return Plane

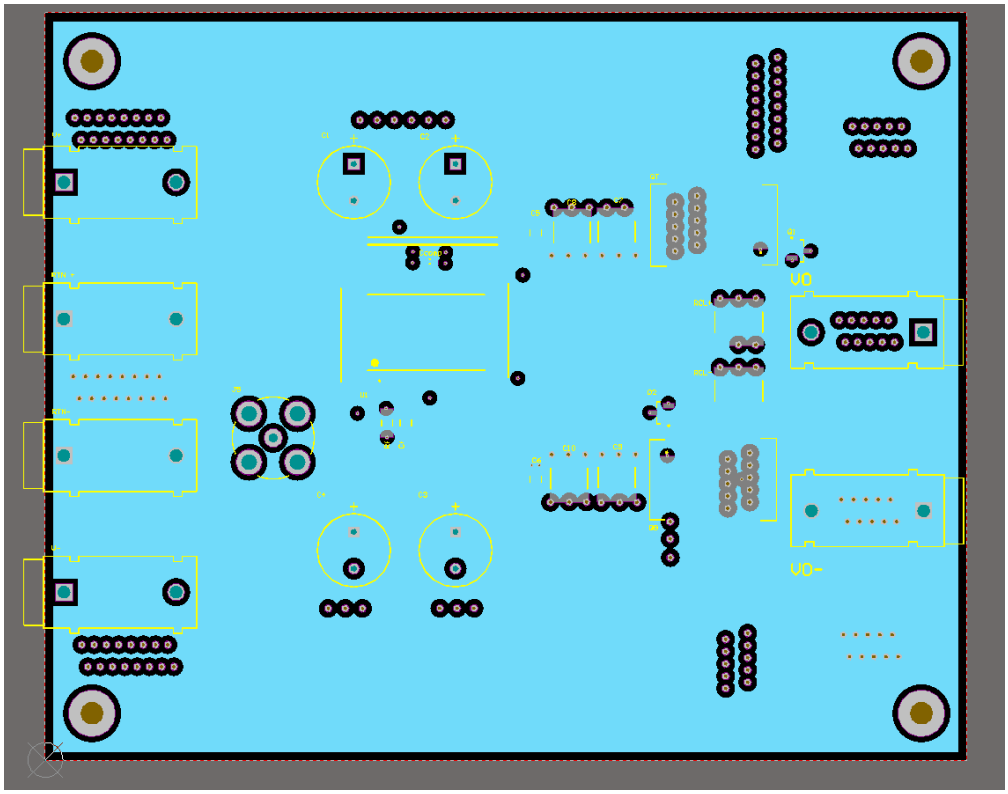
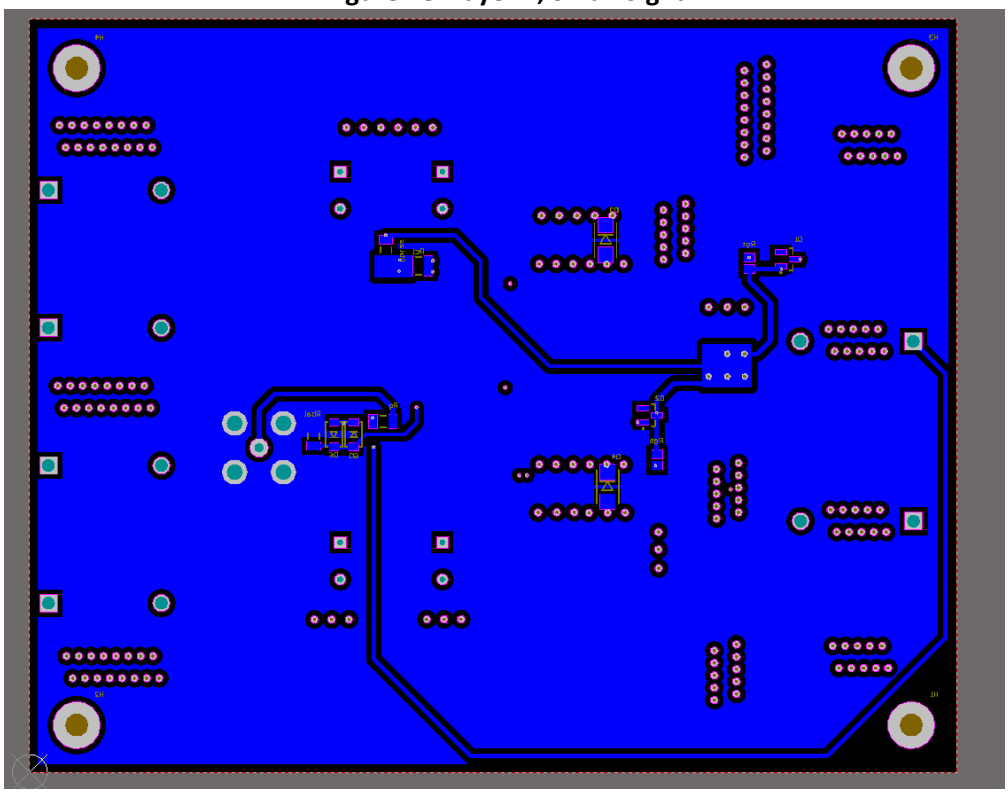


Figure 18: Layer 4, Small Signal



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