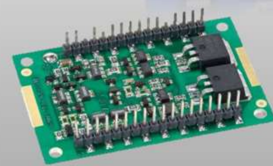
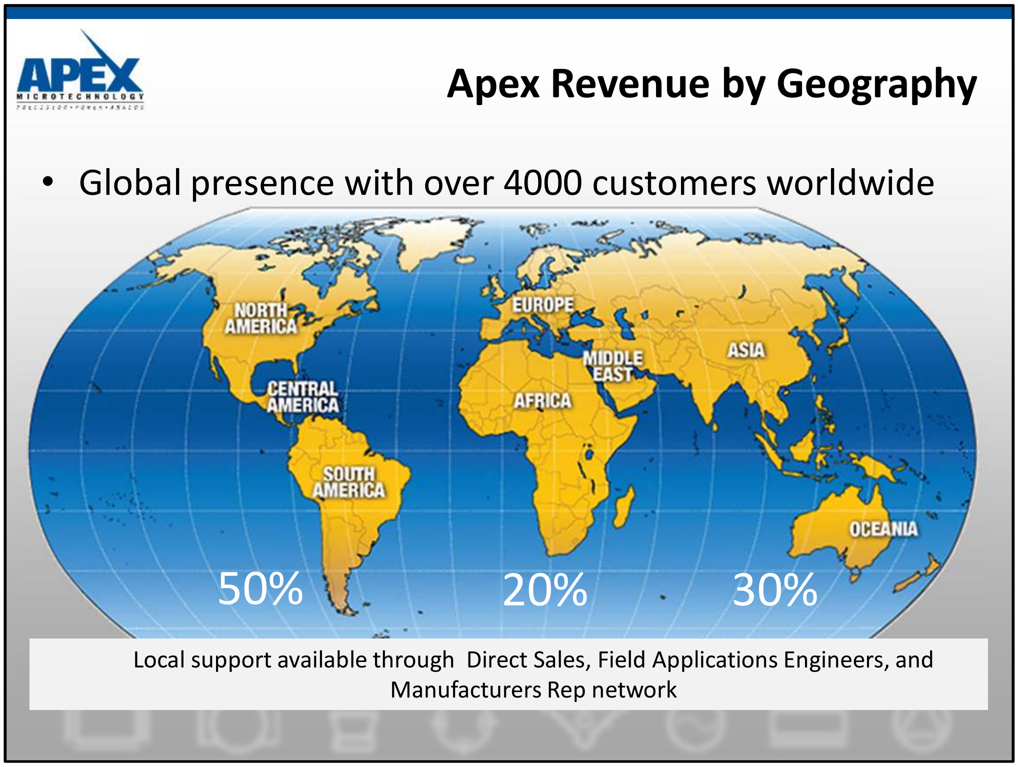
Welcome to Apex Microtechnology. An industry leader in the power analog design of high voltage, high current and high speed power operational amplifiers and pulse width module (PWM) amplifiers. If you have ever needed an operational amplifier that was outside of main stream requirements, then you quite likely have already came across the Apex brand.

While Apex is recognized for excellence in precision power analog products for more than 30 years, we are not content to rest on our laurels. The introduction of new products and new technology concepts continues on course…as you would expect from a company that was founded and continues to grow through innovation.

- **Company Introduction**
- **Market Positioning**
- **Product Offerings**
- **Apex's Value Added**

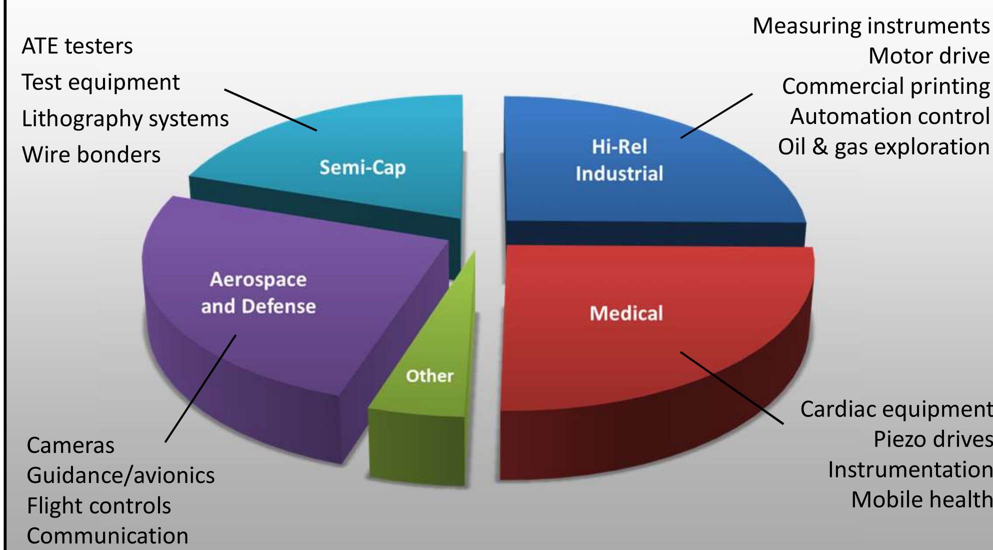


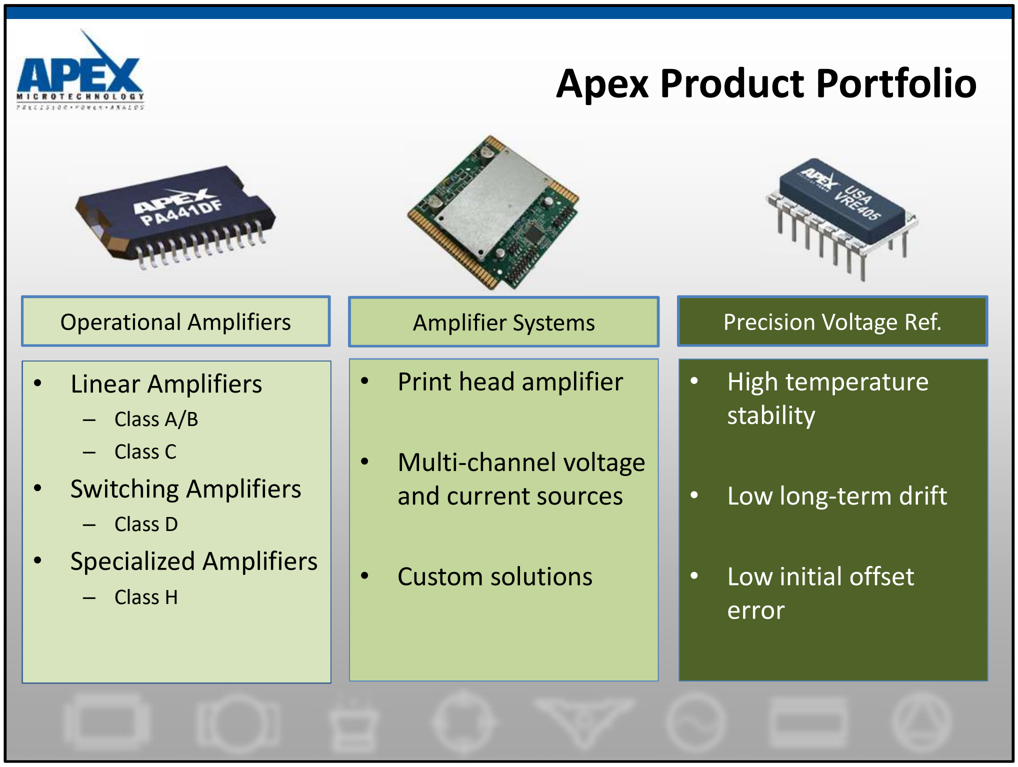
To give you an overview on what we do, we will
- Start with a company introduction,
- Show examples of the markets we serve,
- Give a high level overview on the products we offer
- And discuss the value added resources we can provide



- Apex is well known around the global, servicing more than 3,200 customers world-wide
- Regional sales and engineering support and regional distribution centers ensures timely response to customer questions.

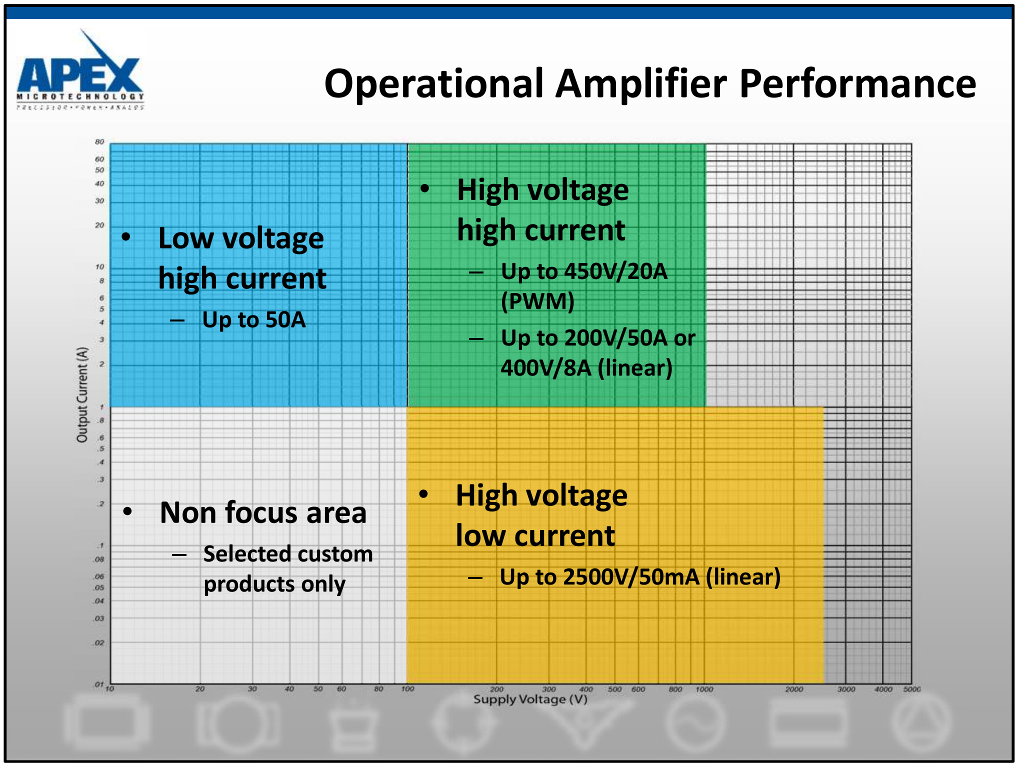
Well Balanced Market Position





Apex is focusing on 3 products categories:

- Power operational amplifiers. Those are amplifiers that operate at high voltage, high current or high speed.
- Amplifier systems combine power operational amplifiers with digital content, providing high feature content on a small footprint.
- Apex's precision voltage references provide best in class performance in terms of temperature drift and long-term stability



Let's look at Apex's power operational amplifiers first:

- Apex solutions support up to 2,500V supply voltage and 50A peak output current
- Besides current and voltage, Apex also offers high speed amplifiers, with slew rates up to 3,000V/µs
- Support for low-voltage and low output current products is limited, as this area is well served by other semiconductor companies.

Select High Performance Products

- High current linear amplifiers

Device	Output Current (A)	Supply Voltage (V)	Slew Rate (V/µs)
MP111FD	50 Peak	100	130
PA50	40	100	50
PA52	40	200	50
PA03	30 Peak	150	8
PA05	30	100	100
PA04	20 Peak	200	50
PA12A	15 Peak	100	4
PA13A	15	100	4
MP104FC	15 Peak x2	200	167
…			

- High current PWM amplifiers

Device	Output Current (A)	Supply Voltage (V)	Frequency (kHz)
SA03	30	100	23
SA01	20	100	48.7
MSA260KC	30 Peak	450	50
SA12	15	200	204
SA160DPA	20 Peak	80	45
…			

- High speed linear amplifiers

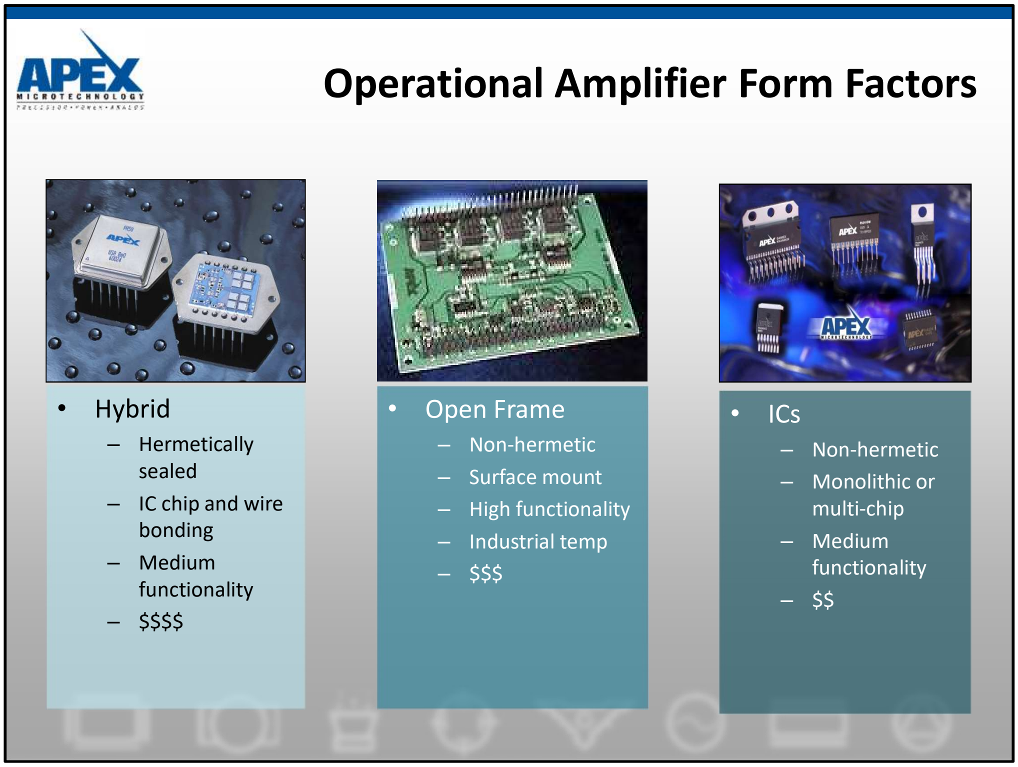
Device	Slew Rate (V/µs)	Supply Voltage (V)	Output Current (A)
PA107DP	3000	200	5
PA98	1000	450	0.2
PA85	1000	450	0.2
PB63DP	1000	200	2
PA119CE	900	80	5
PA94	700	900	0.1
PA79DK	350	350	0.15
PA78DK	350	350	0.15
MP400FC	350	50	0.15
…			

- High voltage linear amplifiers

Device	Supply Voltage (V)	Output Current (A)	Slew Rate (V/µs)
PA99	2500	0.05	25
PA89	1200	0.075	16
PA94	900	0.1	700
PA95	900	0.1	30
PA97	900	0.01	8
PA15	450	0.2	20
…			

More devices can be found in the Product Summary Guide (www.apexanalog.com)

A limited selection of high performance products is shown on this slide. The product summary guide, available from the Apex web site, provides a good overview on all currently available products sorted by various categories.



Now that you know more about what we do, let's show you how we do it. We mentioned that we offer power amplifiers and precision voltage references. Let's look at the power amplifiers first. These come in different flavors, ranging from hybrid designs to power ICs that are based on monolithic solutions.

- Hybrid devices are small circuits that are mounted within a single package. From the outside there is no distinction between a hybrid device and a monolithic device, except that that package might be larger. Package options include hermetically sealed metal packages or plastic SIP packages.
- Power ICs are monolithic circuits that are mounted in plastic packages
- Open Frames are small circuits that are surface mounted on an insulated aluminum frame.

Hybrid packages are typically the most robust packages available. They are also the most complicated and most costly devices, as the limited space demands the use of bare die assembly techniques and special production technologies.
Open frames provide the best flexibility and the shortest development time, They offer high functionality as do the hybrid packages but operate within industrial temp ranges.
Power ICs are what is most commonly used in the semiconductor industry. However, there are limits in terms on functionality and device parameters

Power Operational Amplifiers - Hybrids

12-pin Power DIP

8-pin TO-3

8-pin Power SIP

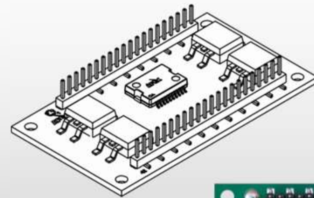
10-pin Power SIP

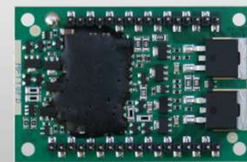
- Features
  - Up to 8kW (DC) power output
  - Up to 2500V supply voltage
  - Up to 50A (continuous) output current
  - Packages that are hermetically sealed
  - Packages that are cavity silicon sealed with nickel plated steel heat tab
  - Standard products with hermetically sealed packages for -55°C to +125°C

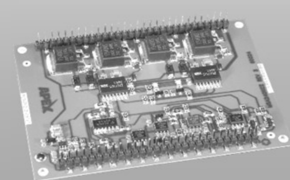
Apex's hybrid amplifier products provide leading edge characteristics, either in terms of power output, supply voltage or speed. They are used in the most demanding of applications. The option of a hermetically sealed package allows the use of the devices in applications where high reliability and robust performance are key design considerations.

Power Operational Amplifiers – Open Frame

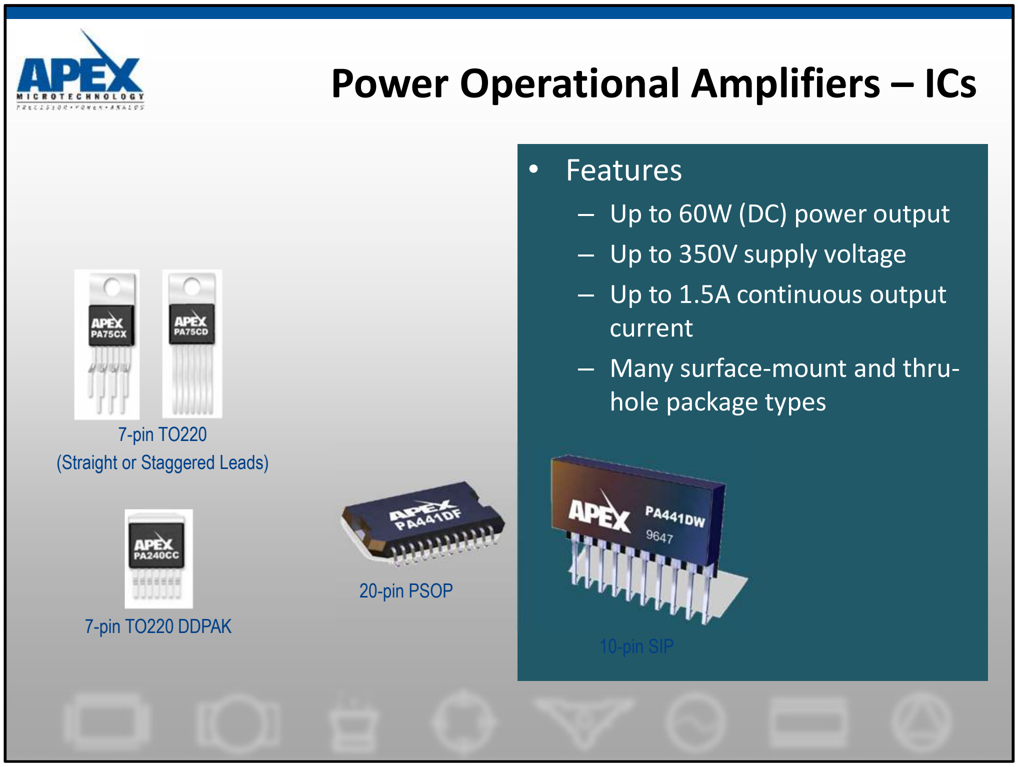
- Features
  - Up to 450V/20A (PWM) or 200V/15A (linear)
  - Digital and analog front ends
    - A/D and D/A converter
  - Advanced protection features
    - Shutdown function
    - Temperature monitors
  - Custom functionality
  - Industrial temperature range
  - Excellent heat dissipation through metal back-plate







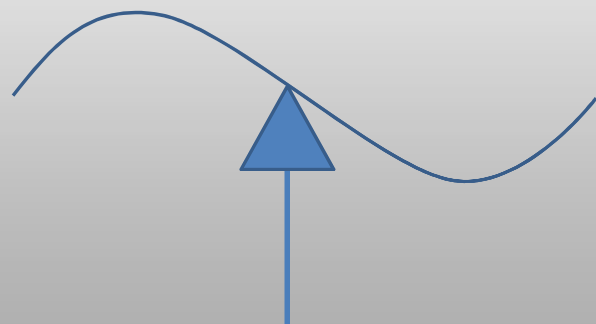
Open frame products offer the ability to add digital and custom content on a platform that provides excellent heat dissipation capabilities.



Power ICs are the lowest cost product options, but are limited in terms of output current and supply voltage. However, we still talk leading edge technology here, as there are only a few suppliers that provide amplifiers that can operate in the 350V range. Packaging varies from very small PSOP and TO-220 packages, to the SIP packages that are also used to house some of the hybrid amplifiers Apex sells.

Precision Voltage References

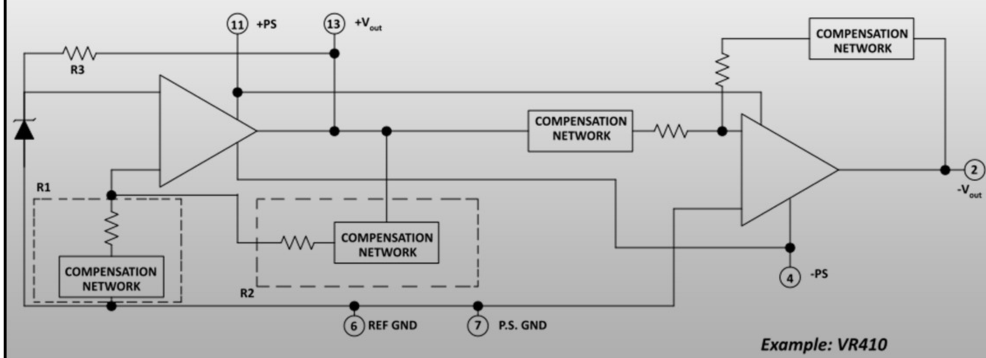
- Best-in-class performance for initial error, temperature drift, thermal hysteresis and noise performance



The other major product family offered by Apex are the industry's best-in-class precision voltage references (VREs). While there is a wealth of voltage references available as monolithic designs, the Apex product line are typically selected when initial error, temperature drift and long-term stability are critical design requirements.

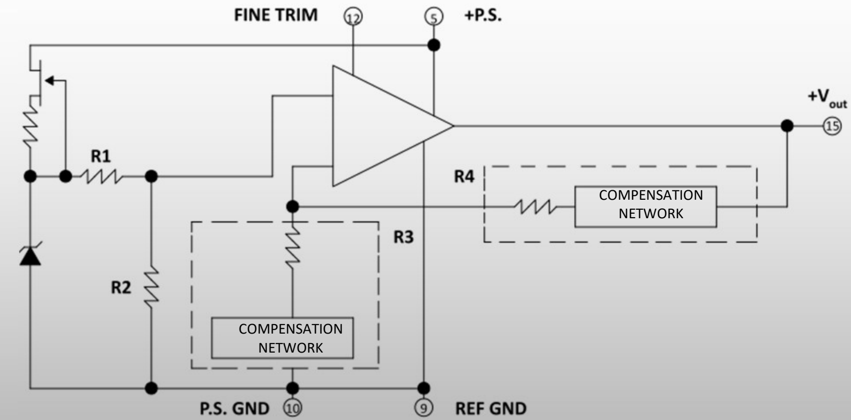
Precision through Compensation

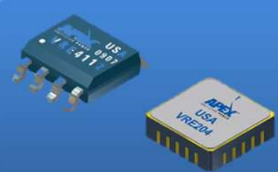
- Multi-stage compensation networks deliver superior voltage precision over temperature and low noise



This best-in-class performance is the result of very labor intensive production. Various compensation networks that need to go through an iterative trimming process ensure that the resulting reference output meets and exceeds the device specifications. Voltage reference are available as single or dual output. The VRE410, shown in this example, offers +10V and -10V output within a single 14-pin package.

Precision Voltage References





Best In Class

Initial Error
Temperature Drift
Thermal Hysteresis
Noise Performance

Precision Voltage References

- 25 precision voltage references
  - Zener based with 3rd-order compensation voltage references
    - Functionally equivalent to 3-terminal regulator
  - Total error over – 25 / +85C as low as 0.5 PPM / C
  - Several supply voltage and reference output options
    - 1.25V, 2.5V, 3V, 4.5V, 5V, 6V, and 10V References
  - Very unique feature set
    - Positive/Negative and dual outputs available

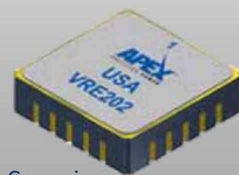
Not Self-Heating!

- Precision Reference Target Applications
  - Precision A/D and D/A converters
  - Transducer excitation
  - Accurate comparator threshold reference
  - High resolution servo systems
  - Digital voltmeters
  - High-precision test and measurement instruments
  - High-precision ATE system and instrument calibration modules

VRE 100/200 Product Families

- Highest Performance References Available Anywhere
  - Initial Error: .005%
  - Noise: 0.3ppm (0.1-10Hz)
  - Temperature Coefficient: 0.5ppm/ºC
- Hi Reliability Construction
  - MIL Temp Range
  - 100% Burn-In
  - Ceramic Packages

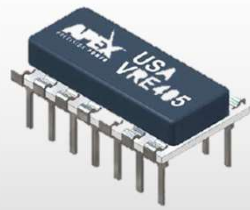
Hermetic 14-pin
Ceramic DIP



20-pin Ceramic
LLC

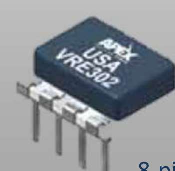
VRE 300/400 Product Families

- High Performance Industrial References
  - Initial Error: .01%
  - Noise: 0.3ppm (0.1-10Hz)
  - Temperature Coefficient: 0.6ppm/ ºC
- Graded Performance
  - Plastic DIP and SMT packages
  - Commercial (0/70C) and Industrial (-25/85C) Temp Range



14-pin DIP

8-pin Surface Mount



8-pin P

14-pin Surface Mount

Voltage Reference Product Overview

MODEL	Output (V)	Initial Error (mV)	Temp Coefficient (ppm/°C)	Noise (µVpp)	Features
VRE102	±10	1.0, 1.2, 1.5, 1.7	1.09, 1.11, 1.33, 1.45	6	High Rel Military
VRE104	4.5	0.8, 0.9	1.48, 1.62, 1.70, 1.98	3	High Rel Military
VRE107M	±5	0.8, 0.9	1.33, 1.56	3	High Rel Military
VRE204M	4.5	0.8, 0.9	1.48, 1.70	3	Small Pkg, High Rel Military
VRE205	5	0.8 , 0.9	1.33, 1.45, 1.56, 1.82	3	Small Pkg, High Rel Military
VRE210	10	0.5, 0.7, 0.8, 1.0	1.09, 1.11, 1.33, 1.45	6	Small Pkg, High Rel Military
VRE302	2.5	0.4, 0.6	1.0, 2.2	1.5	Low Cost
VRE304	4.5	0.45, 0.9	0.6, 2.0	3	Low Cost
VRE305	5	0.5, 0.8, 1.0	0.6, 1.0, 2.0	3	Low Cost
VRE306	6	0.6, 1.2	0.6, 2.0	4	Low Cost
VRE310	10	1.0, 1.6, 2.0	0.6, 1.0, 2.0	6	Low Cost
VRE410	±10	1.6, 2.0, 2.2	1.0, 2.0, 2.2	6	Dual, Low Cost
VRE3025	2.5	0.25, 0.375, 0.5	0.6, 1.0, 2.0	1.5	+10 V Supply
VRE3050	5	0.5, 0.8, 1.0	0.6, 1.0, 2.0	3	+10 V Supply
VRE3041	4.096	2.0	1.0	3	Low Drift
SWR200	7.071 RMS	0.5%	20	0.05% THD	Sine wave reference

The table shows the available precision voltages and the grade choices for initial error and temperature coefficient.

Apex Quality

ISO 9001 REGISTRATION

This is to certify that the Quality Management System meets ISO 9001 (2008). Registration is hereby awarded to

Apex Microtechnology, Inc.
5980 North Shannon Road
Tucson, AZ 85741

FOR: The design, development, production, and test of hybrid microcircuits at the Tucson, Arizona facility.

THIS REGISTRATION IS VALID UNTIL TERMINATED BY WRITTEN NOTIFICATION FROM DLA LAND AND MARITIME. REFERENCE DLA LAND AND MARITIME LETTER VQ(VQH-15-029212) FOR DETAILS.

Certificate Number: VQ-223
Issue Date: April 29, 2015
Telephone Number: 614-692-0582

Todd Lewis
Director, Engineering and Technical Support Directorate
DLA Land and Maritime

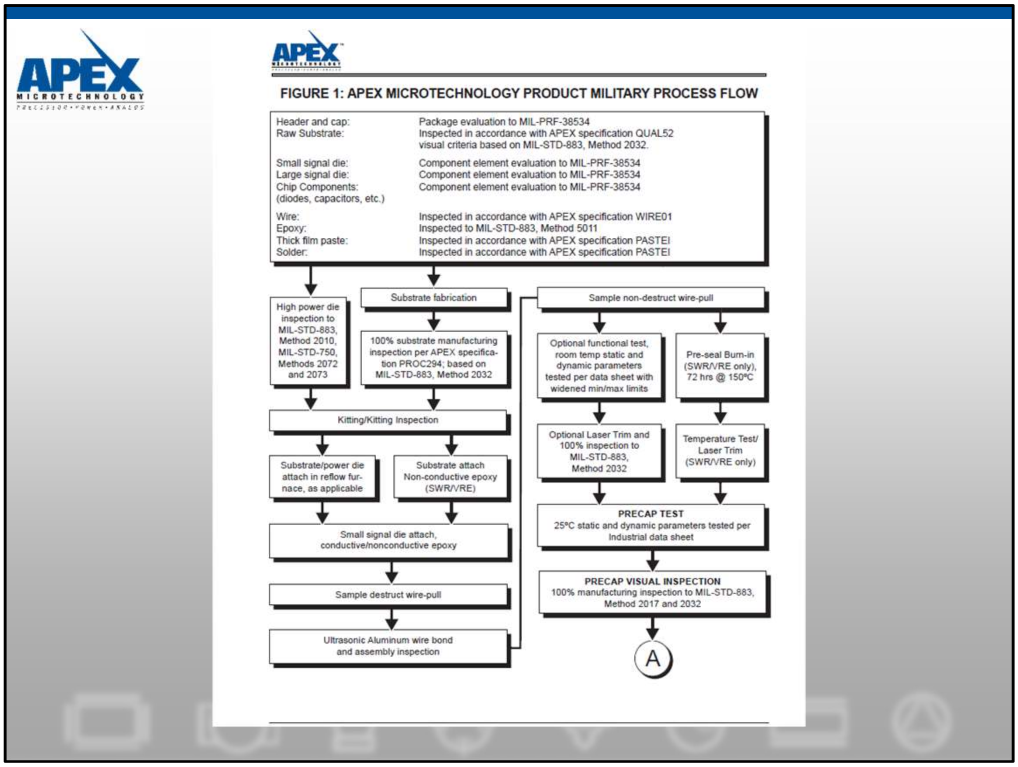
MIL-PRF-38534

HYBRID MICROCIRCUIT CERTIFICATION
FOR
CLASS H
IS HEREBY AWARDED TO

APEX MICROTECHNOLOGY
5980 North Shannon Road
Tucson, Arizona 85741-5230

THIS CERTIFICATION IS VALID UNTIL TERMINATED BY WRITTEN NOTIFICATION FROM DLA LAND AND MARITIME. REFERENCE DLA LAND AND MARITIME LETTER VQ(VQH-15-029211) FOR DETAILS PERTAINING TO THIS CERTIFICATION.

Todd Lewis
Director, Engineering and Technical Support Directorate
DLA Land and Maritime


APEX MICROTECHNOLOGY
FIGURE 1: APEX MICROTECHNOLOGY PRODUCT MILITARY PROCESS FLOW
Header and cap: Package evaluation to MIL-PRF-38534
Raw Substrate: Inspected in accordance with APEX specification QUAL52 visual criteria based on MIL-STD-883, Method 2032.
Small signal die: Component element evaluation to MIL-PRF-38534
Large signal die: Component element evaluation to MIL-PRF-38534
Chip Components: (diodes, capacitors, etc.) Component element evaluation to MIL-PRF-38534
Wire: Inspected in accordance with APEX specification WIRE01
Epoxy: Inspected to MIL-STD-883, Method 5011
Thick film paste: Inspected in accordance with APEX specification PASTEI
Solder: Inspected in accordance with APEX specification PASTEI
High power die inspection to MIL-STD-883, Method 2010, MIL-STD-750, Methods 2072 and 2073
Substrate fabrication
100% substrate manufacturing inspection per APEX specification PROC294; based on MIL-STD-883, Method 2032
Kitting/Kitting Inspection
Substrate/power die attach in reflow furnace, as applicable
Substrate attach Non-conductive epoxy (SWR/VRE)
Small signal die attach, conductive/nonconductive epoxy
Sample destruct wire-pull
Ultrasonic Aluminum wire bond and assembly inspection
Sample non-destruct wire-pull
Optional functional test, room temp static and dynamic parameters tested per data sheet with widened min/max limits
Pre-seal Burn-in (SWR/VRE only), 72 hrs @ 150ºC
Optional Laser Trim and 100% inspection to MIL-STD-883, Method 2032
Temperature Test/ Laser Trim (SWR/VRE only)
PRECAP TEST
25ºC static and dynamic parameters tested per Industrial data sheet
PRECAP VISUAL INSPECTION
100% manufacturing inspection to MIL-STD-883, Method 2017 and 2032
A

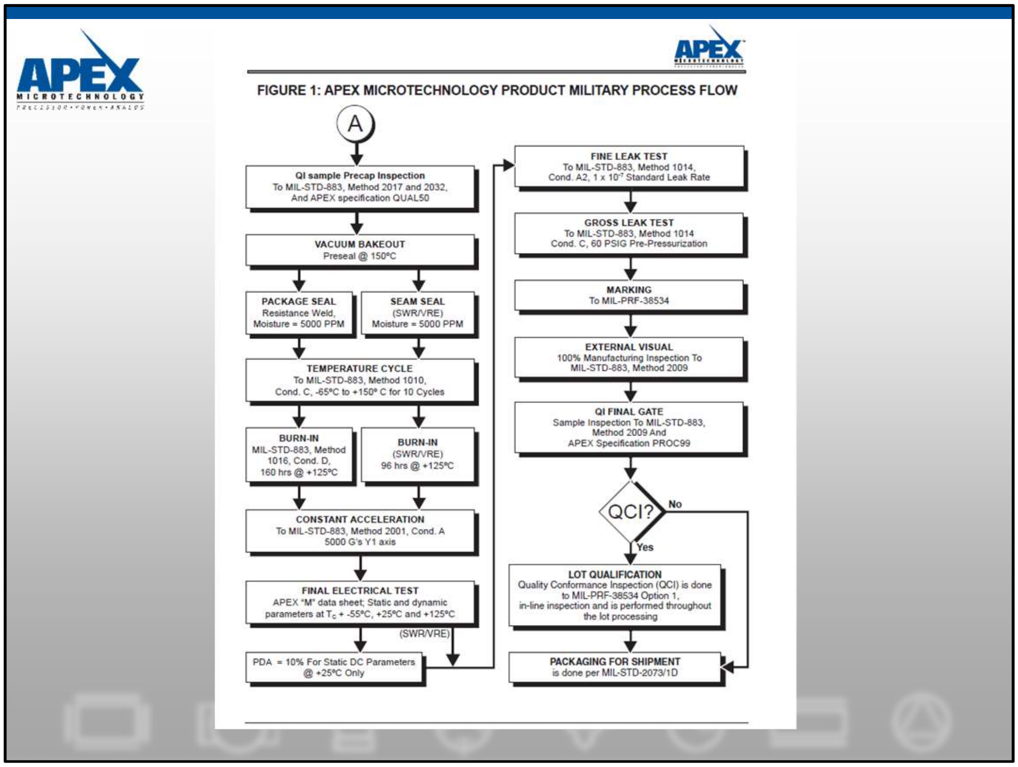
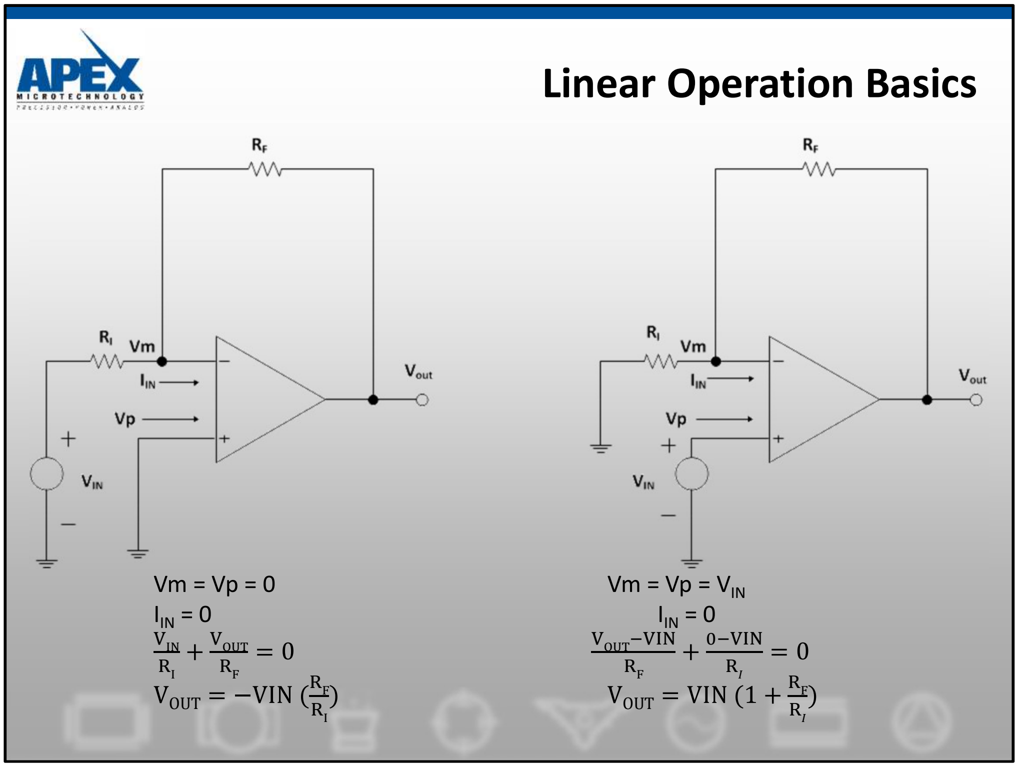


FIGURE 1: APEX MICROTECHNOLOGY PRODUCT MILITARY PROCESS FLOW
A
QI sample Precap Inspection
To MIL-STD-883, Method 2017 and 2032,
And APEX specification QUAL50
VACUUM BAKEOUT
Preseal @ 150°C
PACKAGE SEAL
Resistance Weld,
Moisture = 5000 PPM
SEAM SEAL
(SWR/VRE)
Moisture = 5000 PPM
TEMPERATURE CYCLE
To MIL-STD-883, Method 1010,
Cond. C, -65°C to +150° C for 10 Cycles
BURN-IN
MIL-STD-883, Method
1016, Cond. D,
160 hrs @ +125°C
BURN-IN
(SWR/VRE)
96 hrs @ +125°C
CONSTANT ACCELERATION
To MIL-STD-883, Method 2001, Cond. A
5000 G's Y1 axis
FINAL ELECTRICAL TEST
APEX "M" data sheet; Static and dynamic
parameters at T_C + -55°C, +25°C and +125°C
(SWR/VRE)
PDA = 10% For Static DC Parameters
@ +25°C Only
FINE LEAK TEST
To MIL-STD-883, Method 1014,
Cond. A2, 1 x 10^{-7} Standard Leak Rate
GROSS LEAK TEST
To MIL-STD-883, Method 1014
Cond. C, 60 PSIG Pre-Pressurization
MARKING
To MIL-PRF-38534
EXTERNAL VISUAL
100% Manufacturing Inspection To
MIL-STD-883, Method 2009
QI FINAL GATE
Sample Inspection To MIL-STD-883,
Method 2009 And
APEX Specification PROC99
QCI?
No
Yes
LOT QUALIFICATION
Quality Conformance Inspection (QCI) is done
to MIL-PRF-38534 Option 1,
in-line inspection and is performed throughout
the lot processing
PACKAGING FOR SHIPMENT
is done per MIL-STD-2073/1D

Seminar Topics

OP AMPS

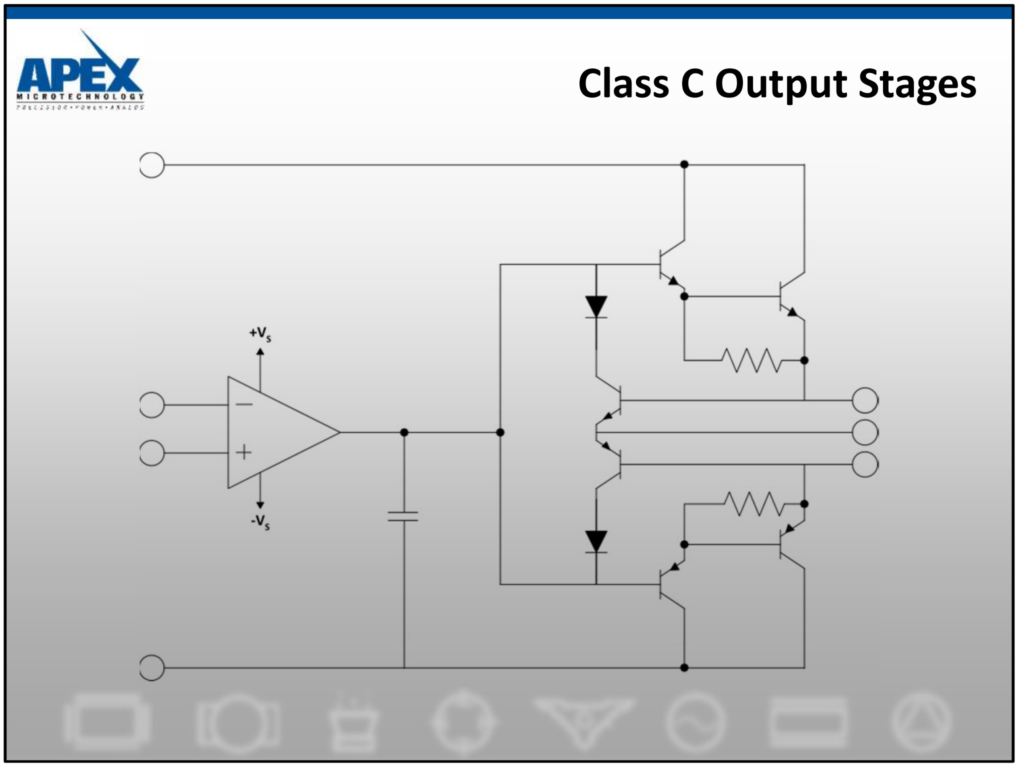


Three most important characteristics of an ideal op amp are: 1) infinite input impedance
2) zero output impedance
3) infinite open loop gain

Let's review the inverting configuration in light of these three basic characteristics. #1 dictates that the input current into the op amp is 0. #3 implies that any voltage appearing between the input terminals will result in infinite output voltage. The resistive divider action of Rf and Ri causes a portion of the output voltage to be fed back to the inverting input. It is this NEGATIVE FEEDBACK action coupled with #3, open loop gain, that keeps the voltage between the two inputs at zero.

In the inverting configuration, this results in a "virtual ground" node. The concept of a virtual ground, coupled with the zero input current flow, allows the "closed loop gain" or transfer function of the circuit to be easily calculated. Current flow in Ri is equal to Vin/Ri. The same current is forced to flow through Rf, giving an output voltage of -IinRf.

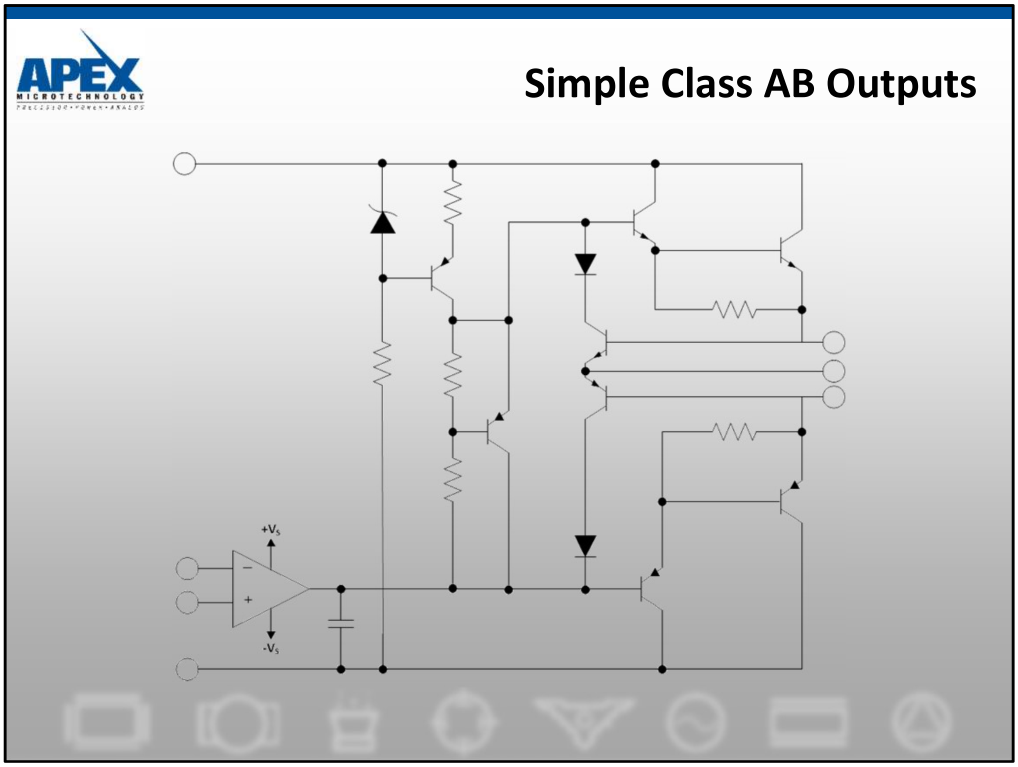
In the non-inverting amplifier, the infinite open loop gain of the amplifier, coupled with negative feedback, force the inverting terminal to be equal to the non-inverting terminal. This sets up a voltage across Ri which develops a current that also flows through Rf. Therefore, the total output voltage is s Vin/Rin current times the series combination of Rf and Ri.



Class “C” output stages tie the bases or gates of the power devices together. Omitting the usual bias network between these bases reduces cost with the penalty of increased crossover distortion.

Assuming a resistive load and the drive stage voltage in the range of ±0.6V. There is no output current because the power devices need about a Vbe to turn on. There is a dead band of about 1.2V which the driver must cross over before output current can change polarity. For MOSFET outputs this dead band is usually somewhere between 4 to 6V.

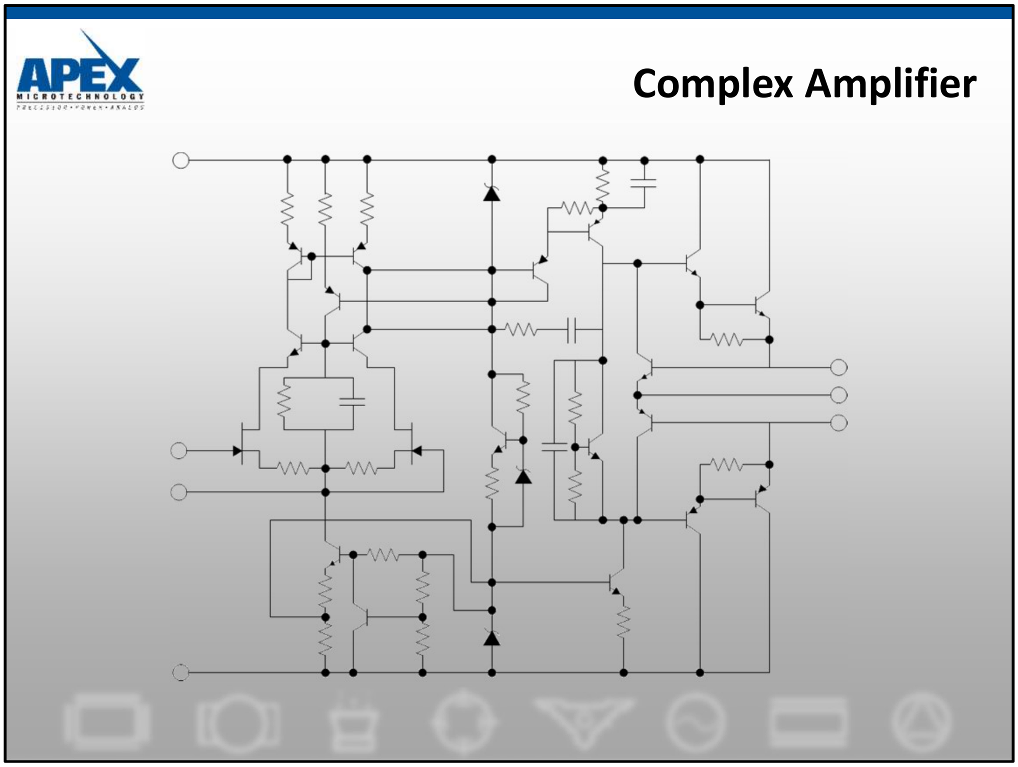
The good news is that because the output does not move, there is no feedback to the driver. It is running open loop during dead band transition and slews across as fast as it can. This means at low frequencies this distortion is quite low. Class “C” outputs are generally not recommended above 1KHz but this varies with tolerance of distortion.



The class “AB” output keeps some current flowing in the output transistors at all times to minimize crossover distortion. This area is still the largest contributor to total harmonic distortion but the “dead” band is gone.

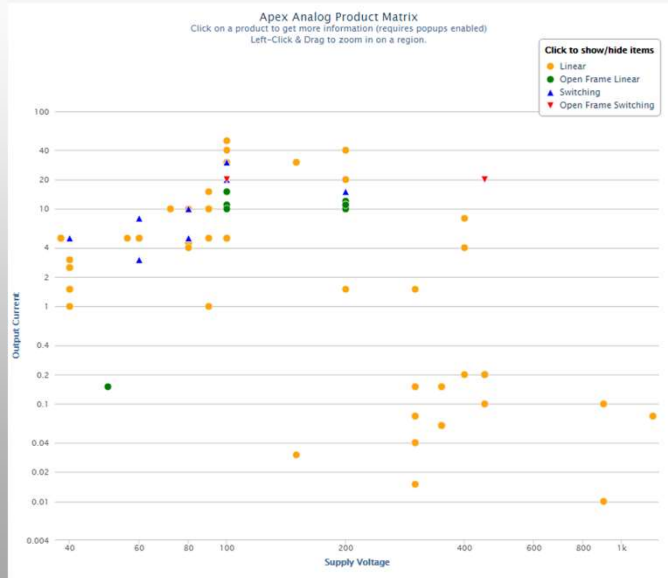
The circuit is known as a Vbe or Vgs multiplier. Think of this transistor as a noninverting op amp with the Vbe (Vgs) as an input and two about equal input and feedback resistors. If the multiplier transistor and the output transistors are tightly thermally coupled, distortion can be kept low and the possibility of thermal runaway is eliminated. This is one area where the hybrid really shines over a discrete circuit because these transistors are physically and thermally close to each. Many Apex amplifiers also use thermistors to compensate for tracking differences due to the transistors being different types. Imagine the tracking differences when the multiplier and power transistors are in separate packages.

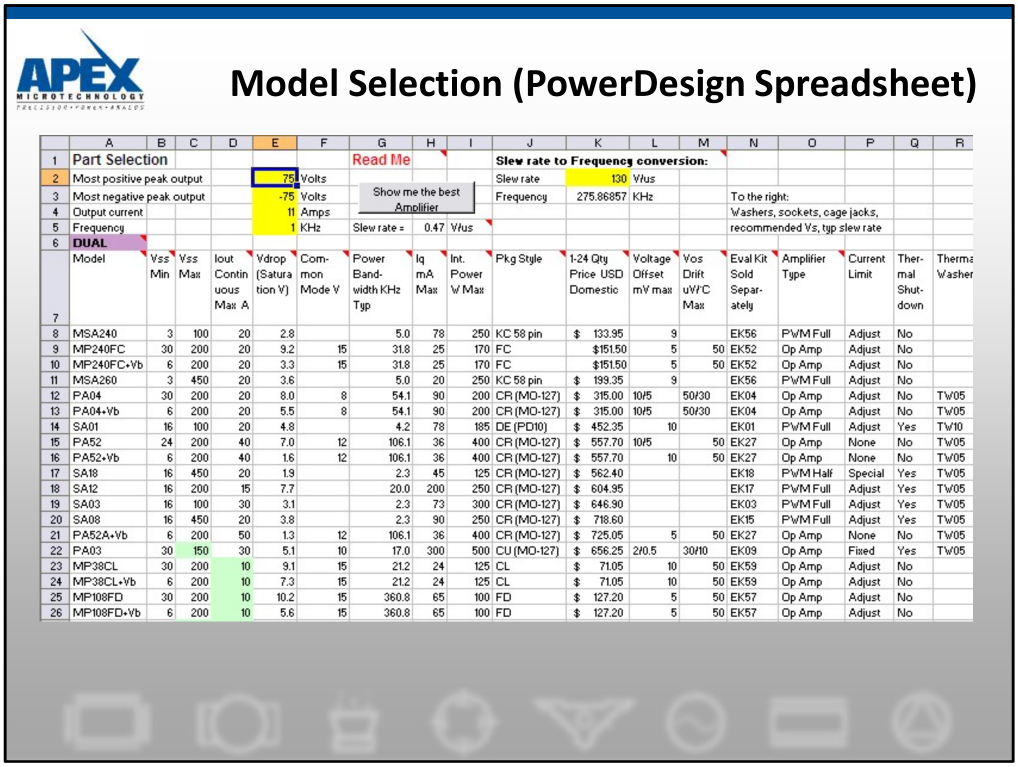
We refer to this as a simple amplifier because of the monolithic driver stage which may incorporate 50 to 100 transistors on a single chip.



Here is the most difficult and costly way to build a power op amp. Monolithic driver candidates are often lacking in performance above ±15V and above ±40V the picture is down right discouraging. Being able to select each individual transistor for optimum overall performance of the power op amp results in DC accuracy under 1mV, speeds to 1000V/µs or total supply voltages to 1200V.

Apex Analog Product Matrix





Model Selection (PowerDesign Spreadsheet)

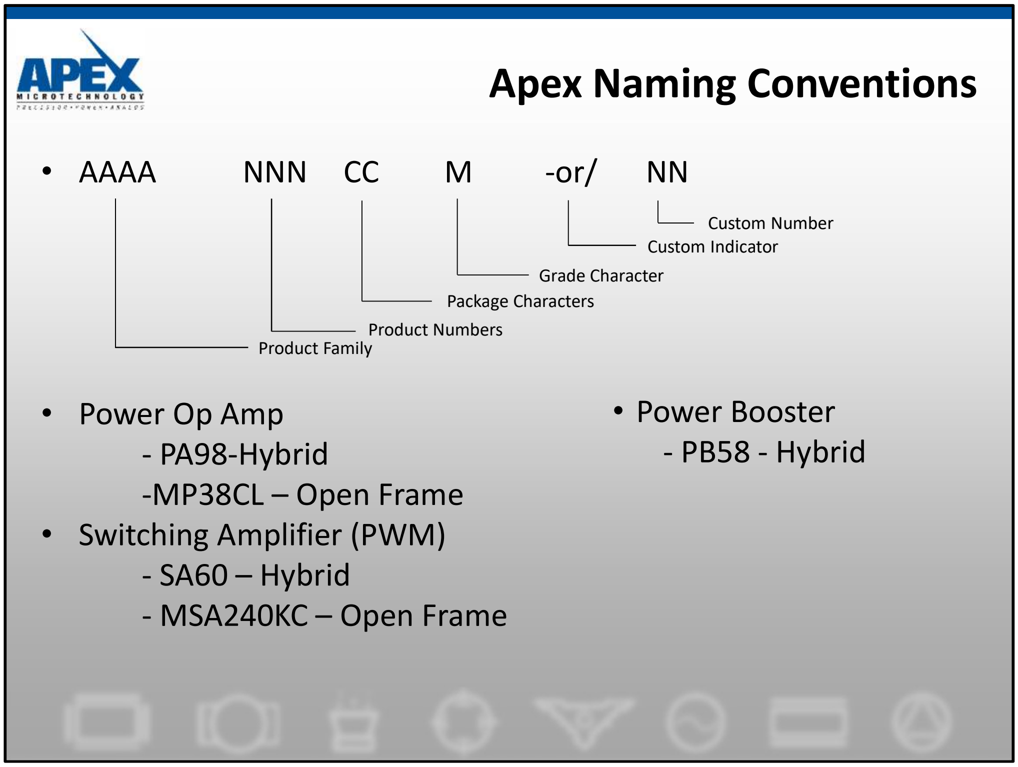
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
1	Part Selection						Read Me			Slew rate to Frequency conversion:								
2	Most positive peak output				75	Volts				Slew rate	130	V/us						
3	Most negative peak output				-75	Volts	Show me the best Amplifier			Frequency	275.86857	KHz		To the right:				
4	Output current				11	Amps								Washers, sockets, cage jacks,				
5	Frequency				1	KHz	Slew rate =	0.47	V/us					recommended Vs, typ slew rate				
6	DUAL																	
7	Model	Vss Min	Vss Max	Iout Continuous Max A	Vdrop (Saturation V)	Common Mode V	Power Bandwidth KHz Typ	Iq mA Max	Int. Power W Max	Pkg Style	1-24 Qty Price USD Domestic	Voltage Offset mV max	Vos Drift uV/°C Max	Eval Kit Sold Separately	Amplifier Type	Current Limit	Thermal Shutdown	Therma Washer
8	MSA240	3	100	20	2.8		5.0	78	250	KC 58 pin	$ 133.95	9		EK56	PWM Full	Adjust	No	
9	MP240FC	30	200	20	9.2	15	31.8	25	170	FC	$151.50	5	50	EK52	Op Amp	Adjust	No	
10	MP240FC+Vb	6	200	20	3.3	15	31.8	25	170	FC	$151.50	5	50	EK52	Op Amp	Adjust	No	
11	MSA260	3	450	20	3.6		5.0	20	250	KC 58 pin	$ 199.35	9		EK56	PWM Full	Adjust	No	
12	PA04	30	200	20	8.0	8	54.1	90	200	CR (MO-127)	$ 315.00	10/5	50/30	EK04	Op Amp	Adjust	No	TW05
13	PA04+Vb	6	200	20	5.5	8	54.1	90	200	CR (MO-127)	$ 315.00	10/5	50/30	EK04	Op Amp	Adjust	No	TW05
14	SA01	16	100	20	4.8		4.2	78	185	DE (PD10)	$ 452.35	10		EK01	PWM Full	Adjust	Yes	TW10
15	PA52	24	200	40	7.0	12	106.1	36	400	CR (MO-127)	$ 557.70	10/5	50	EK27	Op Amp	None	No	TW05
16	PA52+Vb	6	200	40	1.6	12	106.1	36	400	CR (MO-127)	$ 557.70	10	50	EK27	Op Amp	None	No	TW05
17	SA18	16	450	20	1.9		2.3	45	125	CR (MO-127)	$ 562.40			EK18	PWM Half	Special	Yes	TW05
18	SA12	16	200	15	7.7		20.0	200	250	CR (MO-127)	$ 604.95			EK17	PWM Full	Adjust	Yes	TW05
19	SA03	16	100	30	3.1		2.3	73	300	CR (MO-127)	$ 646.90			EK03	PWM Full	Adjust	Yes	TW05
20	SA08	16	450	20	3.8		2.3	90	250	CR (MO-127)	$ 718.60			EK15	PWM Full	Adjust	Yes	TW05
21	PA52A+Vb	6	200	50	1.3	12	106.1	36	400	CR (MO-127)	$ 725.05	5	50	EK27	Op Amp	None	No	TW05
22	PA03	30	150	30	5.1	10	17.0	300	500	CU (MO-127)	$ 656.25	2/0.5	30/10	EK09	Op Amp	Fixed	Yes	TW05
23	MP38CL	30	200	10	9.1	15	21.2	24	125	CL	$ 71.05	10	50	EK59	Op Amp	Adjust	No	
24	MP38CL+Vb	6	200	10	7.3	15	21.2	24	125	CL	$ 71.05	10	50	EK59	Op Amp	Adjust	No	
25	MP108FD	30	200	10	10.2	15	360.8	65	100	FD	$ 127.20	5	50	EK57	Op Amp	Adjust	No	
26	MP108FD+Vb	6	200	10	5.6	15	360.8	65	100	FD	$ 127.20	5	50	EK57	Op Amp	Adjust	No	

Amplifier requirements have been entered into the yellow cells and the command button used to calculate suitability and sort by cost. For each parameter, the suitability ratio is 1 if the product meets (or exceeds) the requirements or is equal to requirement/capability. The sum of the ratios is used to sort the list.

In this example we see both switching and linear solutions meeting all the application requirements spanning more than a 5.5:1 price range. Vss min and max are data sheet specifications while +Vs and -Vs are estimations of supply requirements for this specific application (accounts for Vdrop or Saturation Voltage at the application output current). Note the blank cells where parameters do not apply to PWM amplifiers.

Here we find the MSA240 is the “best” choice. However, the selection process knows nothing about noise tolerance of the application, space and weight limitations for heatsink and filter inductors, duty cycle of the output signal, accuracy requirements, military screening needs or - - - -. This is a good tool, but we still need an engineer to complete the job.

Even though Dilbert would have a fit, we may even find that talking to marketing would be a good idea. Note the last few lines where the output current spec is shaded green because the amplifiers do not meet the application requirements. This indicates we may be able to reduce cost 2:1 if the output current specification could be reduced only 10%!



The overall naming convention for naming new products was adopted in mid- 2002. There will always be at least two alpha and two numeric characters plus two more alpha to define the package. The remaining characters are all optional. The most common grade characters are:

The “A” suffix indicates electrical grade out for improved DC accuracy and sometimes voltage capability, temperature range or speed.

The “M” suffix indicates a part with identical design to the standard but with hi-rel screening added. Various models are offered as non-compliant (Apex verified), /883 (government verified) or SMD (government verified and controls the drawing).

The PA and MP power op amps are indeed operational amplifiers following all the rules for these basic building blocks where in a properly designed circuit, performance is controlled by feedback rather than op amp parameters.

The PB power boosters are a unique cost effective solution providing a programmable gain from 3 to 25 at voltages up to ±150V and up to 2A. They are usually configured as the power stage of a composite amplifier which then acts like a power op amp. With the front end of the composite being a low cost typically ±15V op amp, speed and accuracy are easily tailored to need of the application.

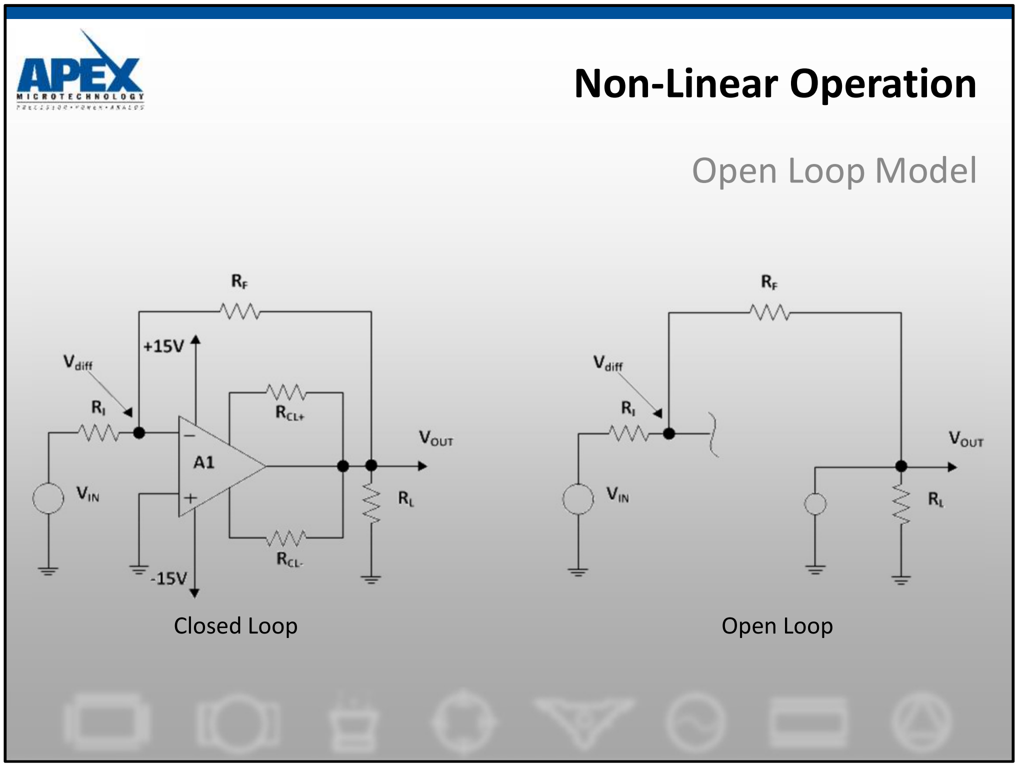
The SA and MSA PWM amplifiers come to the rescue when internal power dissipation gets out of hand with linear devices. They provide one full bridge or one half bridge per package

Electrical Limitation

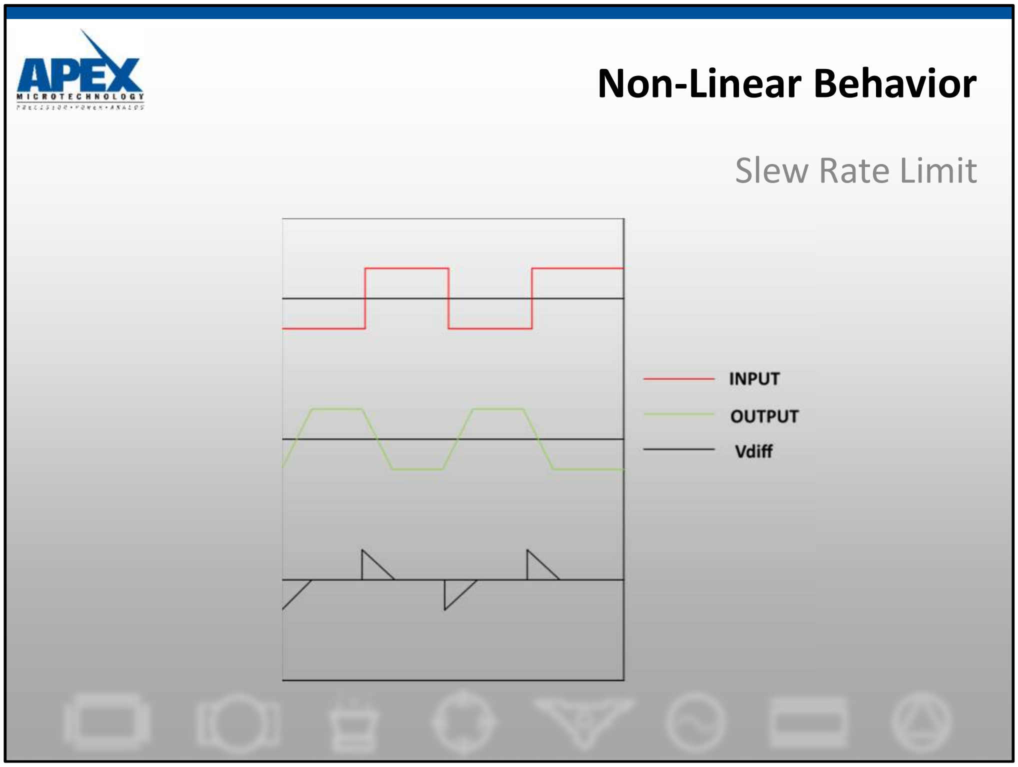
Effects on the Amplifier

- Slew Rate Limiting
- Output Saturation
- Current Limiting
- Shut Down
- Common Mode Requirements

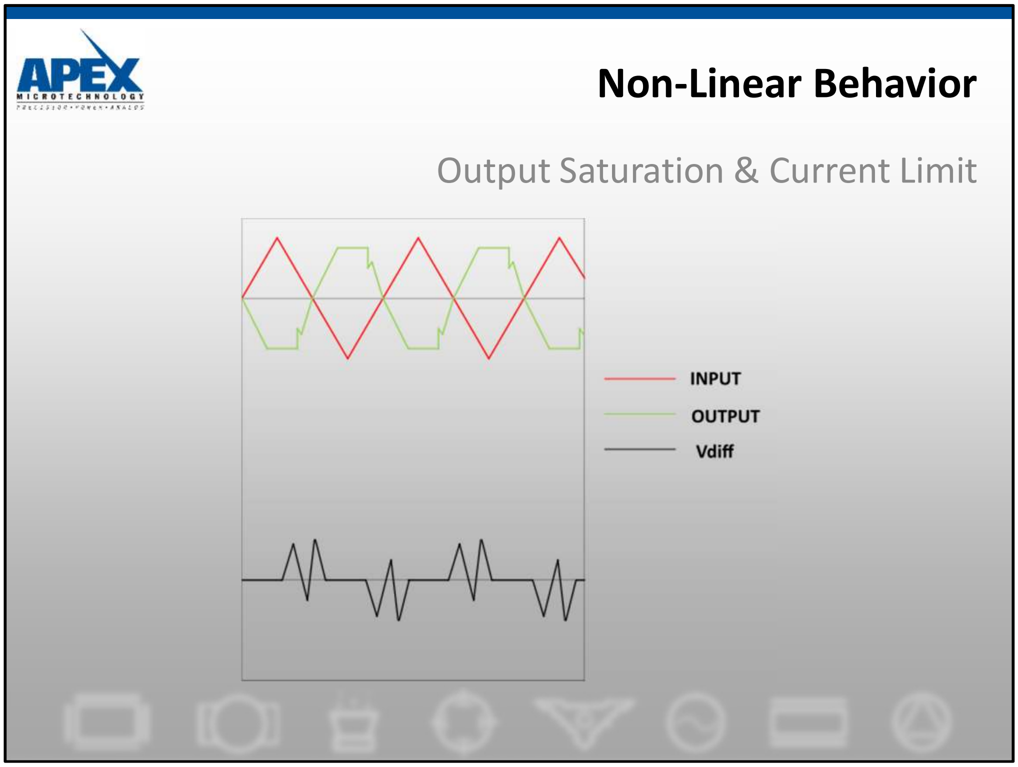
Power amplifiers and small signal op amps share many limitations. Understanding the limitations of a standard op amp will help you design more accurate, reliable circuitry. It helps to have a good understanding of what happens to an amplifier when it operates outside of its linear region. Most of these electric limitations can be traced to this common denominator



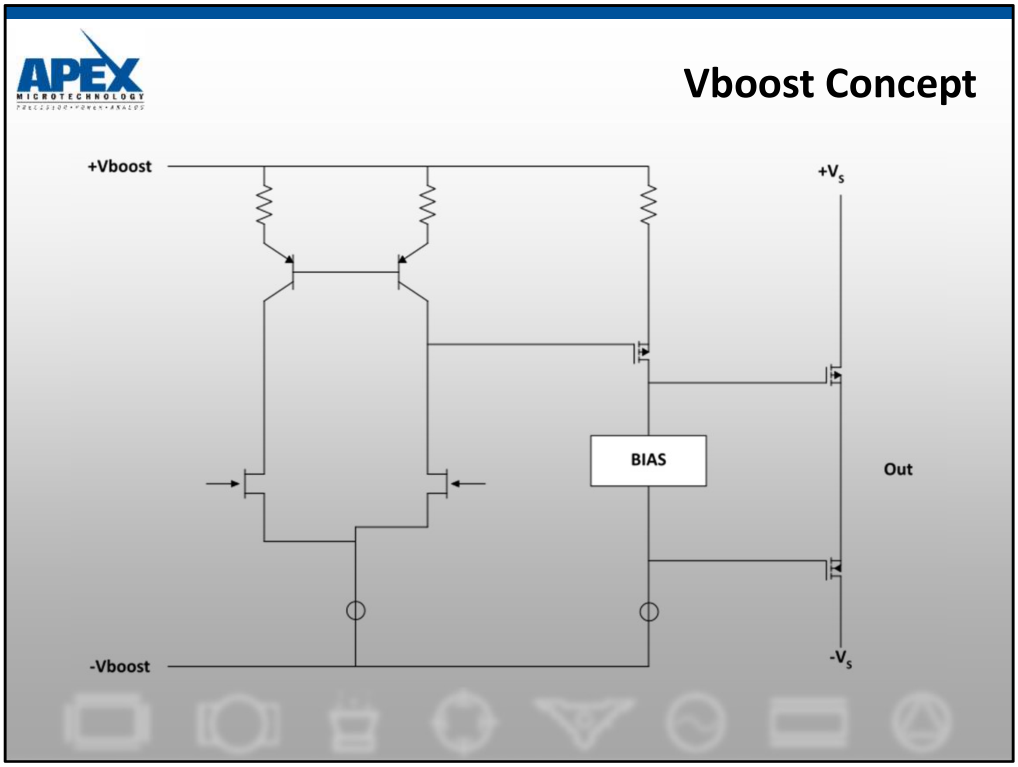
When an amplifier is operated in a closed loop it exhibits linear behavior. A violation of any of the limitations mentioned earlier will effectively open the loop. Once the loop is opened, Vin and Vout appear as two independent voltage sources. Rf and Ri function as a simple voltage divider between the two resistors. This voltage appears as a differential input voltage. In cases where the output stage is in a high impedance state, such as power off or thermal shutdown, Vout goes away and Vin is divided down by the series combination of Rin, Rf and Rload.



The effect of operating the amplifier in the slew limited region can be seen most dramatically by applying a step voltage to the input. Since the output of the amplifier cannot keep up with an infinite dV/dt, it goes into slew limited mode and begins changing its output voltage. At the point the amplifier goes into slew limit, we can use our "disappearing op amp" model to visualize what happens at the inverting input node of A1. In the example above, at t=0+, the input voltage has changed from +10 volts to - 10 volts, but the output voltage has not yet changed from -10 volts. Therefore, -10 volts will be on both sides of the divider comprised of RF and RI. Since there is no voltage difference, the full -10 volts will appear as VDIFF. As the output tries to "catch up", the right side of the divider will be changing linearly to +10 volts, therefore the differential voltage will drop linearly until the output catches up with the input. When the output catches up, the loop is closed and the differential voltage is zero.



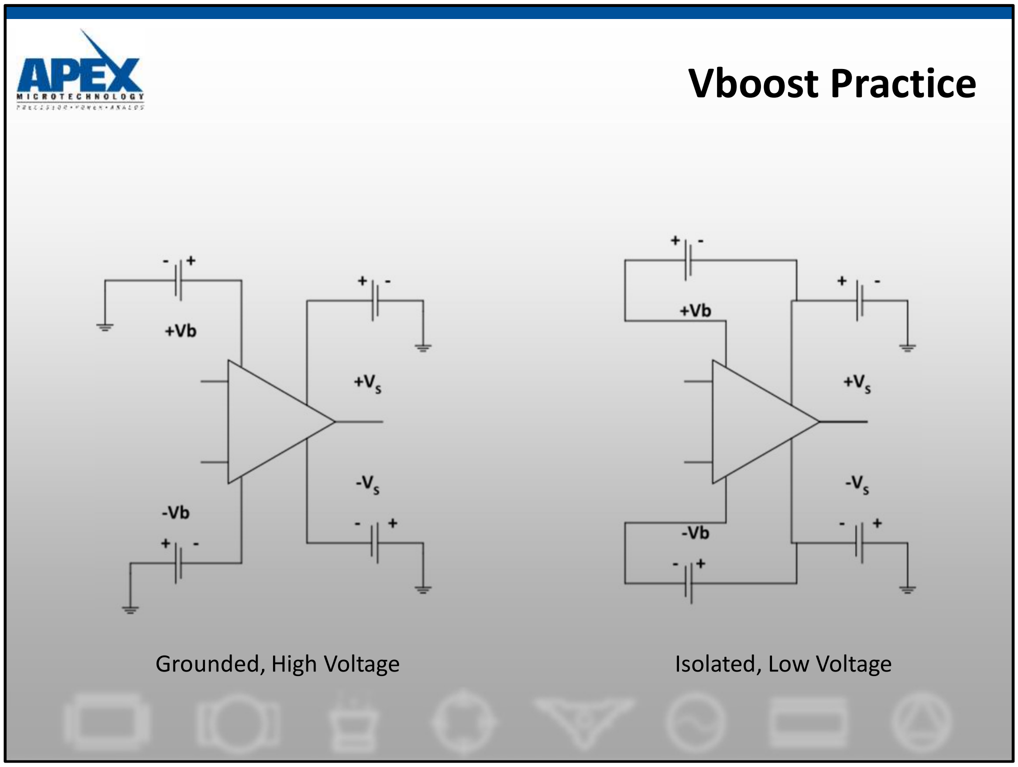
Output saturation and current limit exhibit similar behavior — clipping on the amplifier output. This clipping produces differential input voltages. Any type of clipping can result in an overdriven condition internal to the amplifier. This can lead to recovery problems ranging from simple long recovery to ringing during recovery.



The Vboost concept separates the supplies of the front end, or driver stage, from the supplies of the output stage. When the Vboost supply magnitudes are larger than those of the Vs supplies, the output power MOSFETs can be driven closer to saturation. This allows lower voltages for the high power supply for a given output voltage requirement, thus increasing efficiency and reducing heatsink requirements.

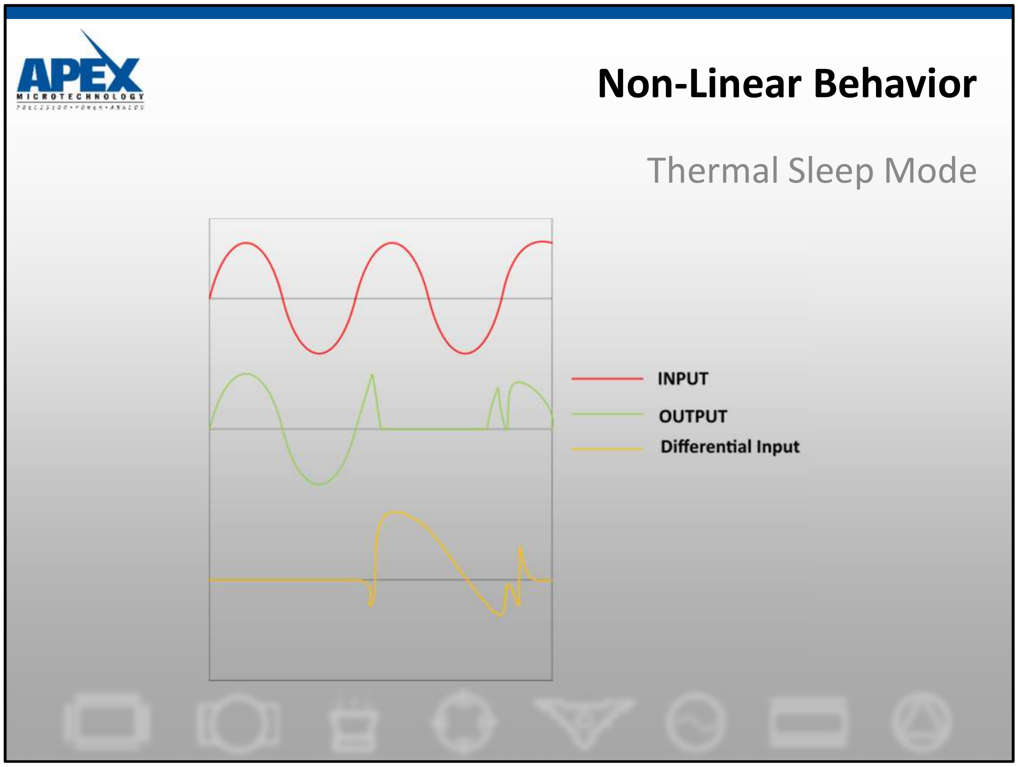
Additionally, the higher Vboost voltages allow a wider range of common mode voltage on the inputs. This can be especially valuable when paralleling amplifiers. While the Vs supplies will be rated for many amperes, it is rare that the Vboost supplies need to be rated over 100mA.

This is especially true of asymmetrical supply circuits with reactive loads - discussed in more detail later in the presentation. Consider a capacitive piezo drive circuit with symmetric slew rates that drives from 0-100V. Traditional asymmetric supplies might be -15 and 115V. In order to charge and discharge the capacitance symmetrically, these supplies need to be rated for the full current. With the Vboost feature, the -15V can be applied to –Vb and -Vs is tied directly to GND, still allowing an output voltage of 0-100V. –Vb need only to be rated for the input stage Iq of the amplifier.

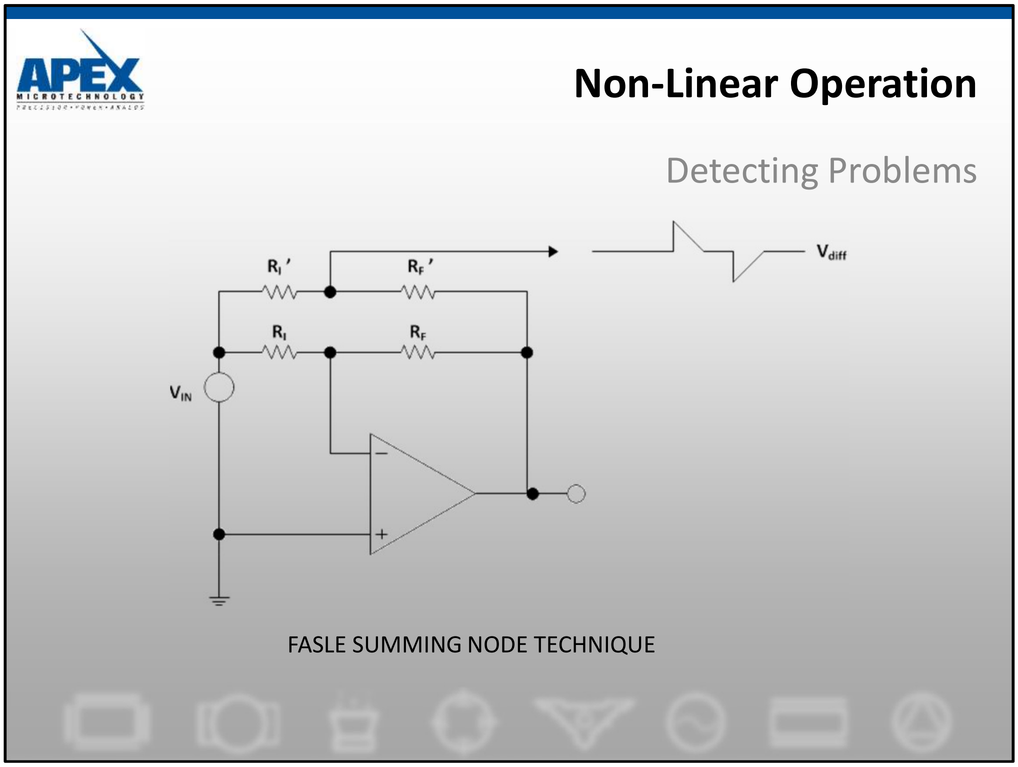


On the left, we see simple ground referenced Vboost supplies which are 5 to 20V larger in magnitude than the Vs supplies. While these supplies do not carry the multiple ampere output currents, they do need to support amplifier quiescent current.

On the right, the Vboost still needs to supply amplifier quiescent current, but with voltage ratings of only 5 to 20V, the wattage requirement will be substantially lower than the ground referenced topology. Sometimes, truly isolated supplies will be used, but converter circuits tied directly to the Vs supplies are very common



The situation with sleep mode is similar to thermal shutdown. In both cases, the amplifier is disabled by some circuitry which results in the output going into a high impedance state. One additional caution is that when coming out of sleep mode, an amplifier may saturate to one of the rails before recovering.



The common denominator of all non-linear modes of operation is the appearance of differential input voltages. One method of sensing when an amplifier is in a non-linear region is to use this false summing node technique.

If Rf"/Ri'=Rf/Ri, then Vdiff equals the voltage at the inverting node of the amplifier. This buffered error voltage signal can be used as an error flag possibly to drive a logical latch that could shut down the system.

ABS Maximums vs. The Spec Table

- Absolute Maximum Ratings
  - Stress levels, applied one at a time, will not cause permanent damage
  - Does NOT guarantee op amp performance
- Specifications
  - Linear operation ranges
  - Vos, Ib, drift, CMRR…guaranteed performance

Beware that one stress level may bring on a second, which calls off all bets on op amp survival. Consider a commercial part where the last line of the specification table called “TEMPERATURE RANGE,case” is listed as -25/+85°C. Even though the ABS MAX temperature is 125°C, the part may latch up (very large voltage offset) at 86°C. With loads such as DC coupled inductors this may also lead to violation of the SOA.

Datasheet, page 2

MP108 • MP108A

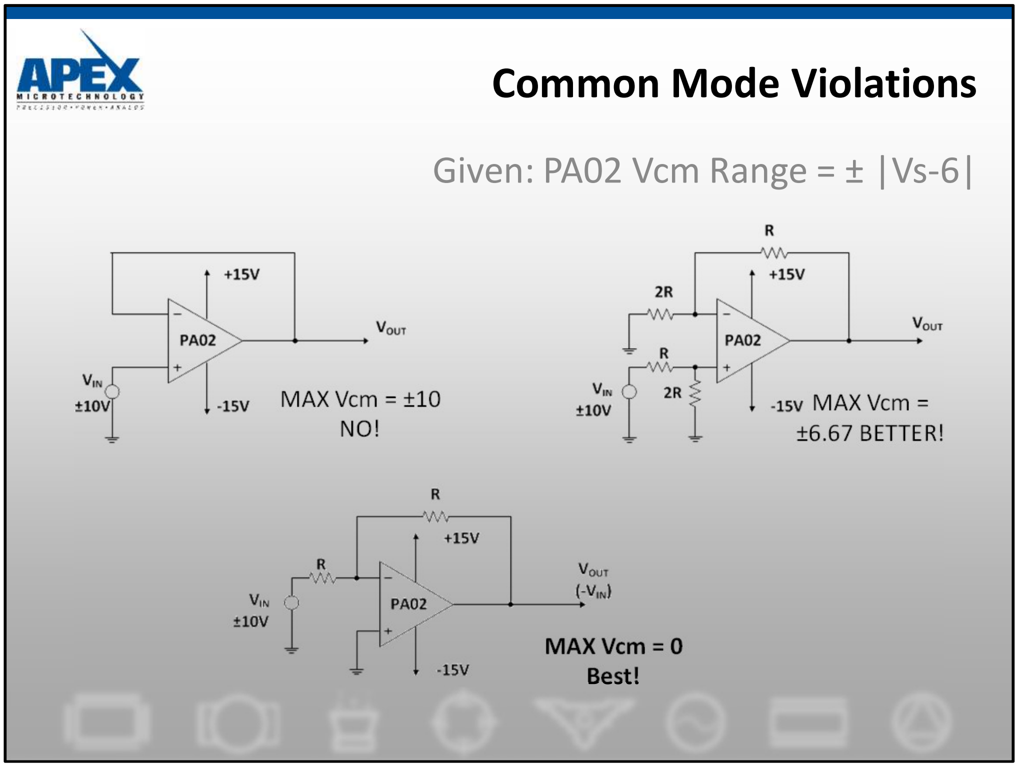
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_S$ to $-V_S$			200	V
SUPPLY VOLTAGE, $+V_B$ (Note 6)			$+V_S$, +15	V
SUPPLY VOLTAGE, $-V_B$ (Note 6)			$-V_S$, -15	V
OUTPUT CURRENT, peak, within SOA			12	A
POWER DISSIPATION, internal, DC			100	W
INPUT VOLTAGE			$+V_B$ to $-V_B$	V
TEMPERATURE, pin solder, 10s			225	°C
TEMPERATURE, junction (Note 2)			150	°C
TEMPERATURE, storage		-40	+105	°C
OPERATING TEMPERATURE RANGE, case		-40	+85	°C

SPECIFICATIONS

Parameter	Test Conditions (Note 1)	MP108			MP108A			Units
		Min	Typ	Max	Min	Typ	Max	
INPUT								
OFFSET VOLTAGE			1	5		*	3	mV
OFFSET VOLTAGE, vs. temperature	Full temp range		50			*		µV/°C
OFFSET VOLTAGE, vs. supply				20			*	µV/V

Absolute Maximum specification are found at the top of the second page of every Apex datasheet. Guaranteed specifications can be found below the absolute max specs.



In an inverting configuration, the op amps non-inverting terminal is usually tied to ground, making the inverting terminal a “virtual ground.” This results in zero common mode voltage: a desirable benefit. However, operating the amplifier in a non-inverting mode results in the common mode voltage being equal to the voltage at the non-inverting terminal.

The schematics above illustrate the problem. The amplifier used in this example cannot have any common mode voltage that approaches within 6 volts of either supply rail. The first example shows a unity gain follower. This is the configuration where common mode violations are most common. Note that the input voltage is equal to the common mode voltage. In our example the input voltage exceeds the common mode range.

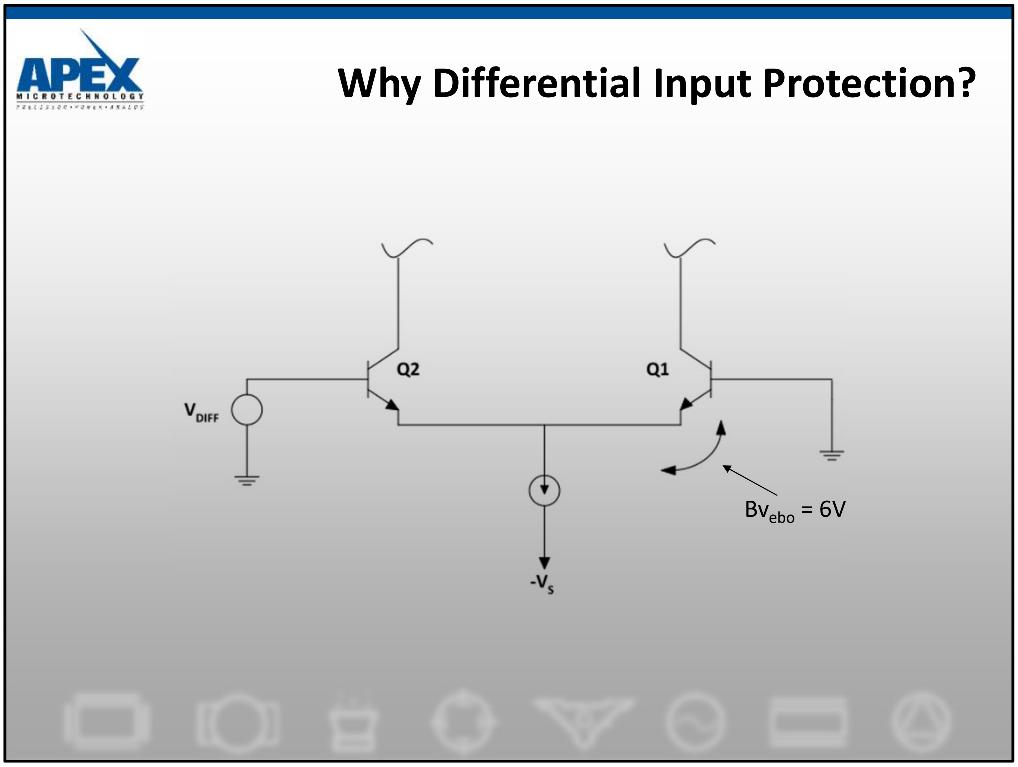
In the second example the input signal is first attenuated and then gained back up to result in a lower common mode voltage but a unity gain non-inverting transfer function. That is:
Vo = Vi(2R/(2R+R))(1+Rf/Ri)
where Rf = R and Ri = 2R

The third example shows the best approach to eliminating common mode violations: use inverting configurations. In this case the input voltage is still 10 volts, the output voltage is 10 volts, but the common mode voltage is zero, eliminating the problem. Of course this does invert the phase of the output signal.

Amplifier Protection

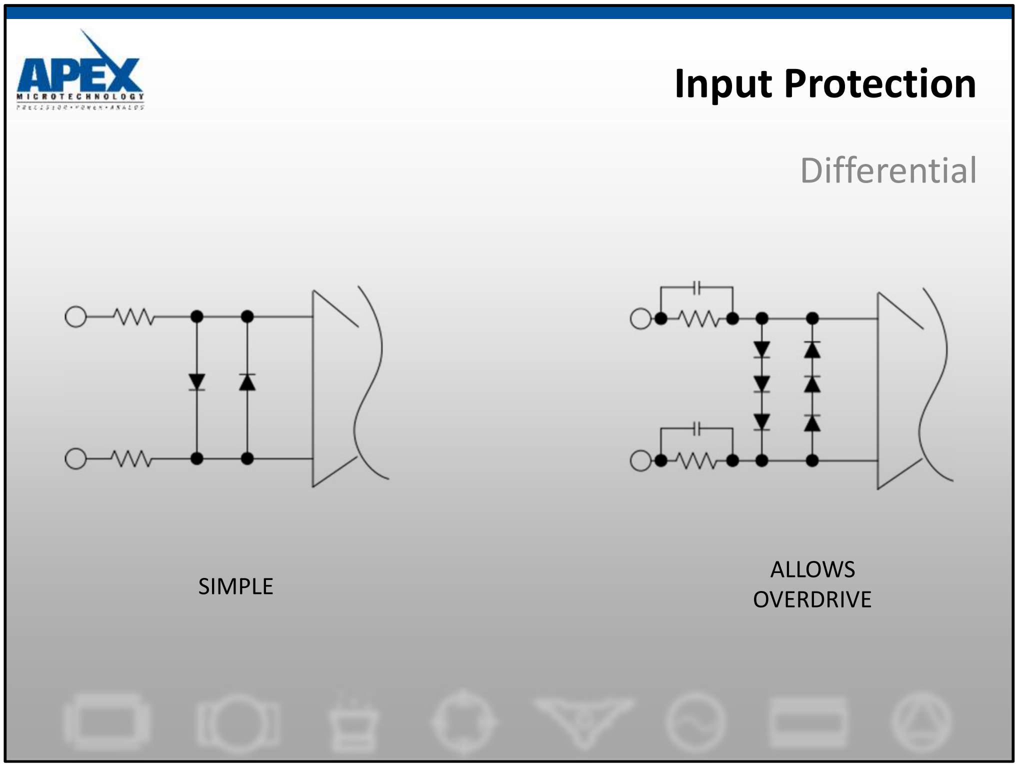
Electrical

- Input Transients
- Output Transients
- Over-voltage



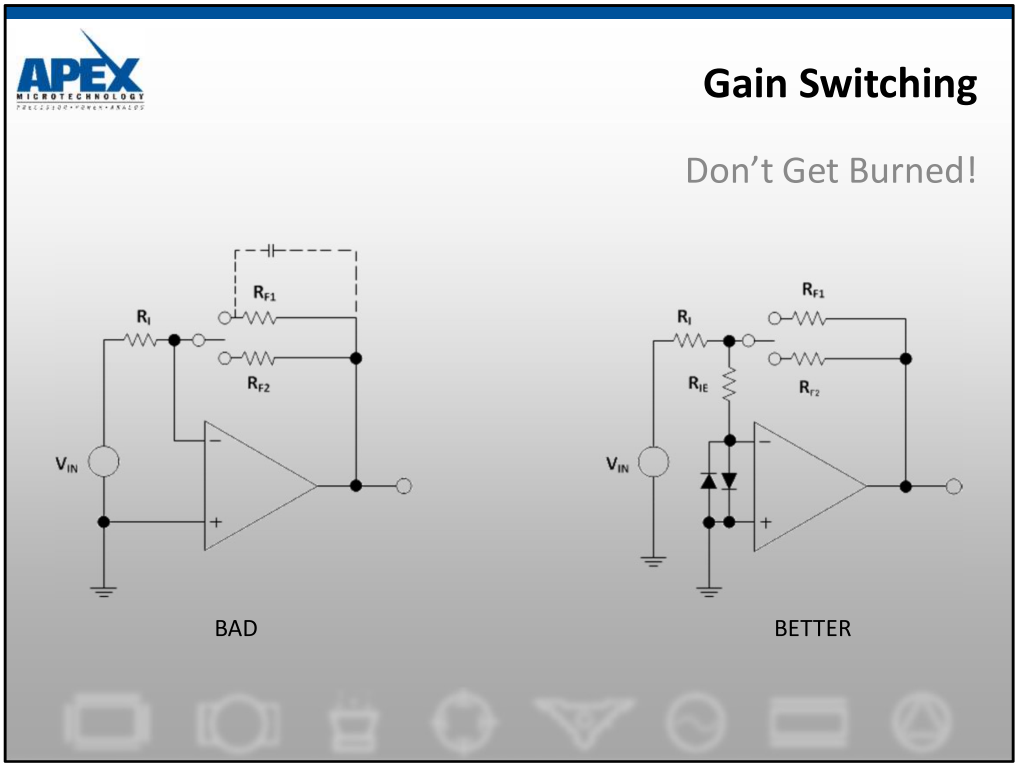
WHY DIFFERENTIAL INPUT PROTECTION?
Simple, to avoid damaging input stages due to differential overstress. Any input stage has maximum differential limits that can be exceeded any number of ways, with the most subtle occurring during non-linear operation.

In amplifiers with bipolar inputs, such as a PA12, differential overload has the additional hazard of causing degradation without catastrophic failure. Exceeding the reverse-bias zener voltage of a base-emitter junction of a transistor used in a differential amplifier can permanently degrade the noise, offset, and drift characteristics of that junction.



The protection scheme on the left uses parallel diodes to limit the differential voltage and uses series resistors to limit the current that flows through the diodes. The slightly more complicated scheme on the right accomplishes the same thing, but by using stacked diodes, allows a higher differential voltage to be developed. This allows a greater slew rate overdrive. The capacitors perform a similar function by allowing high frequency information to be passed directly to the input terminals.

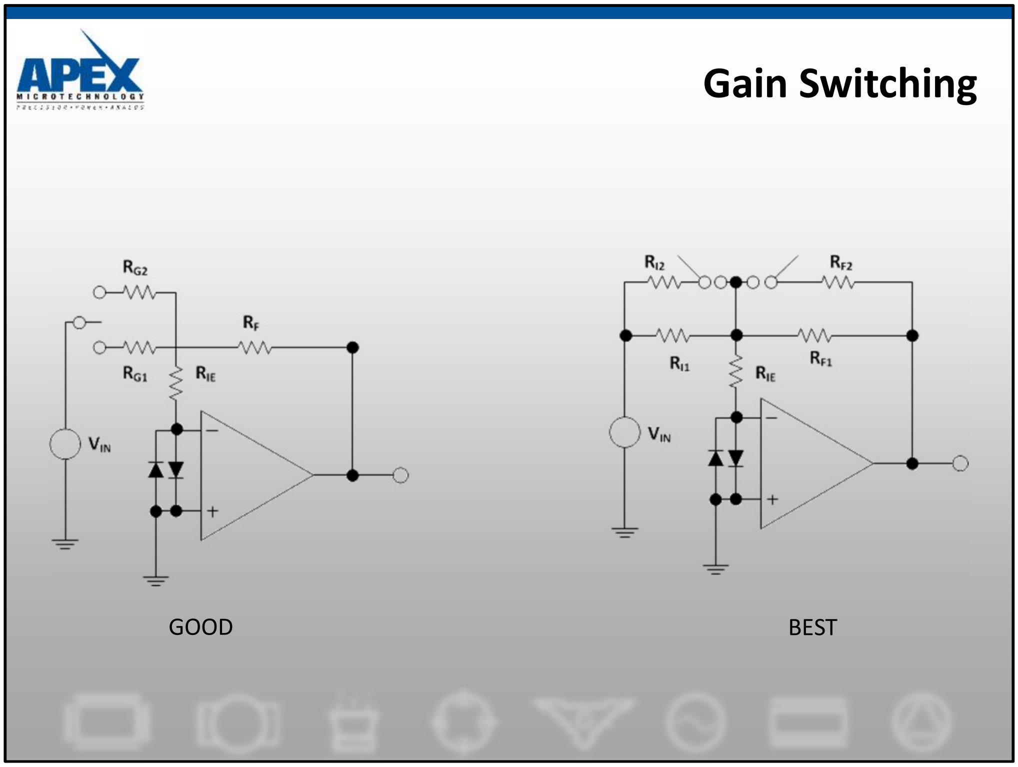
Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS
AN25 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS



Often it is a requirement that the gain of an amplifier be switchable. This is very common in ATE applications. One method of doing this is shown on the left. This is a very poor way to accomplish gain switching. The problem is that the amplifier is usually much faster than the relay used to switch between the two resistors. WHEN THE RELAY OPENS, THE AMPLIFIER HAS NO FEEDBACK. Since the amplifier is now open loop, the amplifier will immediately slew toward one of the supply rails. By the time the relay closes, the amplifier will be saturated and the output voltage will appear directly at the inverting terminal of the amplifier.

The method on the right does not solve the problem, but it does provide amplifier protection. The parallel diodes clamp the differential input voltage while Rie limits the amount of current that can flow during transient conditions. The value of Rie should be chosen to limit the current to approximately 15mA with one full supply voltage across the resistor.

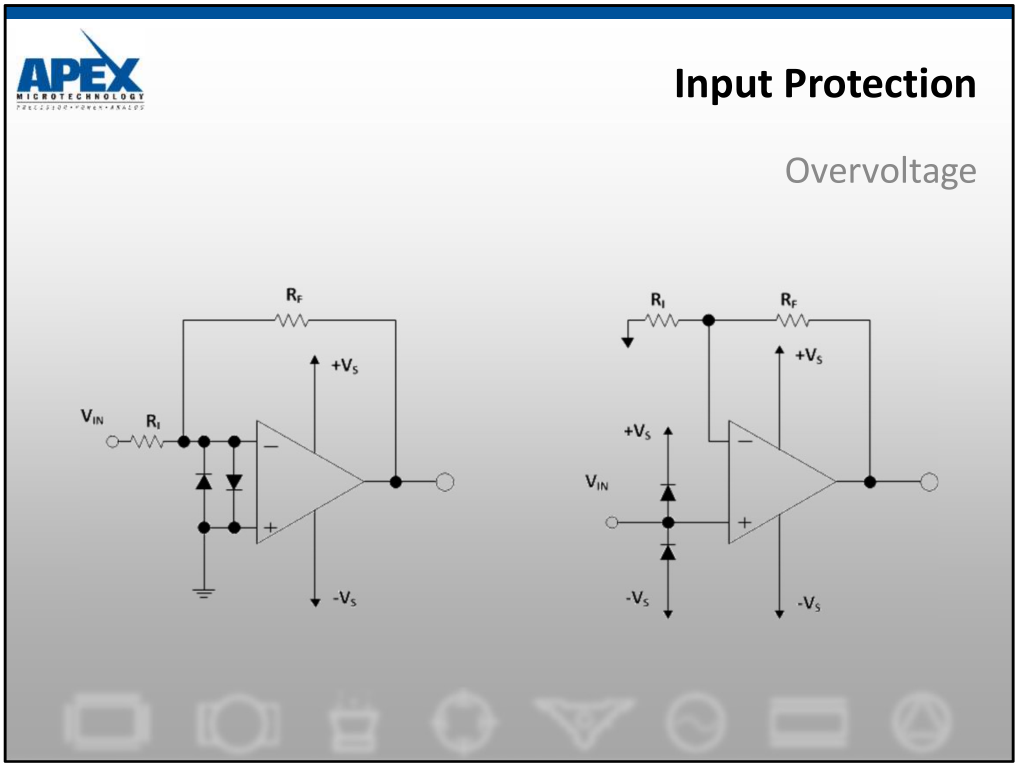
Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS



The "good" approach above represents a vast improvement over the previous technique. In this approach, gain is switched by switching the value of the input resistors rather than the feedback resistor. The major advantage to this approach is that the feedback loop is kept closed at all times. When the relay opens, the amplifier is now a unity gain follower with a zero volt input. The most voltage that will appear at the output is the offset of the amplifier. Input protection is still shown in this configuration to protect against possible switching transients.

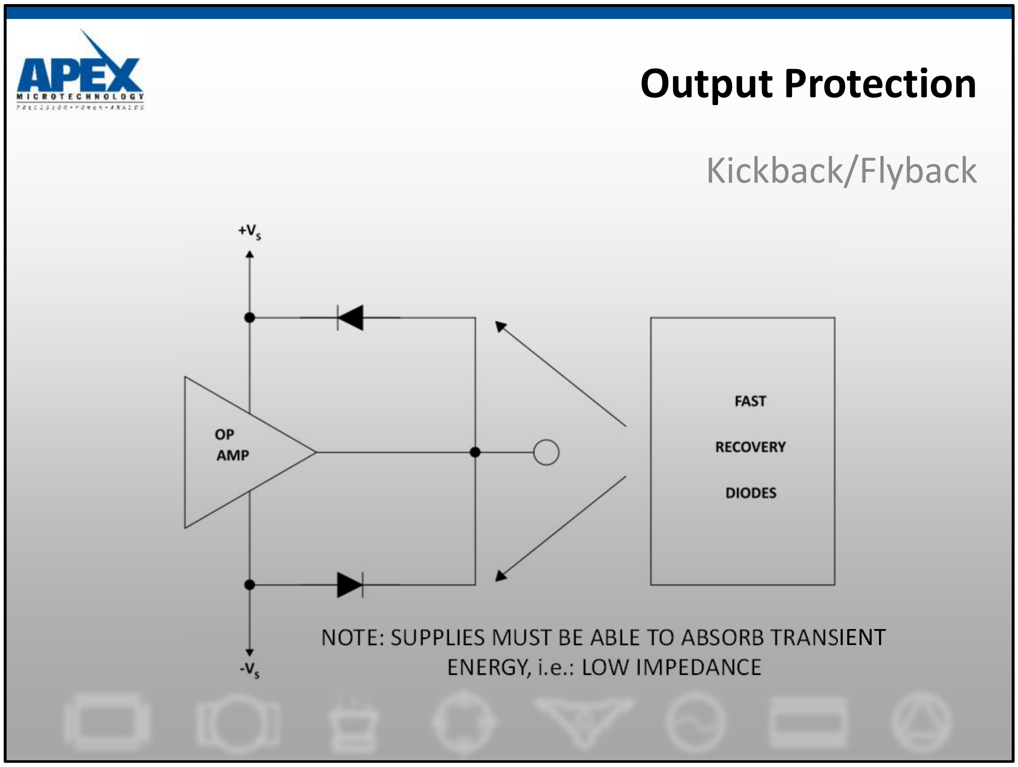
The "best" approach above shows a configuration that prevents switching inside the feedback loop or opening up the input loop. Ri1 and Rf1 are in place at all times. The gain of the circuit is switched by EITHER switching in Ri2 to parallel Ri1 OR by switching in Rf2 to parallel Rf1. This approach eliminates any transient voltages due to relay switching. At the time of contact closure, only the gain changes. Although input protection is still shown in this schematic, its only function is to protect the input in cases of non-linear operation, such as slew rate or current limit.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS



In multiple power supply systems, power supply sequencing is often a problem. If the power supplies for the "driving stage" come up before the "driven stage", the maximum input common mode specification may be violated. The diodes shown in the two circuits above serve to clamp the driven input to the amplifier supply pin so that the input cannot be raised above the supply voltage. Note, however, that if the supplies are in a high impedance state when the power supply is turned off, this approach will not protect the amplifier. Under those conditions however, the inverting amplifier configuration could be protected by running parallel diodes from the inverting node to ground. These would clamp the inverting input to ground under any circumstances. Since the inverting terminal is normally at virtual ground, these diodes would not interfere with signal in any way. However, on the non-inverting amplifier this approach will not work because the non-inverting input sustains a common mode voltage.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

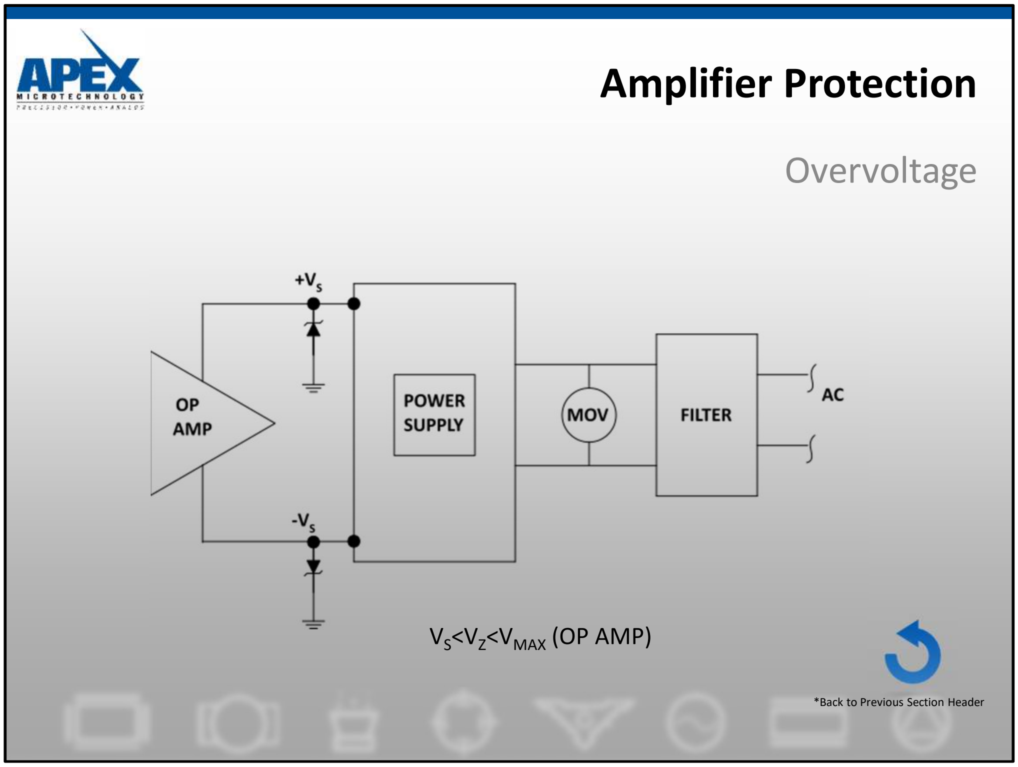


Attempting to make a sudden change in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, piezo-electric transducers not only generate mechanical energy from electrical energy but also vice versa. This means that mechanical shocks to a piezo-electric transducer can make it appear as a voltage generator. Again, this can destroy the output stage of an amplifiier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes SHOULD NOT be counted on to protect the amplifier against sustained high frequency kickback pulses. Under these conditions, high speed, fast recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes. These fast recovery diodes should be under 100 nanoseconds recovery time; and for very high frequency energy, should be under 20 nanoseconds.

One other point to note is that the power supply must look like a true low impedance source or the flyback energy coupled back into the supply pin will merely result in a voltage spike at the supply pin of the op amp again leading to an over voltage condition and possible destruction of the amplifier.

Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS
AN25 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS



The amplifier should not be stressed beyond its maximum supply rating voltage. This means that any condition that may lead to this voltage stress level should be protected against. Two possible sources are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply or AC main transients passing through a power supply to appear at the op amp supply pins. These over voltage conditions can be protected against by using zeners or transorbs direct from the amplifier supply pins to ground. The rating of these zeners whould be greater than the maximum supply voltage expected, but less than the breakdown voltage of the operation amplifier. Note also that MOS's can be included across the input to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors using power supplies will pass all high frequency energy and capacitors used in power supply are usually large electrolytics which have a very high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will pass on through the capacitor largely unscathed.

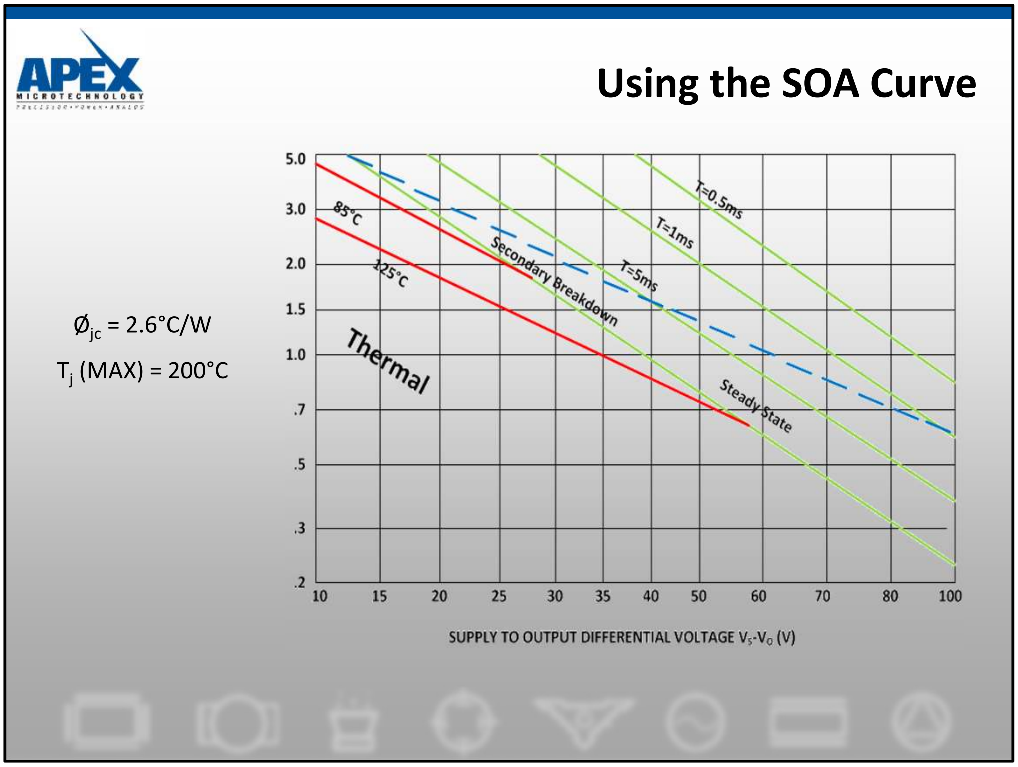
Ref. AN1 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS
AN25 HIGH VOLTAGE AMPLIFIER SUPPORT COMPONENTS

SAFE OPERATING AREA (SOA)

Safe Operating Area

Output Stage Danger!

- Current Handling Limitations
- Thermal (Power) Limitations
  - Steady State
  - Transient/Pulse Operation
- Second Breakdown
  - Bipolar Devices
  - MOSFETs: Not Applicable

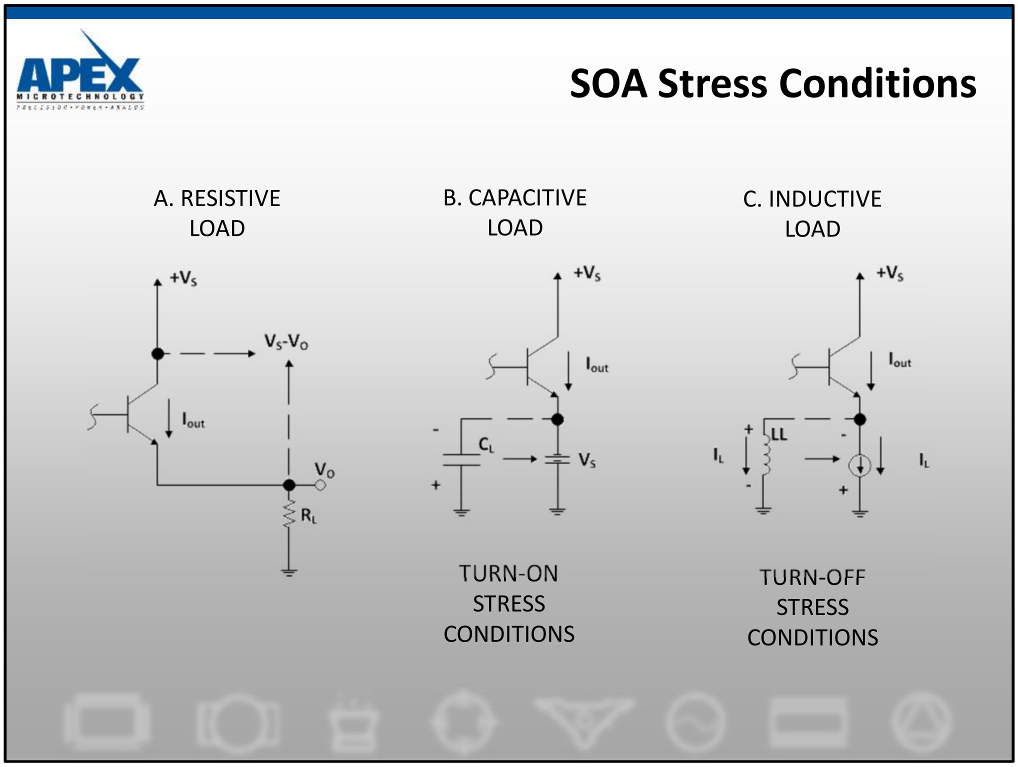


Safe operating area curves show the limitations on the power handling capability of power op amps. There are three basic limitations.

The first limitation is total current handling capability. A horizontal line or the top of the SOA curve and represents the limit imposed by conductor current handling capability die junction area and other current density constraints. The second limitation is total power handling capability or power dissipation capability of the complete amplifier. This includes both of the power die and the package the amplifier is contained in. Note that the product of output current on the vertical axis and Vs-Vo on the horizontal axis is constant over this line. The third portion of the curve is the secondary breakdown areas. This phenomenon is limited to bipolar devices. MOSFET devices do not have this third limitation. Secondary breakdown is a combined voltage and current stress across the device.

Although the constant current boundary and the secondary breakdown boundary remain constant, the constant power/thermal line moves toward the origin as case temperature increases. This new constant power line can be determined from the de-rating curves on the data sheet. The case temperature is primarily a function of the heat sink used.

The dashed line was constructed in this manner for Tc = 25°C for an amplifier advertised as a 67W device (PA07 or PA10). In addition to the fact that very few applications exhibit Tc=25°, secondary breakdown prohibits DC operation over its entire length!



On the SOA graph, the horizontal axis, $V_S–V_O$ does not define a supply voltage or total supply voltage or the output voltage. IT DEFINES THE VOLTAGE STRESS ACROSS THE CONDUCTING DEVICE. Thus $V_S–V_O$ is the difference from the supply to the output across the transistor that is conducting current to the load. The vertical axis is simply the current being delivered to the load.

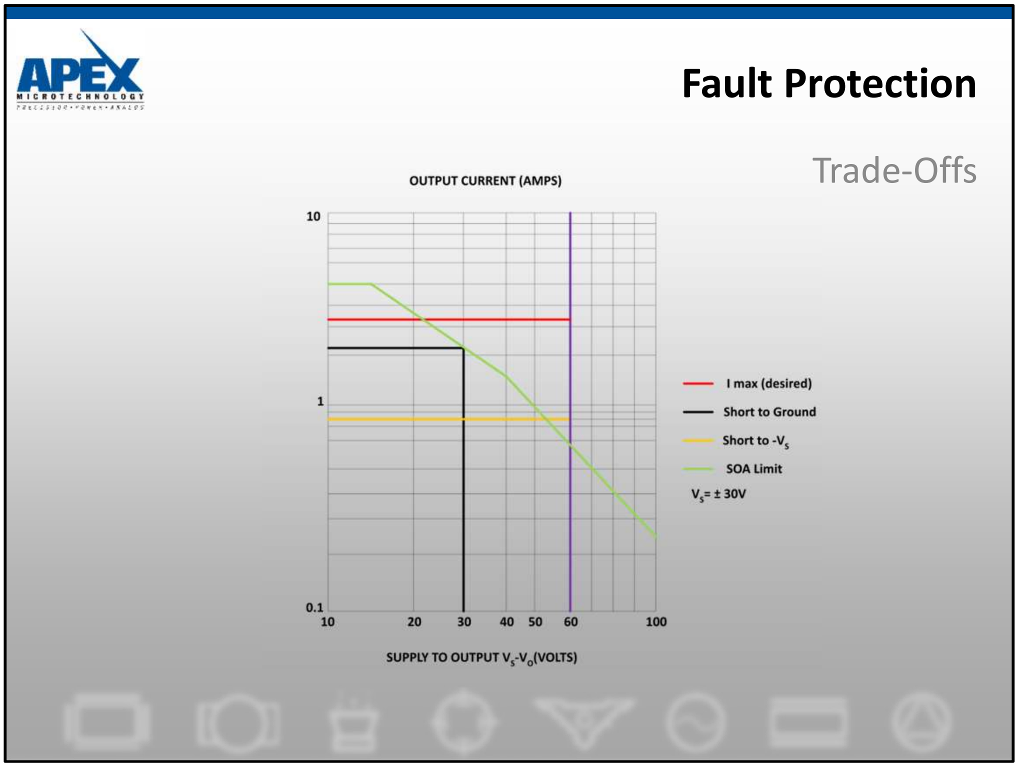
For resistive loads maximum power dissipation in the amplifier occurs when the output is 1/2 the supply voltage. This is because when the output is at 0 volts, no current flows from the amplifier whereas at maximum load current very little voltage is across the conducting transistor since the output voltage is near the supply voltage.

For reactive loads this is not the case. Voltage/current phase differences can result in higher than anticipated powers being dissipated in the amplifier.

An example of an excessive stress condition created by a capacitive load is shown in Figure B. In this case the capacitive load has been charged to $–V_S$. Now the amplifier is given a “go positive” signal. Immediately the amplifier will deliver its maximum rated output current into the capacitor which can be modeled at t = 0 as a voltage source. This leads to a stress across the conducting device of Imax X total supply voltage($2V_S$).

Figure C shows a similar condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the conductor has built up to some value IL. Now the amplifier is given a “go negative” signal which causes the output voltage to swing to down near the negative supply. However the inductor at time t = 0 can be modeled as a current source still drawing IL. This leads to the same situation as before, that is total supply voltage across a device conducting high current.

Ref. AN1 SAFE OPERATING AREA, AN22



Current limit can be used to protect the amplifier against fault conditions. If, for instance, it is desired to protect the amplifier against a short-to-ground fault condition the Vs-Vo number on the horizontal axis is equal to Vs since Vo is zero. Following this value up to the power dissipation limit and then across to the output current gives the value of current limit necessary to protect the amplifier at that case temperature. Note that better heat sinking allows higher values of current limit.

For more aggressive fault protection it may be desired to protect the amplifier against short to either supply. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the Vs-Vo axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit.

It is often the case that requirements for fault protection and maximum output current may conflict at times. Under these conditions there are only four options. The first is simply to go the an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called “foldover” or “foldback.” This is available on some amplifiers such as the PA10 and PA12.

Ref. AN1 SAFE OPERATING AREA, AN22

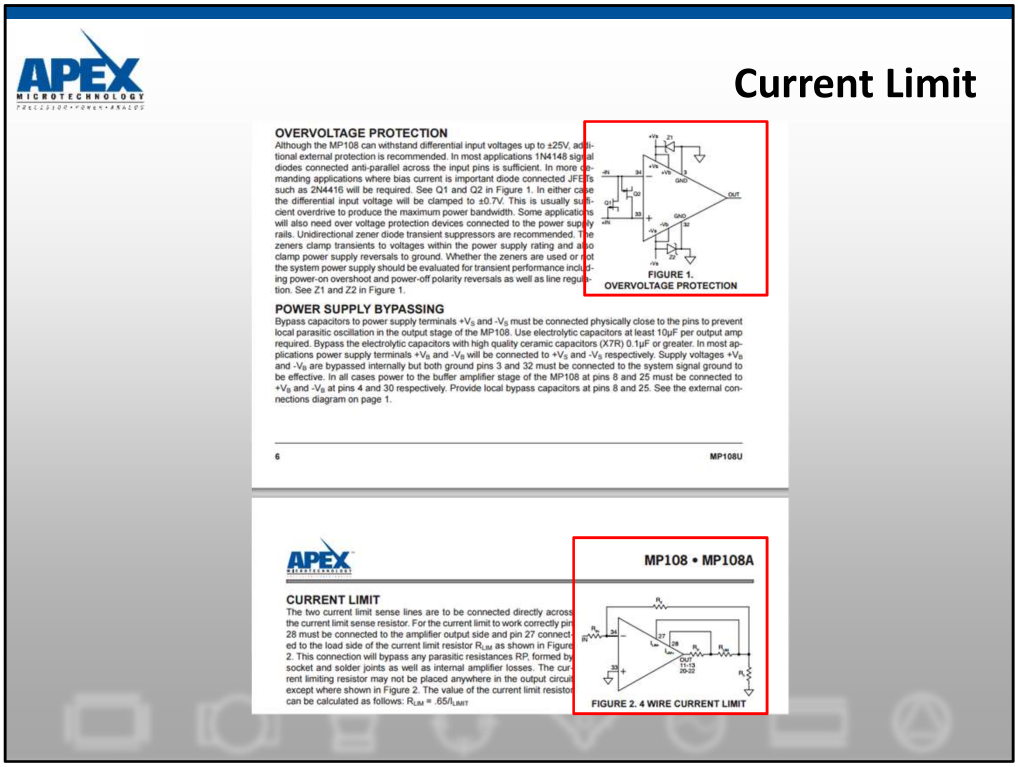
Current Limit Definition

A way to force output voltage where ever needed to maintain constant output current.

- A non-linear mode of operation
- $V_{OUT} = f(I_{LIMIT} \text{ and } Z_{LOAD})$
- I_{LIMIT} is only one term of the power equation

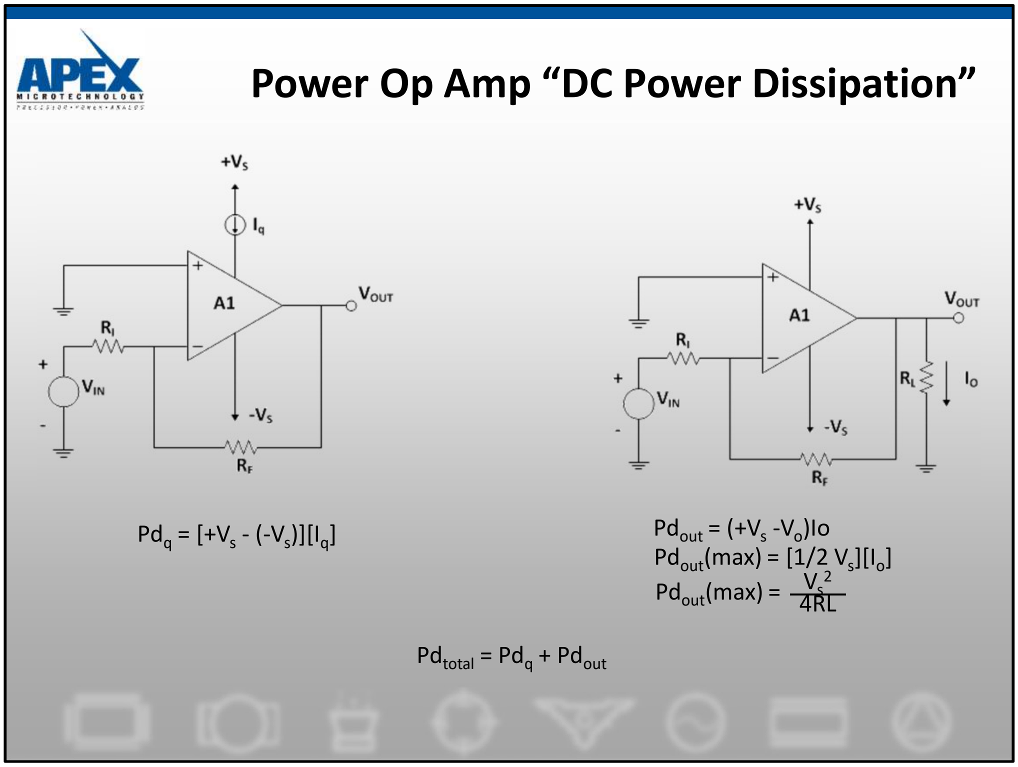
Current limit circuits do what their name implies but they are not magic cures for all load fault conditions. The non-linear operation (the op amp is unable to satisfy input signal/feedback demands) means monitoring the inputs for the presence of a differential voltage will signal this mode of operation.

Usually the current limit mode will reduce the output voltage but this is not always true. To determine critical survival the worst case voltage stress across the conducting transistor must be determined.



There are several different internal schemes used to implement current limit in Apex products. Most datasheets will have a formula or some text explaining the implementation used for the product. If there is no formula or reference, refer to application note 1.

Note that in most cases, all of the output current flows through the current limit resistor. Use $I^2 * R$ to determine the power rating for the resistor



When calculating power dissipation in an amplifier, you MUST NOT FORGET THAT POWER DISSIPATION IN THE AMPLIFIER IS NOT EQUAL TO POWER DISSIPATION IN THE LOAD. That is, most of the time. One exception is when the output voltage is half of the supply voltage and the load is resistive. In this particular case the power dissipations are equal.

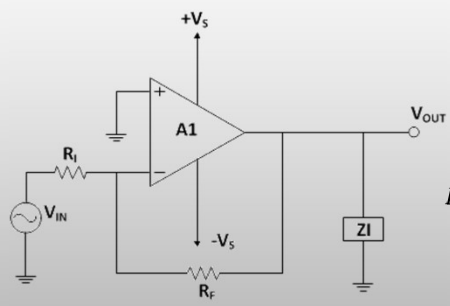
Calculating power dissipation in an amplifier under DC conditions with a resistive load is very simple.

The first portion of power dissipation is due to the quiescent power that the amplifier dissipates simply by sitting there with +Vs and –Vs applied. Multiplying total supply voltage by quiescent current gives the value of this power dissipation.

The maximum power dissipation in the amplifier under DC conditions with a resistive load is when the output voltage is 1/2 of the supply voltage. Therefore, whatever current is delivered to the load at 1/2 supply voltage multiplied by 1/2 supply voltage gives maximum power dissipation in the amplifier. The total dissipation is the sum of these two.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

Power Op Amp "AC Power Dissipation"



$$ZL = |\,Z_l\,|$$

$$Pd_{out}(max) = \frac{2V_s^2}{\pi^2\, ZL \,Cos\,\theta}, \quad \theta < 40°$$

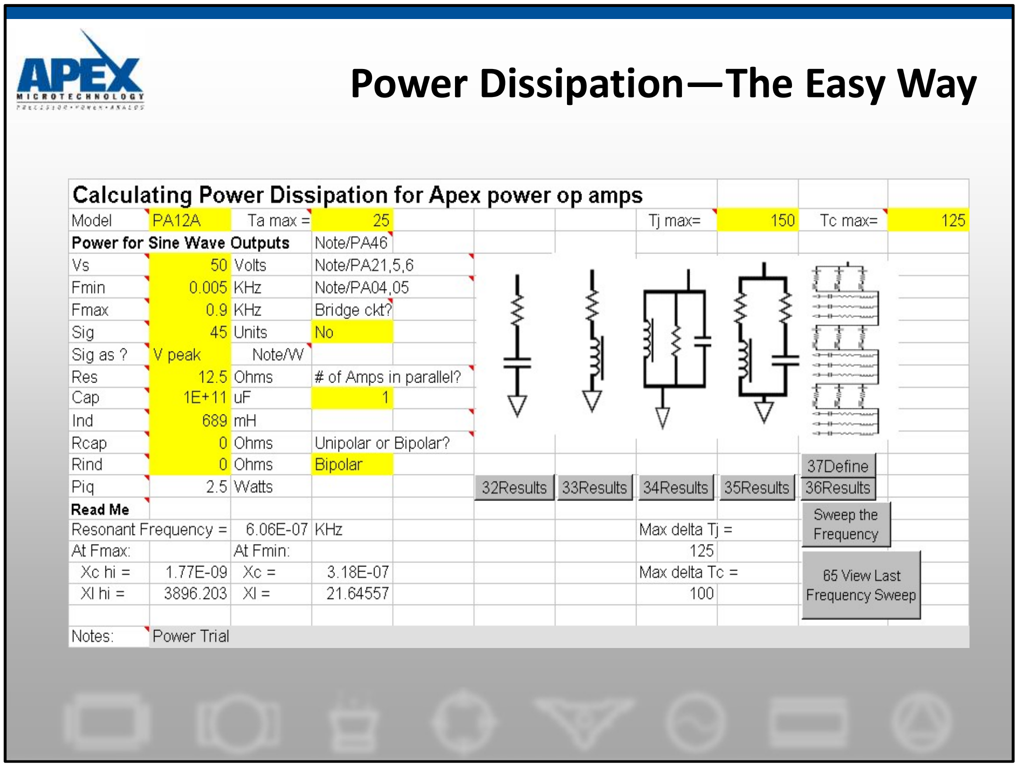
$$Pd_{out}(max) = \frac{V_S2}{2ZL}\left[\frac{4}{\pi} - Cos\theta\right], \quad \theta > 40°$$

$$P_{total} = Pd_{out}(max) + Pd_q$$

With an AC output and/or reactive loads, output power dissipation calculations can get a bit stickier. Several simplifying assumptions keep the problem reasonable for analysis. The actual internal dissipation can be determined analytically or through thermal or electrical bench measurements. Both Application Note 22 and Application Note 1 General Operating Considerations give details on measuring AC power dissipation.

Worst case AC power dissipation formulae are given above for any reactive load range. With these worst case formulae one can calculate worst case power dissipation in the output stage for AC drive conditions and reactive loads.For most power op amps output stage power dissipation is the dominant component of total power dissipation so adding worst case AC output power dissipation with DC quiescent power dissipation and using AC Rθjc AC thermal
impedance for junction to case, will be sufficient for heatsink calculations.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

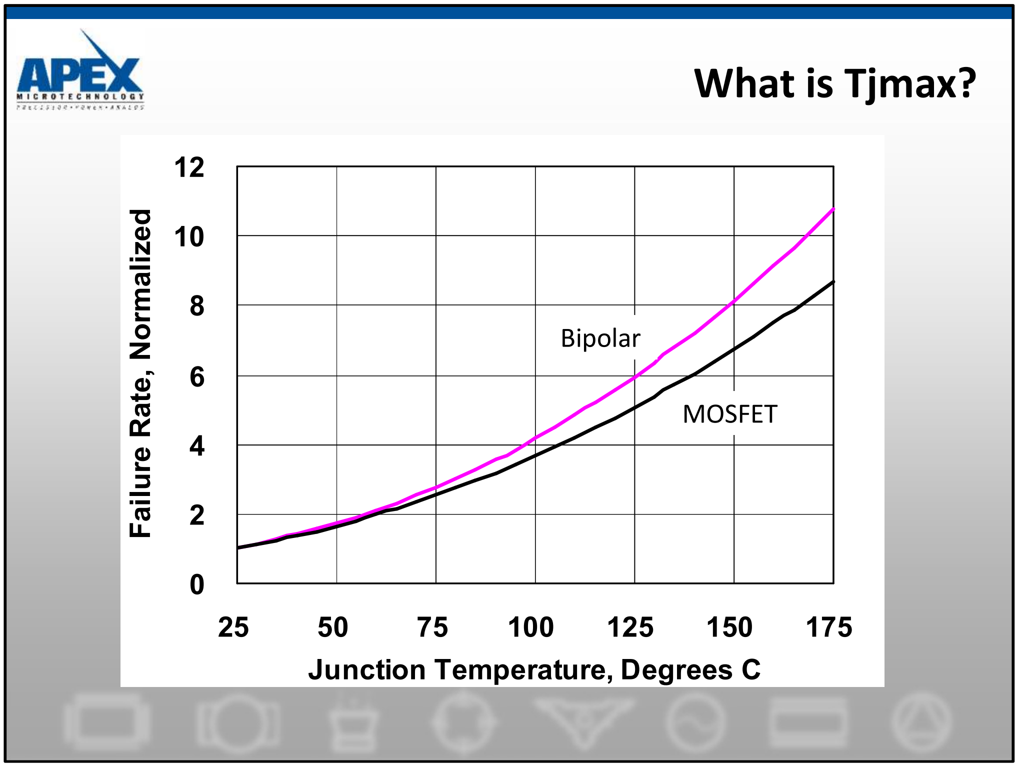


If your application can be modeled as a sine wave of any frequency, this sheet will tell you a lot. Entering a model pulls up a sizable portion of the data sheet for calculation and flag raising. Enter the three temperatures: ambient from the application, case per data sheet max or lower, and junction per contract or philosophy on reliability. If you need DC response, anything below 60Hz is OK. Define your output signal in terms of volts, amps or watts. If your load can be modeled by one of the first four diagrams, enter the values below. If you need diagram 5, use the Define Load command button.

Be sure to check these three cells!
If the Bridge circuit cell is “Yes”, the signal and load values specified will be treated as total but internal power will be for a single op amp.
Internal power will be divided by the # of parallel amplifiers.
“Unipolar” forces only one power supply and the use of DC thermal resistance.

A few useful pieces of information show up on this screen along with a red flag if your specified supply voltage is out of bounds. For more answers use the command button below the desired load diagram.

Ref. AN37



While this author would be the first to agree MIL-HDBK-217 has a few quirks and is very often misused, it does have the curves sloping in the right direction. Electronics is similar to your car, toaster- -almost anything, even engineers! Run it too hot and it dies an early death. Apex suggests a maximum of 150°C for normal commercial applications. If the equipment is remotely located or down time is extremely expensive a lower temperature is appropriate.

This graph represents the temperature acceleration factors from revision F, Notice 2.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

	At Fmin:	At Fmax:
Z in Ohms	15915.50	21.87
Phase angle	-89.95	-46.70
RMS Amperes	0.0012218	0.8891318
Peak Amperes	0.0017279	1.2574223
RMS Volts	19.445436	19.445436
Peak Volts	27.5	27.5
RMS Power	0.0237583	17.289557
Peak Power	0.0475166	34.579113
Power factor	0.001	0.686
Input power	0.04	32.02
True power	0.00	11.86
Percent Efficiency =	1.16	50.82
Vpk capability =	35.00	34.87
Op amp internal dissipation:		
Input power	0.04	32.02
Dissipation RMS	0.04	20.16
Dissipation Peak	0.08	37.14
Total in heatsink	2.08	22.16
WC watts & Rth	22.161084	0.9

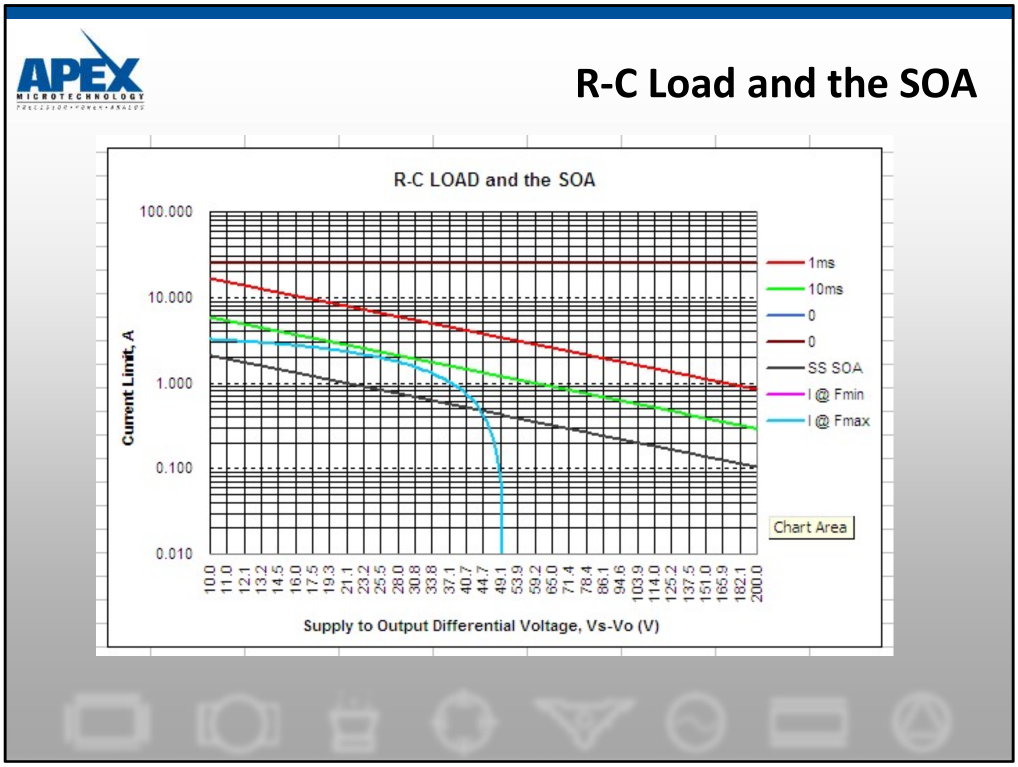
At Fmin:	At Fmax:		
Maximum AC Pint			
39.6	37.8	Vpk	
28.001429	26.728636	Vrms	
0.0017594	1.2221521	Arms	
0.0492652	32.66646	Wrms	
4.643E-05	22.404837	Wtrue	
0.0633588	44.012142	Pin	
Minimum HS:		2.61	°C/W
Actual HS:		10	°C/W
Results in Tjmax =		268.77	°C
Results in Tcmax =		248.82695	°C
TOO *@&!# HOT!!!!			
2.6074487	4.6405182	2.6074487	

If you’re in a hurry, go to the right side just above the yellow box to find the smallest heatsink usable. Enter data sheet rating for selected heatsink to see maximum case and junction temperatures.

Since the low frequency load is so light we'll look at the high frequency numbers only. Below impedance & angle are the operating points of the load; amps, volts, watts and power factor. Next we find power being drawn from the supplies due to driving the load and true power dissipated by the load. This leads to efficiency (at your specified signal level). If the peak output capability based on the supply and output current is more than a few volts above required output, lowering supplies will reduce internal dissipation.

In the upper right, the worst case amplitude for your load is estimated (this amplitude varies with phase angle). Op amp RMS dissipation is calculated by subtracting true power from input power at worst case amplitude or your maximum level. Peak op amp dissipation is taken from the graph below. “Total in heatsink” uses peak if the frequency is below 60Hz (else RMS), then adds quiescent power. The last line picks worst case frequency and gives you power and thermal resistance for heatsink sizing. The three cells in the lower right are heatsink needed to keep the case cool, to keep the junctions cool without regard to the case, and the smaller of the two.

Ref. AN37



Remember transistor load lines from school? This is it and there should be no major surprises. At least none that we can't explain or fix.

The lack of an Fmin curve in this example is because our load is completely off scale with peak current of only 1.7mA.

Note the 10ms and 1ms pulse lines. For the conditions shown above, a 10ms puls at 10% duty cycle or less would be safe. Longer pulses or continuous duty would violate the SOA and would result in the creation of an expensive paper weight.

If one of the load lines peaks over the SOA curve remember we are looking at ½ of a sine wave while the heatsink may have been sized on RMS values. If it looks like you have a lot of wasted power handling capability, go back and enter maximum case and junction temperatures calculated for the actual heatsink to be used.

Application note 37 describes the use of the PowerDesign spreadsheet tool to aid the designer in calculating load lines and determining the suitability of the product.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING, AN22, AN37

Resistive Load Line Calculations

PA07

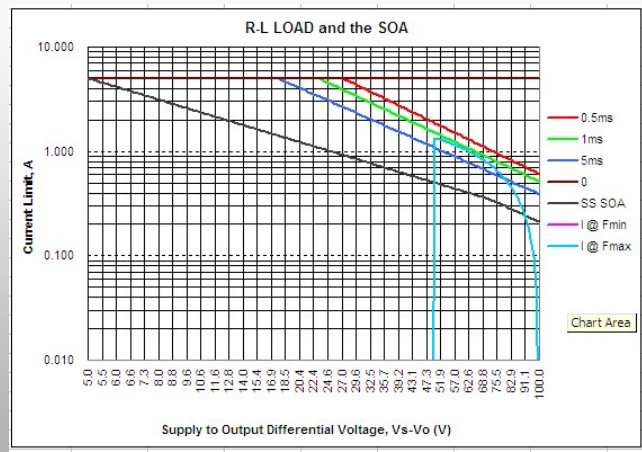
100Vs

37.3 Ω

1.34A @ 50V

67 W max

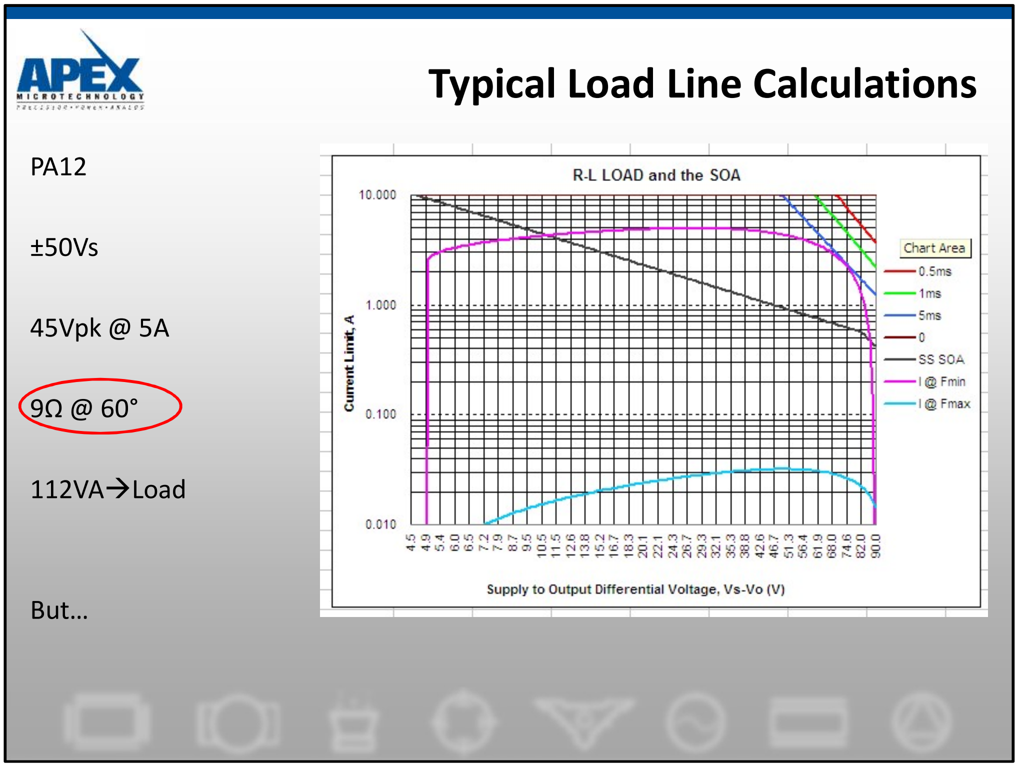
But…



So, you've checked the maximum power dissipation at ½ the single supply voltage and all is well (discounting the fact this example requires an infinite heatsink). The job is not over! At frequencies below 60Hz you do not to cross the second breakdown curve at all. At higher frequencies, keeping the duty cycle of these excursions down to 5% will keep you out of trouble.

When using dual symmetric supplies and pure resistive loads, all Apex power op amps are immune to this problem. For all other cases use Power Design.xls to plot sine wave load lines for you. This graph is from the power sheet but a trick had to be pulled to get a plot where output voltage is over 50% of the total supply voltage. In the Vs cell enter 100 volts and use the Unipolar or Bipolar input cell to specify Unipolar output current. This causes Power Design to calculate quiescent current on a single 100V supply and to use DC thermal resistance because only one transistor is doing all the work.

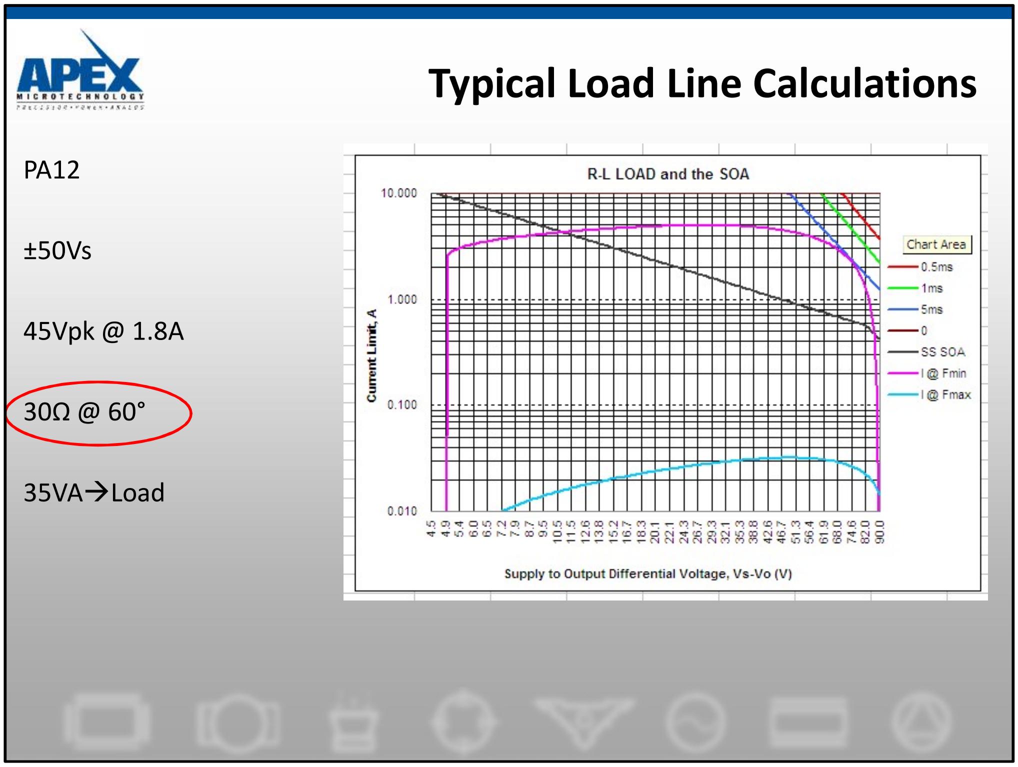
Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING, AN22



Can a 125W, 10A device drive this 5A load? It's a large coil (250mH and 4.5Ω) and the frequency is only 5Hz. If efficiency were only 50%, delivering this 112VA to the load should be OK, shouldn't it? No. And no.

Phase shift is the killer here. You can see right away the load line exceeds the second breakdown curve. Look at current at the 56.2V stress level; its almost 4A (3.93 actually) giving peak dissipation of about 220W. Indeed, the data above this graph says the number is 223.5W (including Iq). We are in big trouble even though a 9Ω pure resistive load would have been fine with dissipation of only 72W and no hint of second breakdown problems.

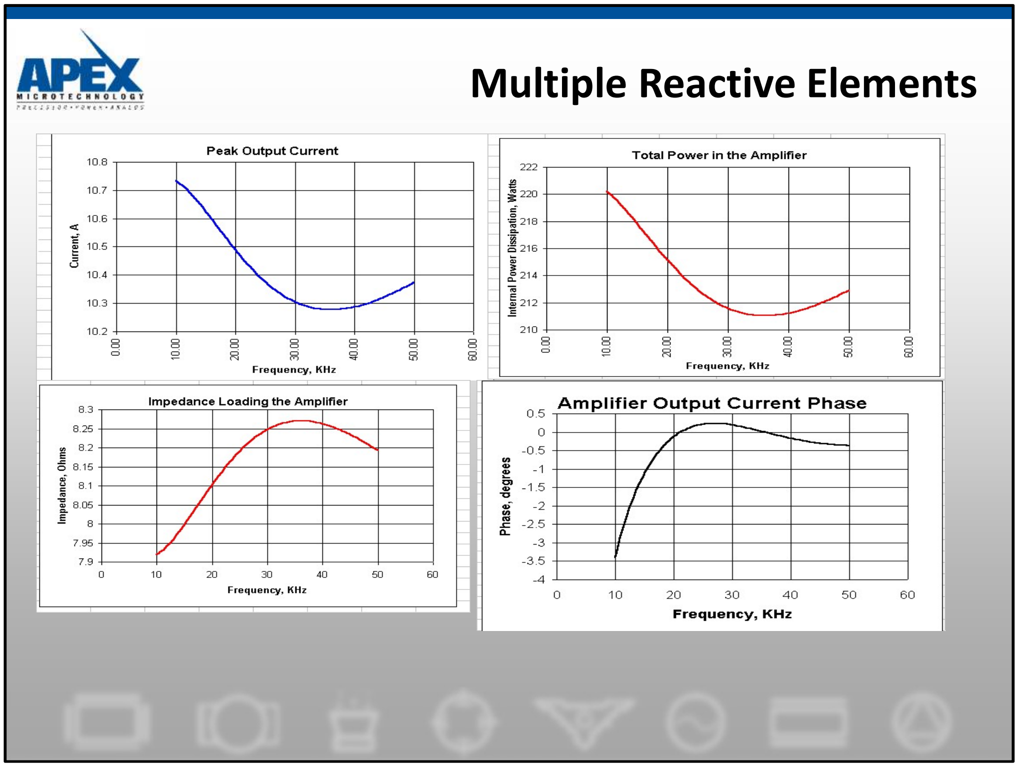
It is time to look for a bigger amplifier or negotiate the load specifications.



Reducing the load requirements all the way to 30Ω produces a load line not in violation of the second breakdown curve and power dissipation in the amplifier is down to a manageable 72W.

The probability of negotiating load specs this far is rather dim. Its time to look at a bigger amplifier such as the PA05.

Of course, this is a very low frequency application with an inductive load so a switching amplifier such as the SA60 may be a much more suitable choice. The PWM section of the seminar explains the pros (high efficiency) and cons (high noise, more involved design) of using the switching amplifier approach.

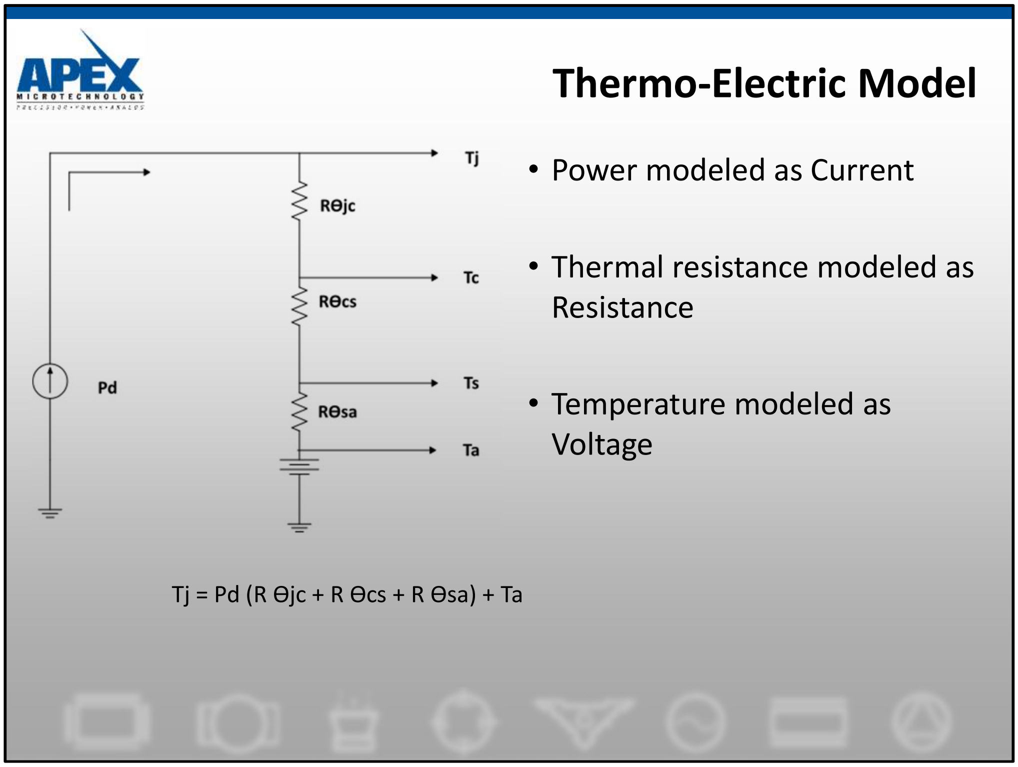


Any time an application has more than one reactive element, peak values of voltage, current, phase shift and power dissipation may not be at the minimum or maximum frequencies. It would be a good idea to run a frequency sweep to locate worst case operating points.

These graphs model operation of a tuned piezo load and the transmission line. In this case we find worst case power dissipation in the amplifier is at minimum frequency. Don’t get caught by surprise with a complex load producing a power peak instead of a dip.

Frequency sweep requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then sweep.

Ref. AN37



The thermo-electric model translates power terms into their electrical equivalent. In this model, power is modeled as current, temperature is modeled as voltage, and thermal resistance is modeled as electrical resistance.

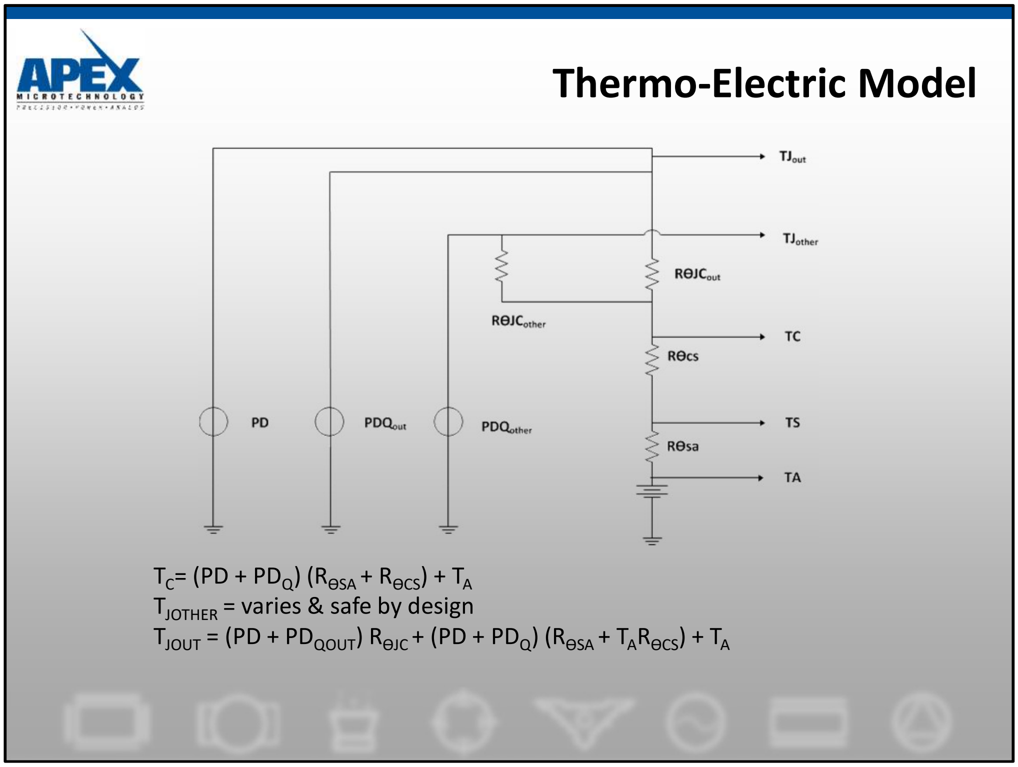
The real "name of the game" for power amplifiers is to keep Tj as low as possible. As you can see from the model, there are two approaches to doing this. The first is to reduce the current, ie; the power dissipation. The second is to reduce the thermal resistance.

Reducing power dissipation can be accomplished by reducing the supply voltage to no more than what is required to obtain the voltage swing desired. This reduces the Vs-Vo quantity to as low a value as possible.

The thermal resistance problem should be attacked on all three fronts. Rjc, the thermal path resistance from the semiconductor junction to the case of the amplifier, is characteristic of the amplifier itself. The way to obtain maximum reliability and cool junction temperatures is to buy an amplifier with as low a Rjc as affordable.

Rcs is the thermal resistance from the case to a heat sink. This resistance is minimized by good mounting techniques such as using thermally conductive grease or an approved thermal washer, properly torqueing the package, and by not using insulation washers.

The last piece of the thermal budget is Rsa, the thermal resistance of the heat sink to ambient air. This is a very crucial piece of the puzzle and should not be skimped on. A quick glance at an SOA curve that shows the difference between the power limitations of an amplifier with a 25°C case and an 85°C case shows the benefit of using the maximum heat sink allowable.
Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING



In this model, quiescent power has been split according to the actual transistors generating the heat. PDQout is only the quiescent current flowing in the output transistors. When appropriate, this specification will appear in the amplifier data sheet. Multiply this output stage quiescent current times the total supply to find worst case PDQout.

PDQout = IQout (+VS + |-VS |)

PDQother is the current flowing in all the other components and could be found by subtracting PDQout from PDQ .

Note that the data sheet junction-to-case thermal resistance speculations refer to only the output transistors. Thermal resistances and power dissipations of other components vary wildly. Design rules applied by Apex for all these components insure they will be reliable when operating within maximum supply voltage, maximum input voltage and maximum "Meets full range specifications" case temperature.

No matter which model you use, there are three thermal resistances contributing directly to hot junctions. The thermal resistance should be attacked on all three fronts:
1) Buy an amplifier with the lowest possible RØJC.
2) Use good mounting practices.
3) Use the largest practical heatsink.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

Heatsink Selection

PA02 POWER OP AMP

- P_d = 14 Watts
- T_a = 35° C
- R_{jc} = 2.6° C/W
- R_{cs} = .2° C/W

APEX HEATSINK TO KEEP T_j = 100° C

- $T_j = P_d (R_{jc} + R_{cs} + R_{sa}) + T_a$
- $100°C = 14W(2.6°C/W + .2°C/W + R_{sa}) + 35°C$
- R_{sa} = 1.8° C/W

SELECT APEX HS03:R_{sa} = 1.7° C/W

This calculation illustrates the heat sink selection procedure using the thermal electric model discussed. First we calculate the power dissipation within the amplifier under worst case conditions. In this example, that number came out to 14 watts. Next we pick a desired value of Tj. In this example, we picked a very conservative value of 100°C. This value of Tj will result in a very large mean time to failure, spelling reliability for this application. Consulting the data sheet for the PA02, we find that the maximum DC thermal resistance from junction to case is 2.6° C per watt. Next, we consult the APEX Data Book to determine that the typical case to heatsink resistance is between .1 and .2° C per watt, when thermal grease is used. Solving the given formula for the unknown, Rsa, we find that the required thermal resistance is less than or equal to 1.8° C per watt. This can easily be achieved by using the Apex HSO3 Heatsink which has an RSA of 1.7° C per watt.

If a system has forced air or a liquid cooling system available, physical size of the heatsink can be decreased. Heatsink data sheets often graph thermal resistance vs. air velocity. Fan data sheets usually speak of volume moved. At the very least a conversion is needed which takes in account the square area of the air path as it passes the heatsink.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

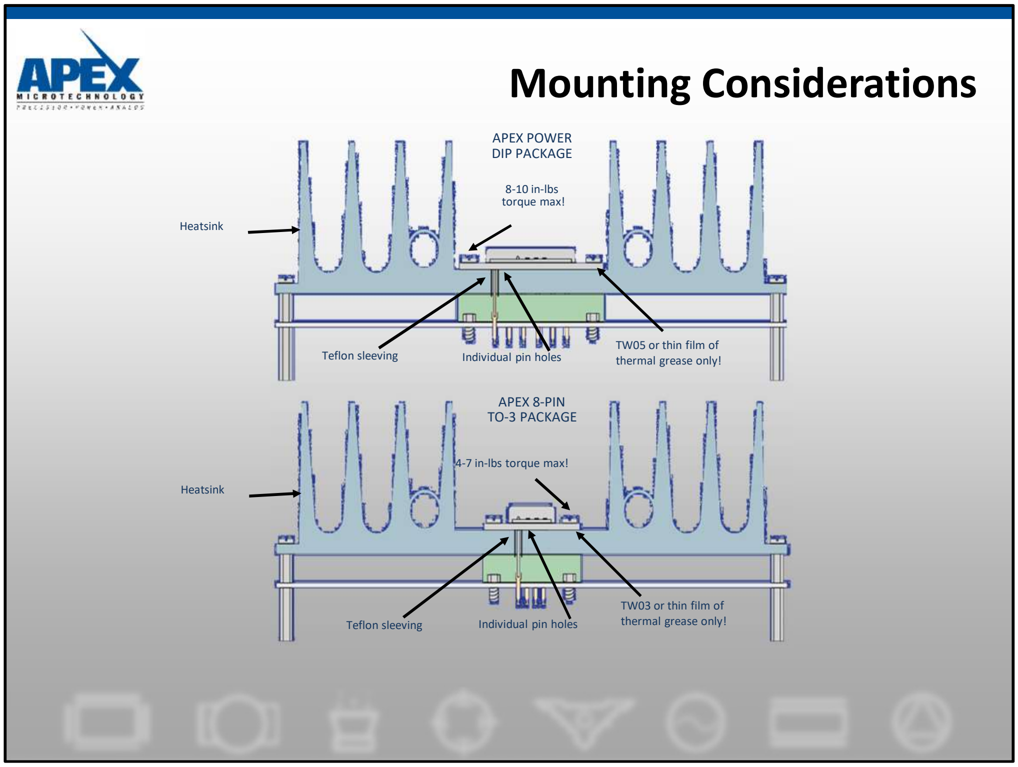
Thermal Capacity can be a Big Friend

- For pulse mode operation
- When pulses > 8ms
- Ap Note 11 Thermal Techniques
- Thermal response $\cong$ to R-C response

- Δ V = e^x-t / RC
- Δ temp = e^x-t / TAU

If the drive signal is pulse mode, internal power between pulses is zero and individual pulses are less than 8ms, size the heatsink by dividing the pulse power by the duty cycle and adding the quiescent power.

For other pulse mode operations Application Note 11, Thermal Techniques, is the reference. It will explain how to calculate thermal capacity, thermal time constants and plot the charge/discharge curve. It also lists some common unit conversions and constants.



Key areas to check for proper mounting techniques:

1) Heatsink flatness.

2) Individual heatsink thru-holes for each pin.

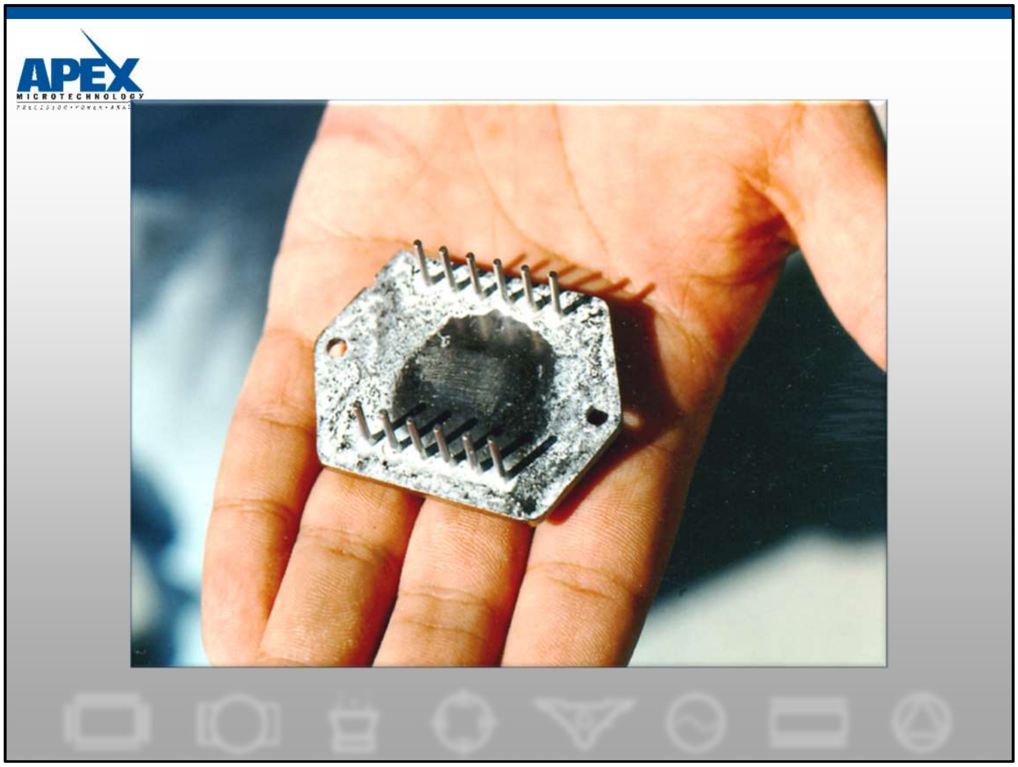
3) Thermal interface between case and heatsink.

4) Mounting torque.

5) Sleeving on pins—thickness of heatsink.

A detailed discussion of these areas follows.

Ref. AN1 AMPLIFIER MOUNTING AND MECHANCIAL CONSIDERATIONS

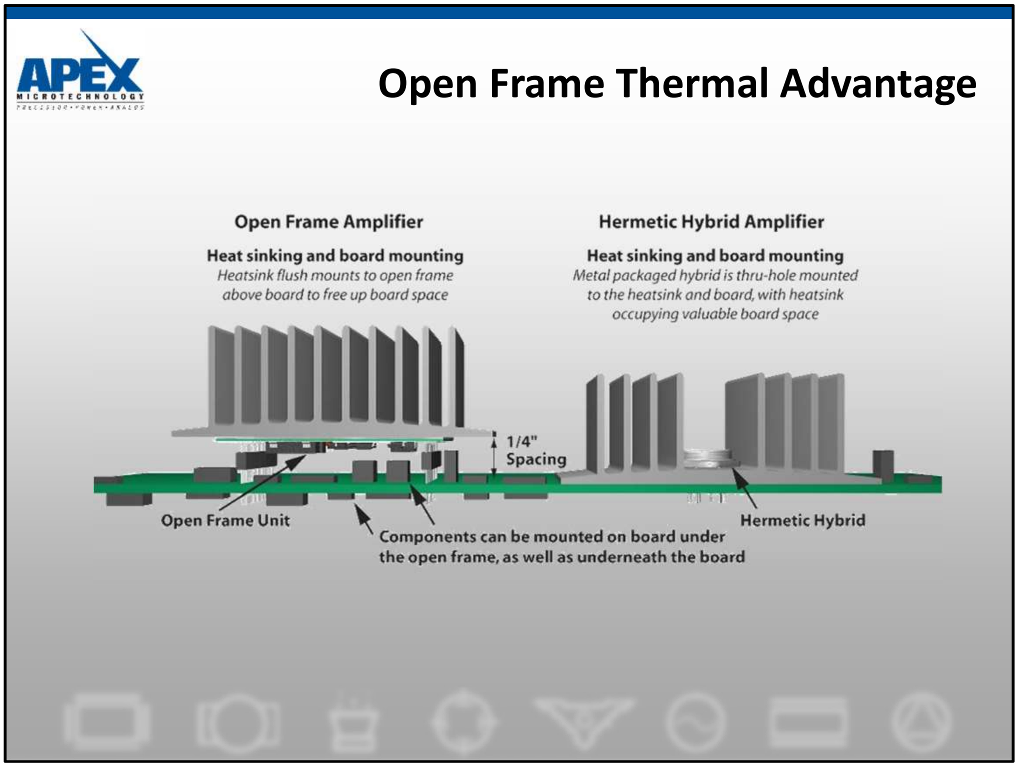


Properly applied grease results in good thermal performance. The operator variable shown above leaves the central area (where the heat is developed) with a high thermal path which led to amplifier destruction. Another variable to watch for is separation of the liquid from the solids in the grease. Too high a percentage of either can result in amplifier destruction due to thermal or mechanical stress. Buying thermal grease in a can or jar rather than a tube allows stiring to avoid the separation problem.

This slide also introduces the Apex failure analysis service. If you have a an elusive problem, call us. We'll attempt to solve it over the phone. Its always good to have a schematic handy you can fax. If appropriate, we'll give you an RMA (return material authorization) to start a failure analysis. We will:

1. Perform an external visual examination.
2. Test the part to all room temperature electrical specifications.
3. Delid and perform an internal visual.
4. Trouble shoot the circuit.

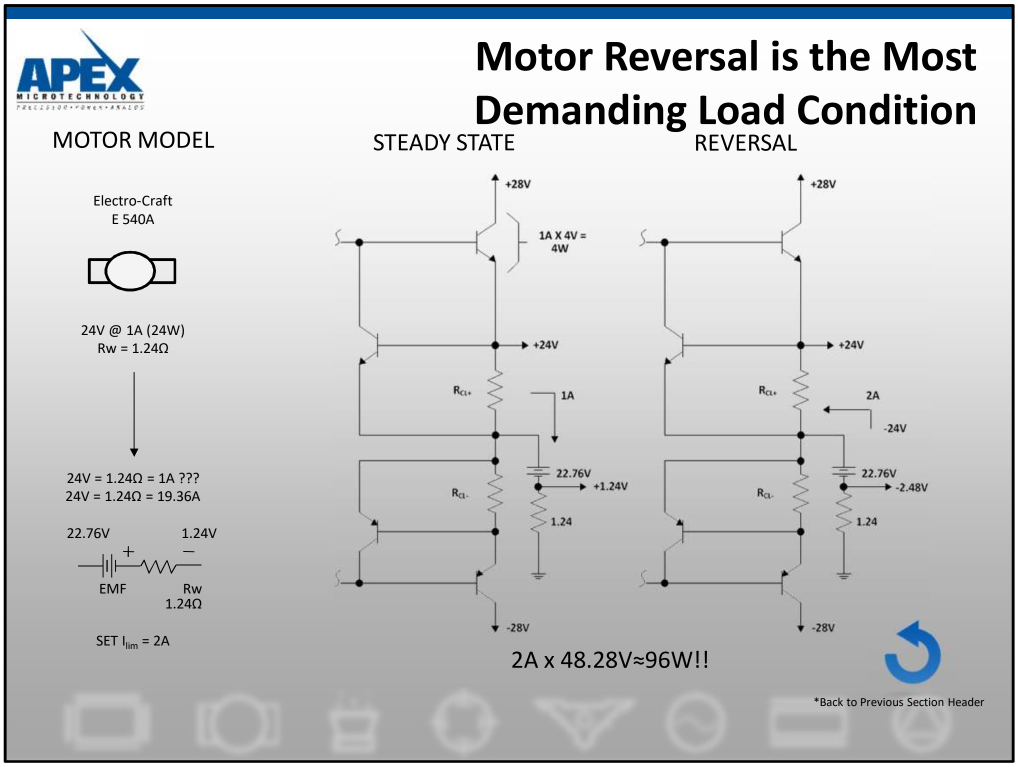
Many times the physical evidence helps pinpoint the problem. The location and nature of damage usually yields a suggestion on how to eliminate the problem.



With the Open Frame packaging style, there are significant thermal and mechanical advantages. Because the entire back side of the open frame is thermally conductive aluminum, any flat backed heatsink will do. We do not need to machine away the fins in order to accommodate the amplifier and there are no precision holes necessary for the pins to feed through.

Because the package of the open frame is larger, the thermal flux density of the heatsink can be reduced. In all, a smaller, lighter, and less expensive heatsink can be used with an Open Frame product compared to a hybrid with the same power dissipation.

Ref: AN11



A DC motor driven at 24V with 1A steady state current flow and a winding resistance specified at 1.24Ω can be modeled as a resistor in series with an EMF. In this example since the 1A drops 1.24V across the 1.24Ω, the remaining 22.76V is back EMF.

Under steady state conditions the motor voltage of 24V subtracted from the supply voltage of 28V leaves a 4V drop across the conducting transistor and a power dissipation of 4W.

When the amplifier is told to reverse the motor, the output of the amplifier attempts to go to -24V. If it could do so this -24V would add to the EMF of 22.76V to give -46.76V across the 1.24Ω resistor, resulting in a current flow of 37.71A. No way! Current limit is set at 2A.

When the current limit value of 2A flows across the winding resistance it drops 2.48V. The positive 22.76V of EMF is added to this negative 2.48V to give an output voltage of 20.28V. The difference between the output and the negative supply is now 28 -(-20.28) or 48.28V. That stress voltage on the conducting transistor means that the internal dissipation in the amplifier immediately after reversal is 48.28 volts * 2 amps or 96.56 watts!

This shows that a simple reversal can increase instantaneous power dissipation in the amplifier by over an order of magnitude. Judicious setting of current limiting and slowing the electrical response time will optimize reliability and mechanical response time.

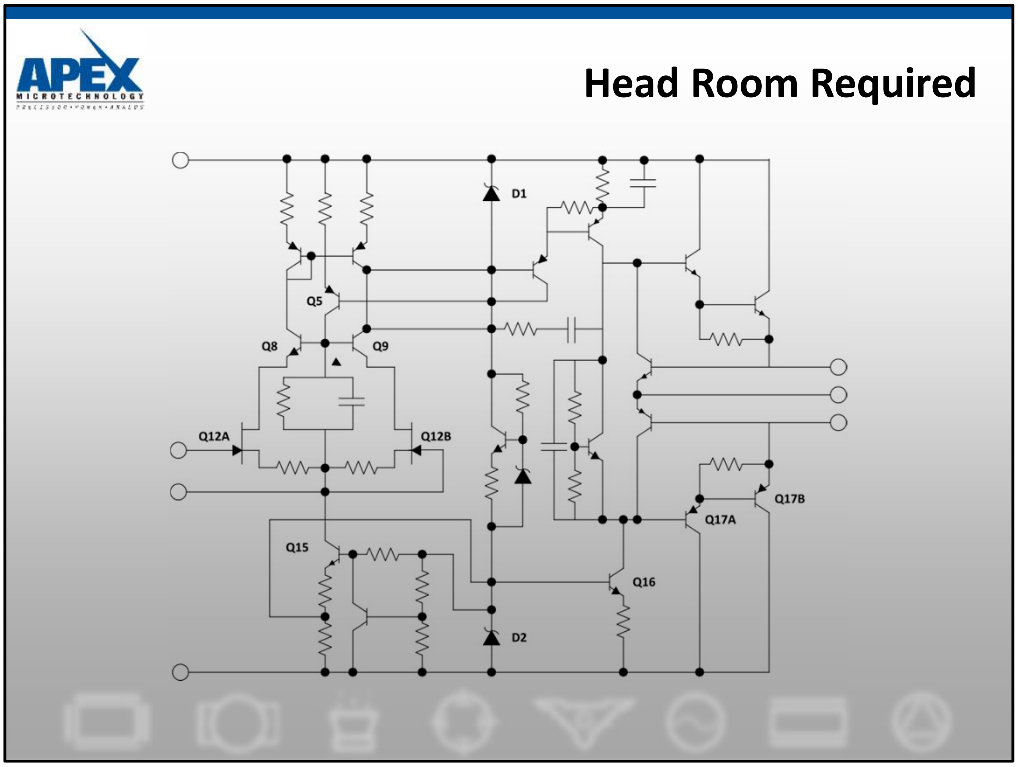
Ref. AN24


SINGLE SUPPLY OPERATION

Single Supply Operation

- Advantages
- Limitations
- Special Considerations

The basic operational amplifier has no ground pin. It assumes ground is the mid-point of the voltages applied to the +Vs and –Vs pin. If voltages on the input pins deviate from the assumed ground, it labels this deviation as common mode voltage. If this common mode voltage is within the op amp’s range and we don’t ask the output to go out of range, the op amp is happy.

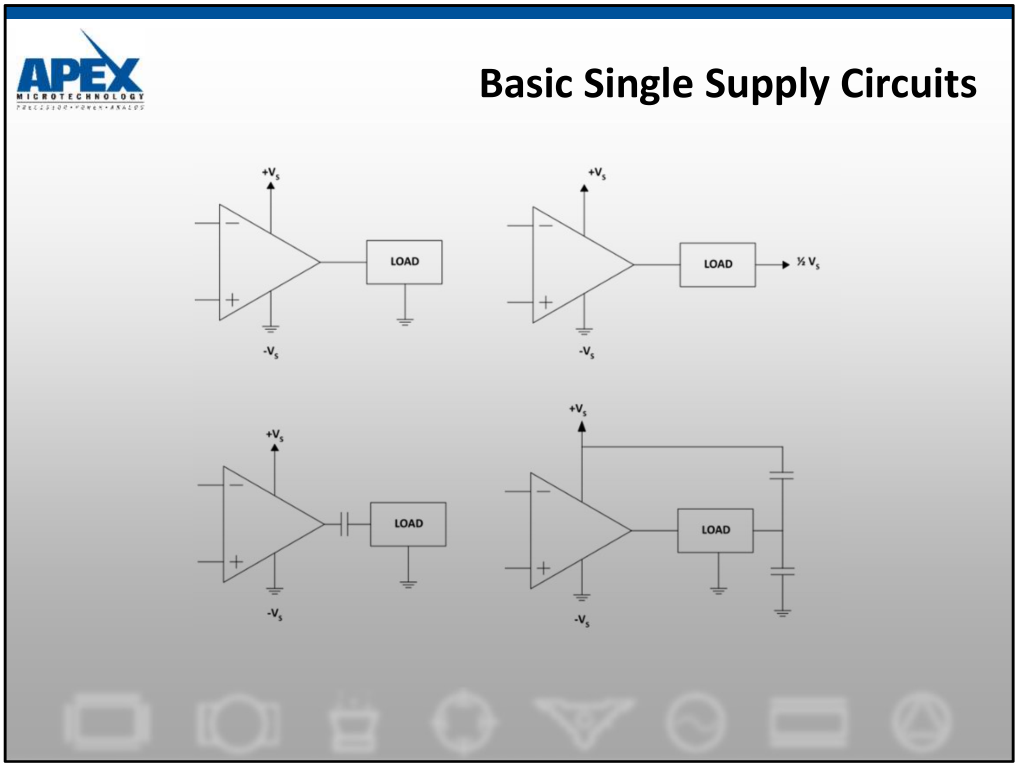


Notice that as the input pins approach the negative rail, the voltage across Q15 decreases. Minimum operating voltages for Q12 and Q15 along with the zener voltage place a limit on how close common mode voltage can get to the negative rail.

With inputs going positive Q5, Q8, Q9 and D1 place a similar limit on how close common mode voltage can get to the positive rail.

On the output side look at a fraction of the D2 zener voltage plus Q16 operating requirements and the Vbe of Q17 as all contributing to a limit of how close the output can approach the negative rail. This is the output voltage swing spec of the op amp. While this spec moves with output current, it never gets to zero even if current does. This means getting to zero output on a true single supply power op amp circuit is NOT going to happen.

While the actual voltages vary a lot, these type limitations are typical of all linear power amplifier output stages and most input stages. The Apex PA21, PA25 and PA26 family is an exception on the input side; common mode input goes below the negative supply rail making them ideal for some moderate power single supply applications.



Circuit A is only suitable for unipolar and non-zero inclusive drives. These type applications might include Programmable Power Supply (PPS), heater controls and unidirectional speed controls.

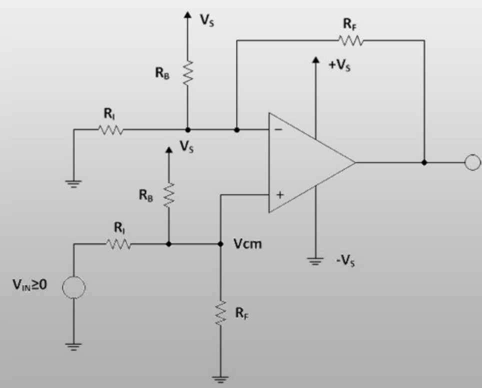
Circuit B is practical only when the power supply has a mid-point capable of bidirectional current flow such as a stack of batteries. Even this is can be a problem due to battery impedance being in series with the load.

Circuit C is reasonably common in the audio world. Circuit D is sometimes used to reduce turn-on pops but must be matched to input signal circuits to be of much use.

Ref. AN21

Single Supply

Non-Inverting Configuration



$V_o = \frac{Rf}{Ri}$

For $V_{in} = 0$

$V_{cm} = \frac{Vs\,(\frac{Ri}{Rf})}{Rb + (\frac{Ri}{Rf})}$

$V_{cm\Delta} = \frac{V_{in}\,(\frac{Rb}{Rf})}{Ri + (\frac{Rb}{Rf})}$

For $V_{in} > 0$

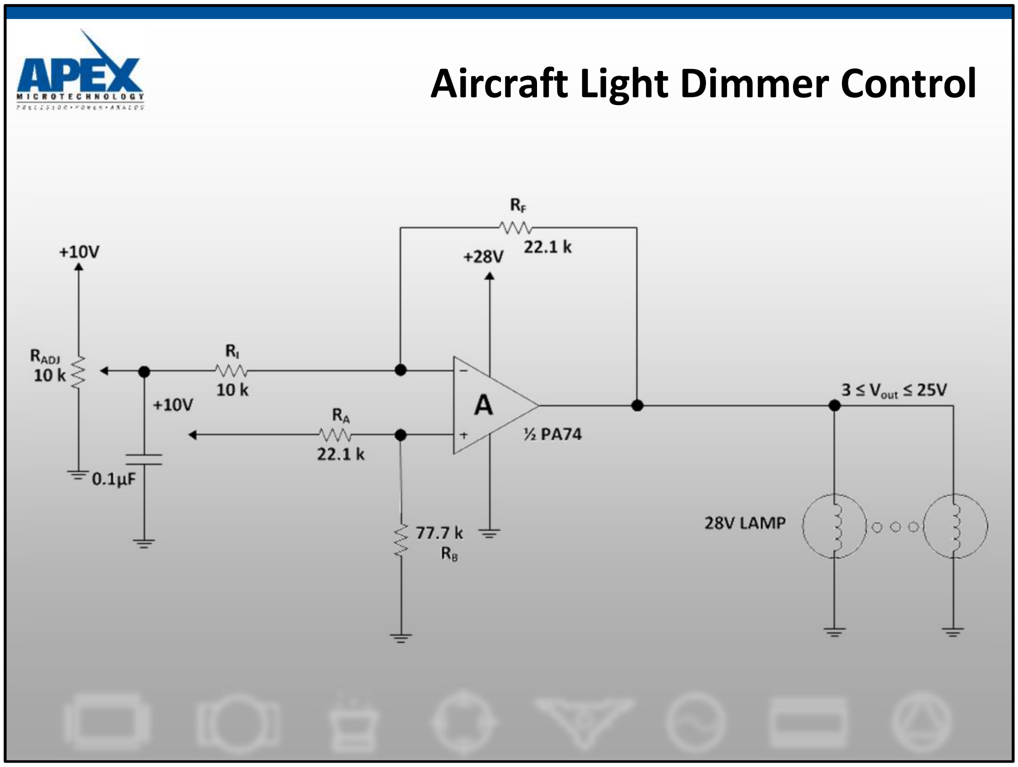
$V_{cm} = V_{cm\ (@\ Vin=0)} + V_{cm\Delta}$

This configuration can easiest be viewed as a differential amplifier with an offset voltage summed in on both + and - input nodes. With this arrangement of resistors the transfer function is: Vout = Rf/Ri Vin.

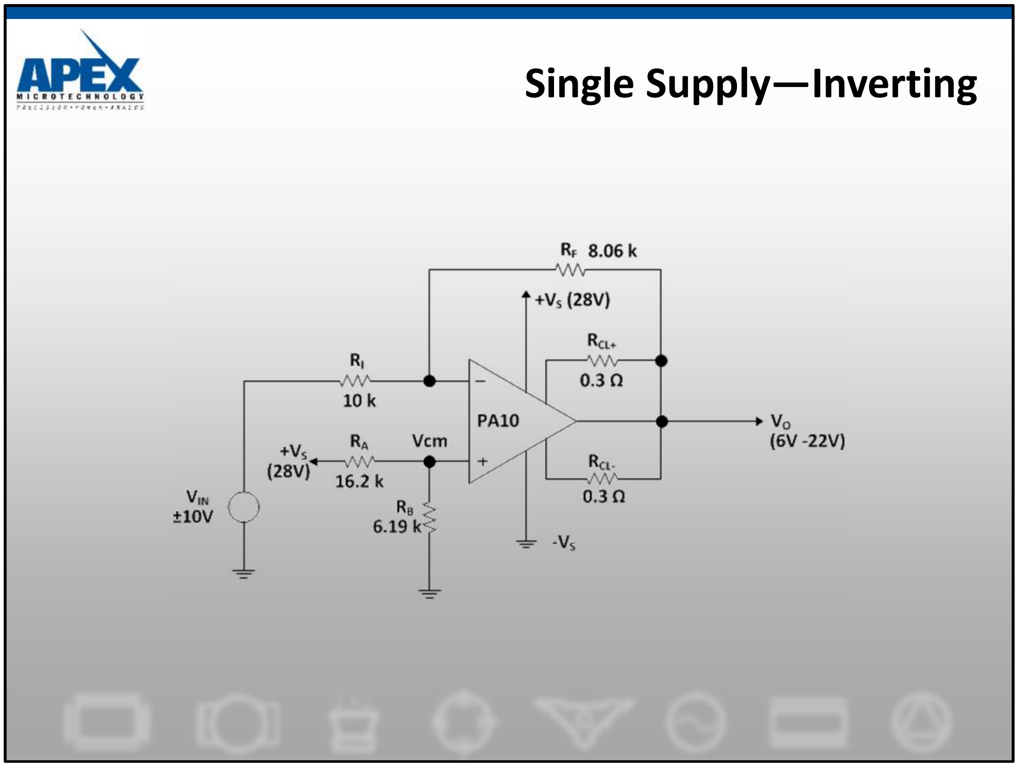
Rb acts as a summation resistor to force the common mode voltage on the power op amp input to be within the common mode voltage specification. When Vin = 0, Vcm = ƒ(Vs*(Ri/Rf)//Rb + (Ri/Rf)). As Vin becomes greater than zero, one can easily calculate the change in common mode voltage using superposition. VcmΔ = ƒ(Vin*(Rb/Ri)//Ri+(Rb/Rf)). Adding these two functions produces Vcm for Vin>0. Always check Vcm for entire range of Vin to guarantee common mode range compliance and thereby linear operation of the power op amp.

Inverting operation is actually easier. Simply move the signal source to the -side and ground the +side Ri. Vcm is set up in the same manner as above but there is no VcmΔ to worry about at all. Since Ri and Rf will both go to ground, they could be replaced with a single resistor. For best accuracy keep two individual resistors; your are likely to get better ratios and tracking from +side to -side. Speaking of accuracy, model any current mismatch through the two Rb resistors as flowing through Rf producing an output error. Realize also that most current through Rb flows through the signal source producing an input error if the signal source is not zero impedance.

Ref. AN21



Accurate brightness control is provided in this aircraft panel light control circuit. A bank of several parallel connected lamps is driven by the PA74 which operates in a closed loop with a command voltage from a low power 10-turn pot. Offset is summed into the noninverting input of the PA74 to allow a zero to 10V input command on the inverting input to be translated into a 3 to 25V output voltage across the lamps. The 3V allowance for saturation voltage on the output of the PA74 assures an accurate low impedance output at 2.5 amps. The advantage of two power op amps in one package provided by the PA74 allows the design engineer to control two independent dimmer channels from one TO-3 power op amp package. The open loop gain of the PA74, along with its power supply rejection, force a constant commanded voltage across the lamps and thus a constant brilliance regardless of power supply line fluctuations, typical in an aircraft from 16 to 32 volts.



GIVEN: Vs= 28V **STEP 3:** Offset: Set Vin =0, Vo=14V

Vin = ± 10V Vo= -Vin(Rf/Ri) + {(Vs*Rb)/RA+RB)}

{1+(Rf/Ri)}

Vo = 6V 22V

FIND: Scaling resistor values 14V = 0+ (Rf/Ri) + {28

*RB)/(RA+RB)} {1+0.8}

SOLUTION: RB/(RA+RB) = 0.278   RA= 2.6 RB

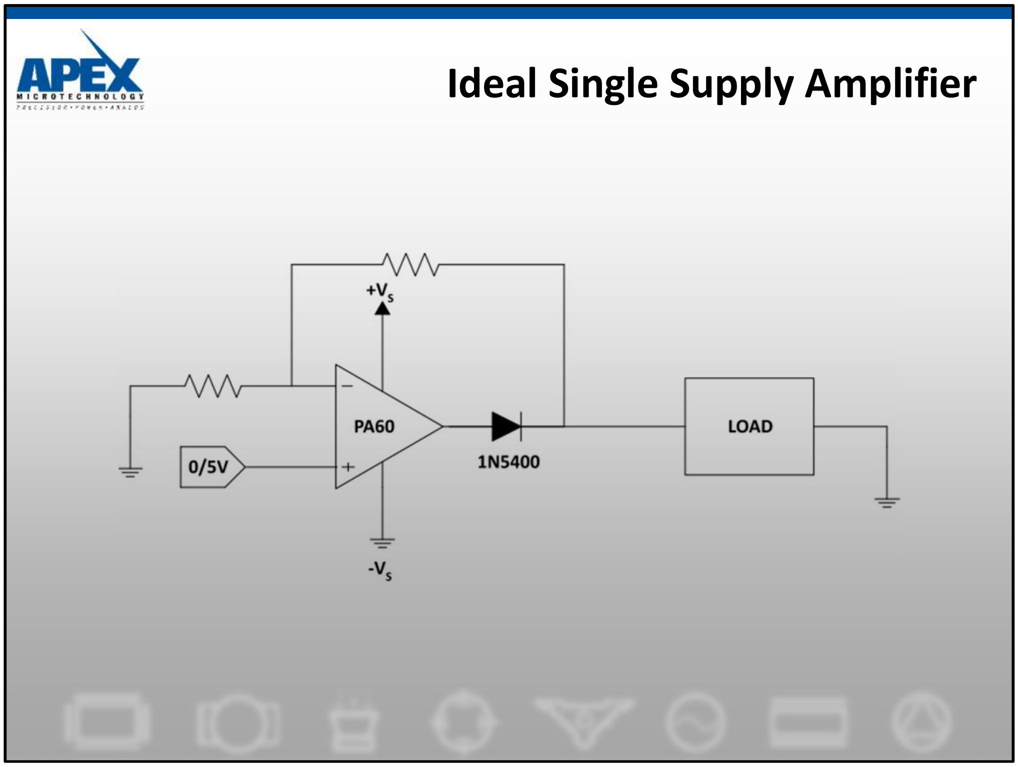
STEP1: Gain = (Rf/Ri)   Offset = {(Vs*RB)/(RA+RB)} {1+(Rf/Ri)}

STEP2: Gain = (Vo p-p)/(Vin p-p) = 16V/20V = 0.8

STEP4: For minimum offset set RA||RB = Ri||Rf

Choose RA = 16.2K, RB = 6.19K

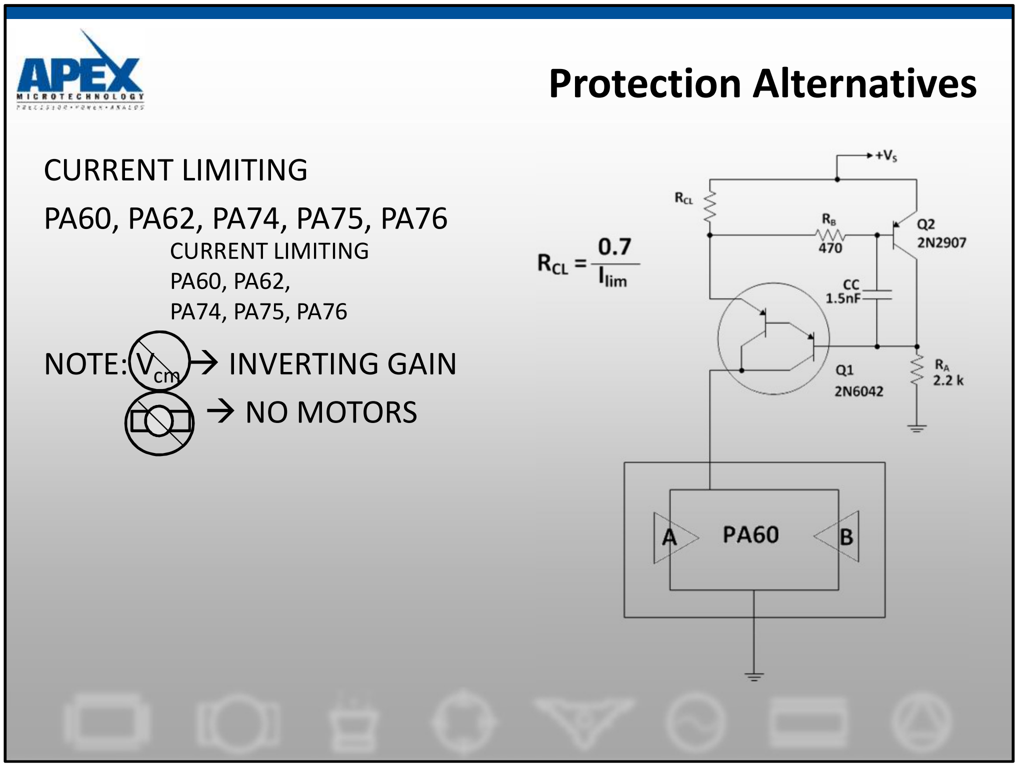
STEP5: Check for common mode: Vcm = 28 RB/(2.6RB+RB) = 7.78V (>6V   OK)



The PA60 series amplifiers feature a common mode voltage range from 0.3V below the negative supply rail (ground in this case) to with in 2V of the positive rail. These amplifiers also swing to about 0.5V of the rail with very light loads making the diode level shifter above quite practical as long as the load is resistive. With the diode inside the feedback loop it contributes essentially no errors at the load.

The non-inverting circuit shown is the most common but grounding the +input and using the -input in the normal summing junction fashion will work just as well.

Ref. PA60 DATA SHEET



This handy circuit can be used with the PA60 series amplifiers in a single supply application to provide external current limit with minimum components.

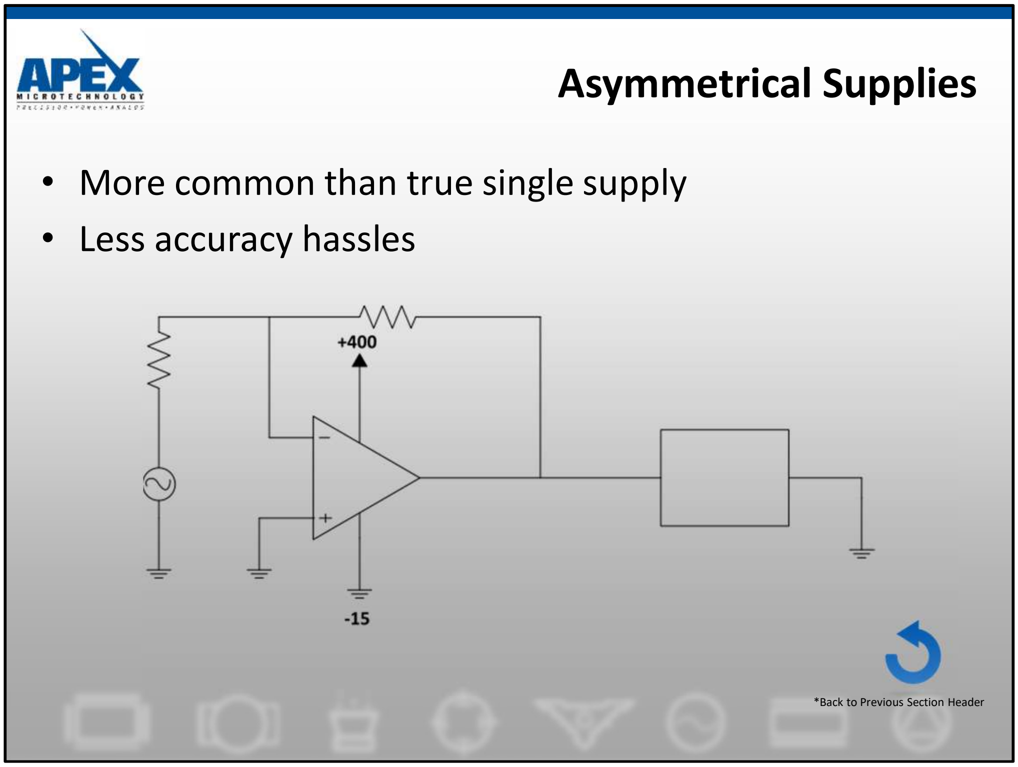
By lowering the PA60 current limit one can keep the operating conditions of the PA60 within its SOA.

Q1 is the series pass element providing voltage to the PA60. During current limit we will limit the current to the load by reducing the supply rail. Ra provides a constant biasing current to the base of Q1. When the current through Q1 is sufficient enough to develop a .7V drop across Rcl Q2 turns on and starts to turn off Q1 until current into the PA60 drops below Ilim = .7V/Rcl. Rb and Cc insure the stability of the current limit circuit.

To avoid common mode violations on the input to op amp A and op amp B, as the supply rail is lowered during current limit, it is important to configure both op amp A and op amp B in an inverting gain configuration.

The maximum additional drop through the current limit circuit is 1.7V at up to 3A. This will reduce the maximum output voltage swing available from the PA60.

In a split supply application the negative current limit circuit would replace Q1 with a 2N6045 and Q2 with a 2N2222.



There’s something very appealing about a circuit with only two gain setting resistors. Many times there is already a low voltage supply in the system just waiting to be used. This supply need only provide quiescent current of the op amp unless the op amp swings negative or in the case of reactive loads where current and voltage are not in phase.

There is nothing magic about having a high positive supply and a low negative supply. As long as the lower voltage supply satisfies the common mode voltage requirement it makes no difference if you turn things over using high negative and low positive. If you are allowed to reverse the load terminals, this could work to significant advantage. Say that the small signal portion of the system runs on +12V or +15V and you need to buy a high power supply to drive the load anyway. If you set up a negative high power rail, the existing low power supply will work fine

STABILITY AND COMPENSATION

Stability and Compensation

- Ground Loops
- Supply Loops
- Local Internal Loops
- Coupling: Internal and External
- Aol Loop Stability

Eliminate Coupling

Internal and External

- Ground the Case
- Reduce Impedances
- Eliminate I_b Compensation Resistor on +IN
- Don’t Run Output Traces Near Input Traces
- Run I_{out} Traces Adjacent to I_{out} Return Traces

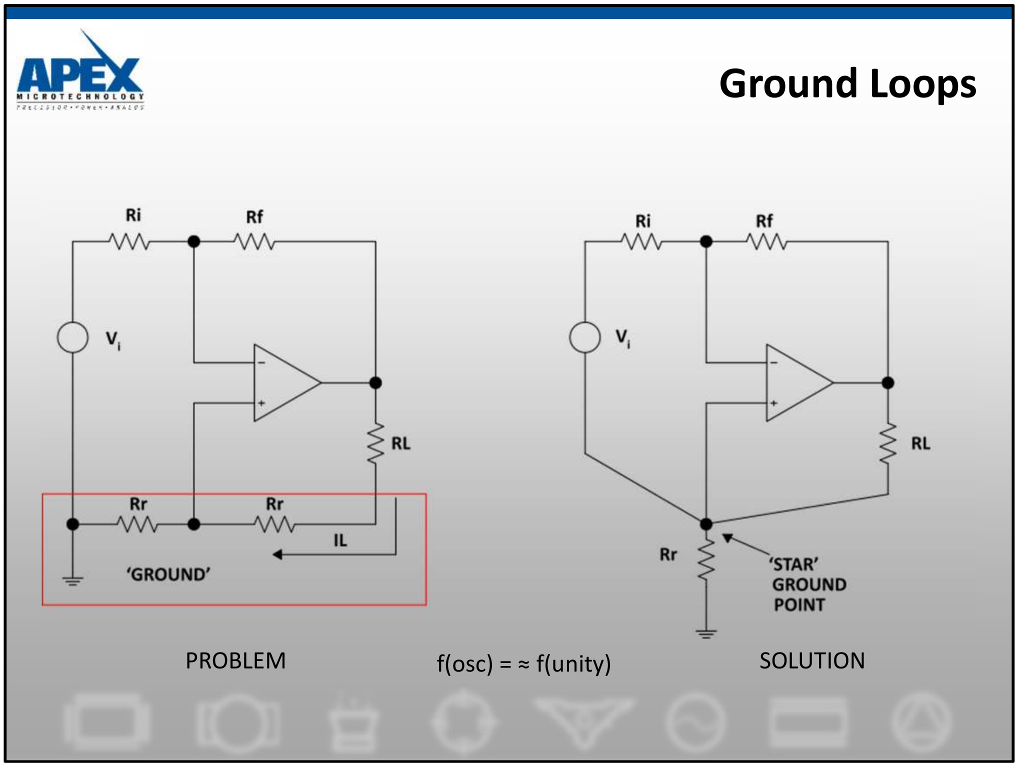
1. Grounding the case forms a Faraday shield around the internal circuitry of the power amplifier which prevents unwanted coupling from external noise sources.
2. Reducing impedances keeps node impedances low to prevent pick-up of stray noise signals which have sufficient energy only to drive high impedance nodes.
3. Elimination of the Ib compensation resistor on the +input will prevent a high impedance node on the +input which can act as an antenna, receiving unwanted noise or positive feedback, which would result in oscillations. This famous Ib compensation resistor is the one from the +input to ground when running an amplifier in an inverting gain. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. Modern op amps feature compensated input stages and benefit very little from this technique.

Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of this resistor. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave this +input bias resistor out and ground the +input if possible. If the resistor is required, bypass it with a 0.1µF capacitor to ground.

4. Don't route input traces near output traces. This will eliminate positive feedback through capacitive coupling of the output back to the input.

5. Run Iout traces adjacent to Iout return traces. If a printed circuit board has both a high current output trace and a return trace for that high current , then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form an equivalent twisted pair by virtue of their layout. This will help cancel EMI generated from outside from feeding back into the amplifier circuit.

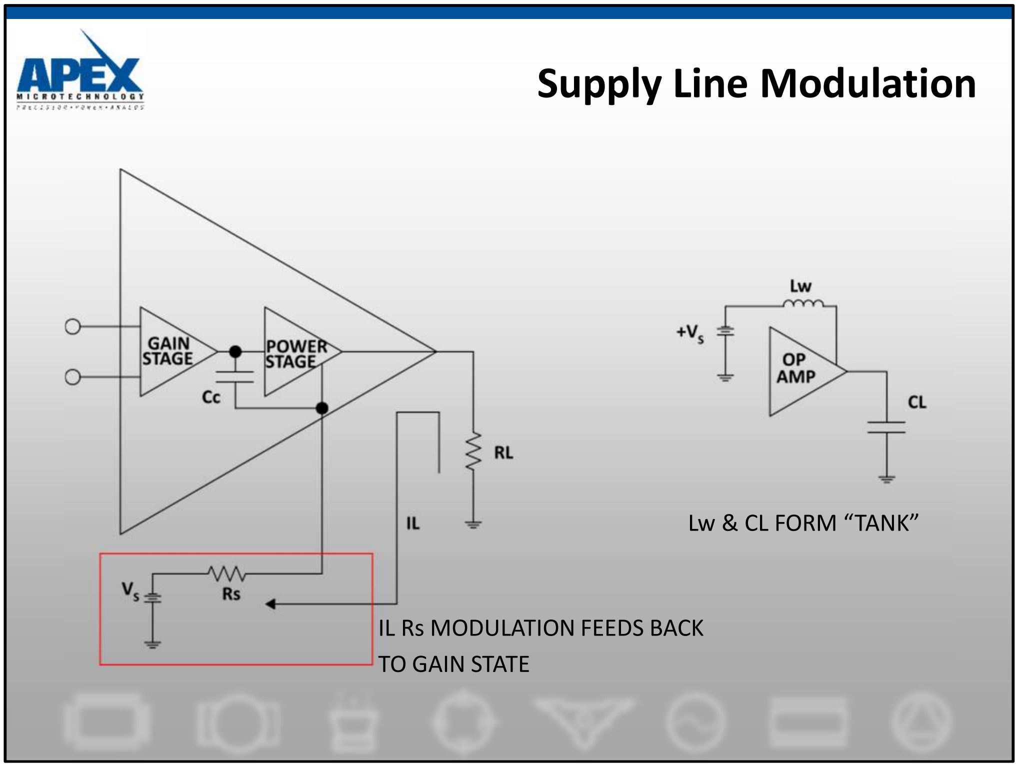
1. Ref. AN1 STABILITY, AN19



Ground loops come about from load current flowing through parasitic layout resistances, causing part of the output signal to be fed back to the input stage. If the phase of the signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (Rr) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier. This is done by the use of a star ground point approach.

The star point is merely a point that all grounds are referred to, it is a common point for load ground, amplifier ground, and signal ground. The star ground point needs to be a singular mechanical feature. Run each connection to it such that current from no other part of the circuit can mingle until reaching the star point. Don't forget your star point when making circuit measurements. Moving the ground lead around may change the indication leading to false assumptions about circuit operation.

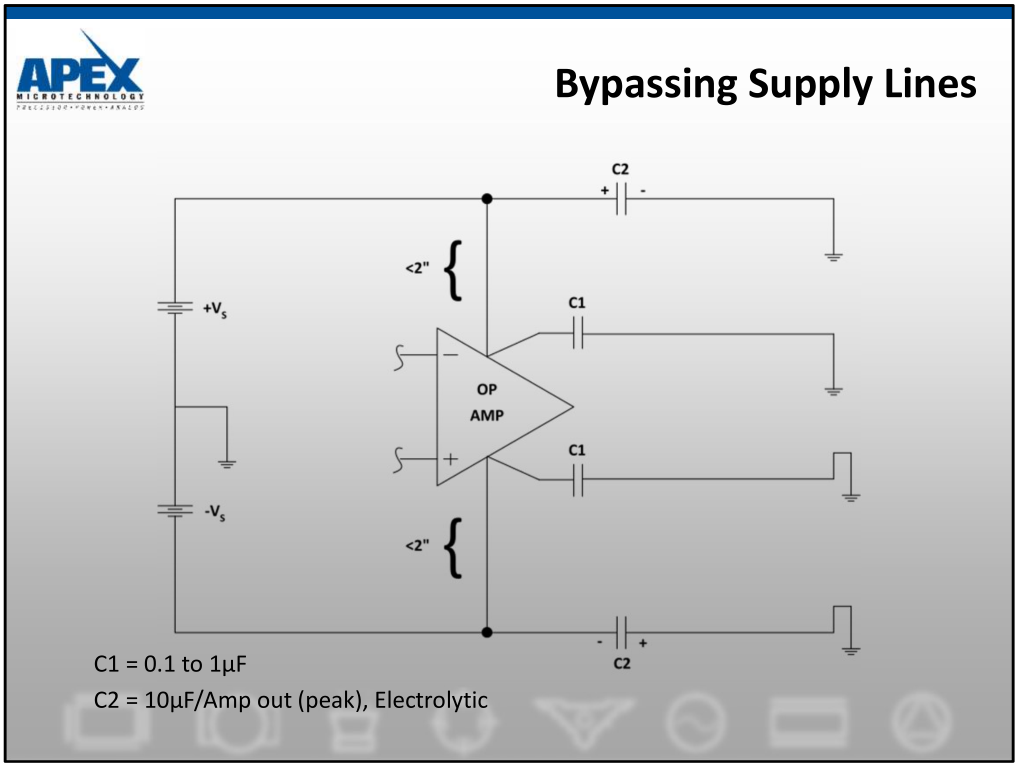
Ref. AN1 STABILITY, AN19



Supply loops are another source of oscillation. In one form of power supply related oscillations the load current flowing through supply source resistance and parasitic trace resistance modulates the supply voltage seen at the power supply pin of the op amp. This signal voltage is then coupled back into a gain stage via the compensation capacitor which is usually referred to one of the supply lines as an AC ground.

Another form of oscillatory circuit that can occur is due to parasitic power supply lead inductance reacting with load capacitance to form a high Q tank circuit.

Ref. AN1 STABILITY, AN19

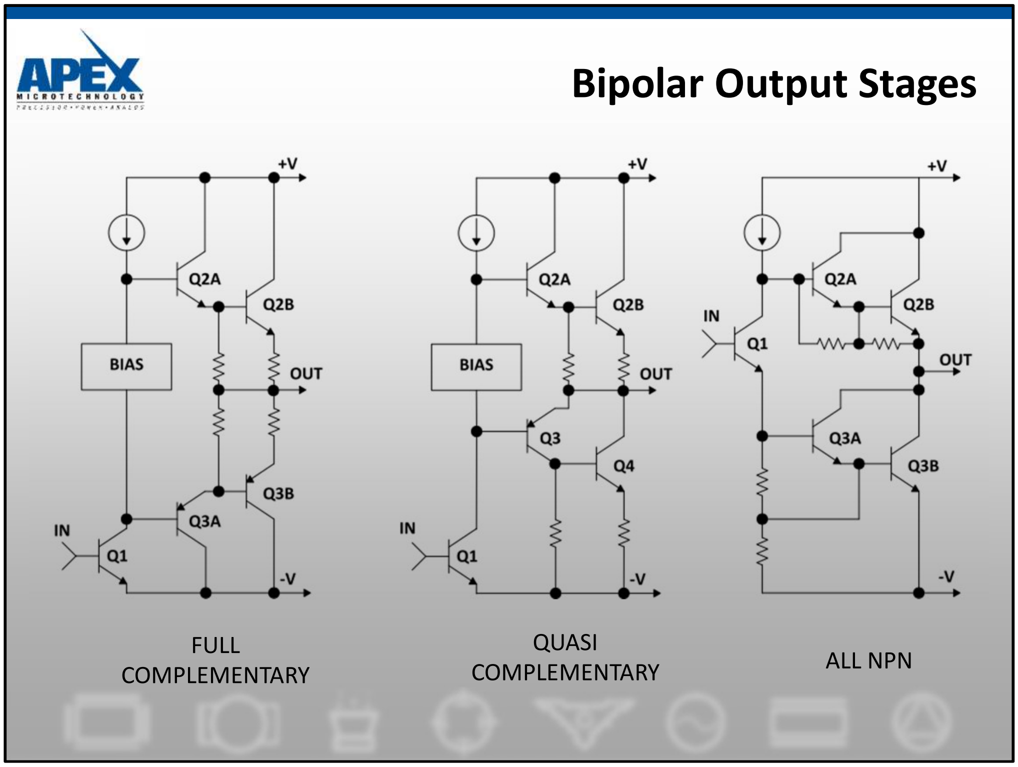


All supply line related oscillation and coupling problems can be avoided with proper bypassing.

The "must do" in all bypassing is a good high frequency capacitor right at each amplifier or socket power supply pin to ground. Not just any ground but the star point ground. This will most often be a multilayer ceramic, at least 1000pF, and as large as possible up to about 1µF. Above that capacitance high frequency characteristics shouldn't be taken for granted. Polysterene, polypropylene, and mylar are possible alternatives when ceramics cannot be used for any reason. Check the manufacturer’s data sheet for low ESR at least two times the unity gain bandwidth of the op amp being used.

Once high frequency bypassing is addressed, additional low frequency decoupling is advisable. In general use about 10µF/amp of peak output current, either electrolytic or tantalum type capacitors.

Ref. AN1 STABILITY, AN19

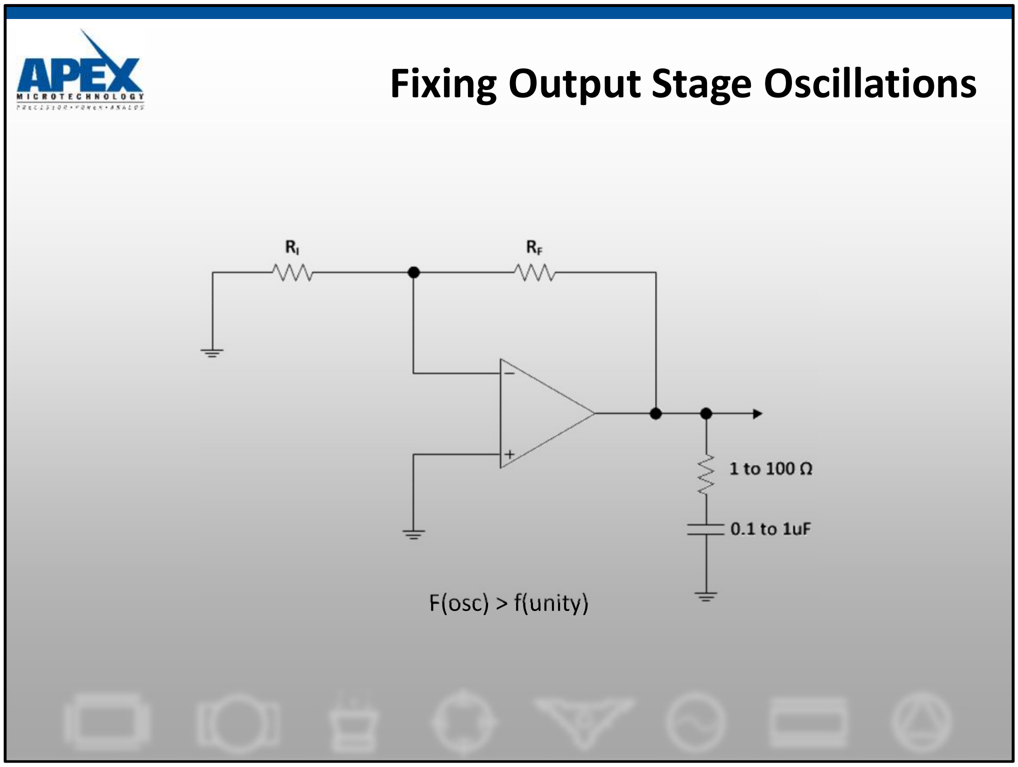


The full complementary output stage is a very easy to use stage. It exhibits symmetric output impedance and low crossover distortion. It is also easy to bias and is inherently stable under most load conditions. Q1 acts as a class A, high voltage gain, common emitter amplifier. Its collector voltage drives the output darlingtons. The bias circuitry provides class AB operation for the output darlingtons, minimizing crossover distortion. Both Q2 and Q3 are only called upon to provide impedance buffering. This is a unity voltage gain, high current gain stage. Both devices are operated as followers and thus provide very low output impedance for either sinking or sourcing current. Monolithic designers are constrained to work with NPN's for handling high currents. For this reason, the "all-NPN" output stage, followed by the "quasi-complementary" output stage were developed.

The quasi-complementary is similar to the full complementary in that Q1 again acts as a class A, common emitter, high gain amplifier and the output devices provide impedance buffering only. Q2 provides the same function as Q2 in a full complementary approach. Q3 and Q4 form a "composite PNP". The inherent problem with this approach is that there is heavy local feedback in the Q3, Q4 loop and this can lead to oscillations driving inductive loads.

The "all-NPN" output stage was an early approach to delivering power in a monolithic. During current source this stage operates much the same as the previous two. The major difference comes about during current sink. During the current sink cycle Q1 changes from a common emitter to an emitter follower. It now provides base voltage drive for Q3. Q3 is operated as a common emitter amplifier. The major disadvantage to this approach is the large changes in both output impedance and open loop gain between source and sink cycles. A problem common to both the quasi-complementary and the all NPN stage is the difficulty of biasing properly over extended temperature range.

Ref. AN1 STABILITY, AN19

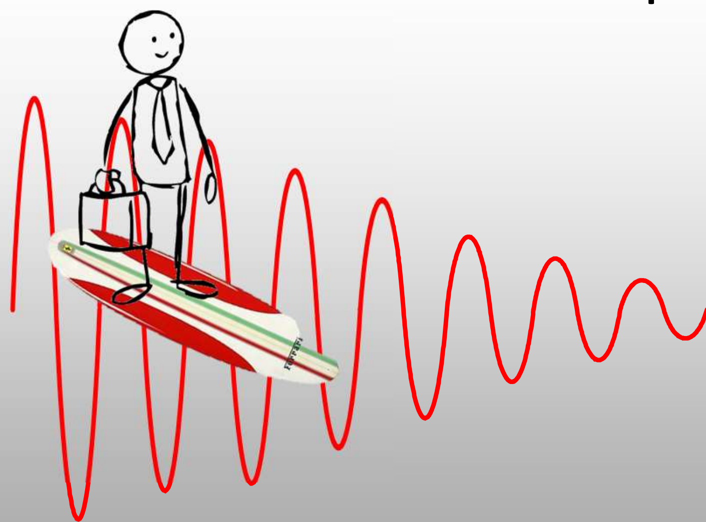


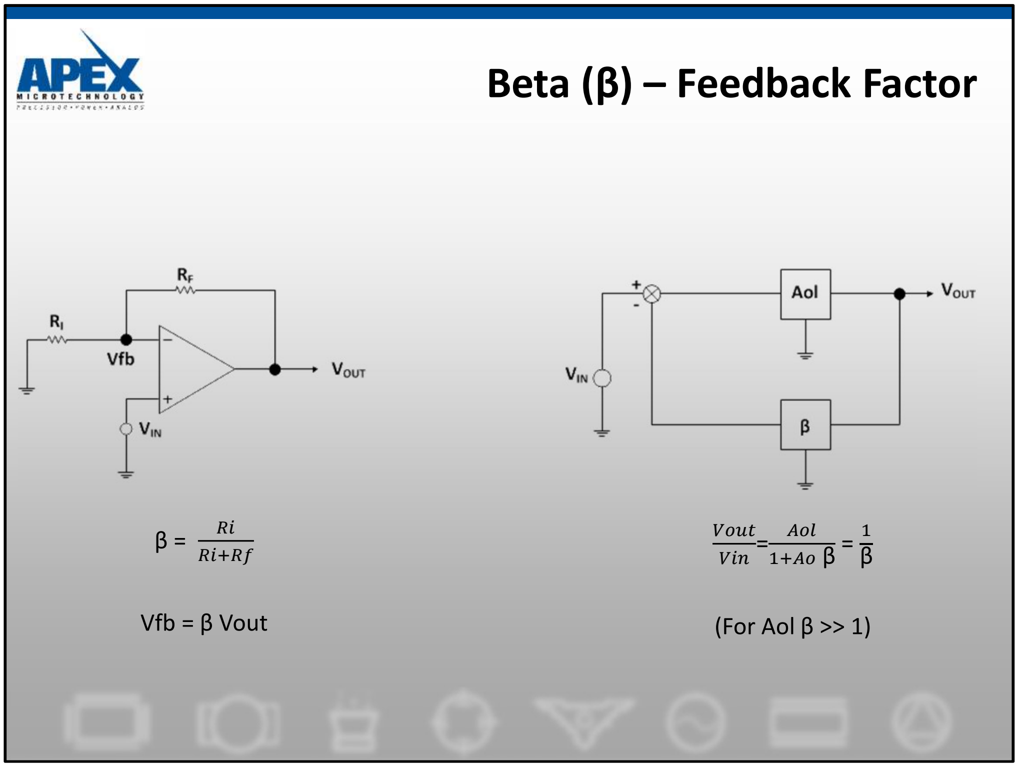
Any time you encounter an oscillation above the unity gain bandwidth of the amplifier it is bound to be one of the output stage problems discussed previously. These can be fixed through the use of a simple “snubber” network from the output pin to ground. This network is comprised of a resistance of from 1 to 100 ohms in series with a .1 to 1 uF capacitor. This network passes high frequencies to ground, thus preventing it from being fed back to the input.

Some manufacturers who use all NPN output stages in their monolithic power amplifiers suggest the use of this type of network to reduce output stage oscillations. Other manufacturers, while having a similar problem, never suggest that this type of network is necessary for proper use. Apex either takes care of the problem internally or specifies specific values for the external network.

Ref. AN1 STABILITY, AN19

Loop Stability





$$Vfb = \frac{Vout*Ri}{Ri+Rf} \qquad Vout = Vin\ Aol - Aol\ \beta\ Vout$$

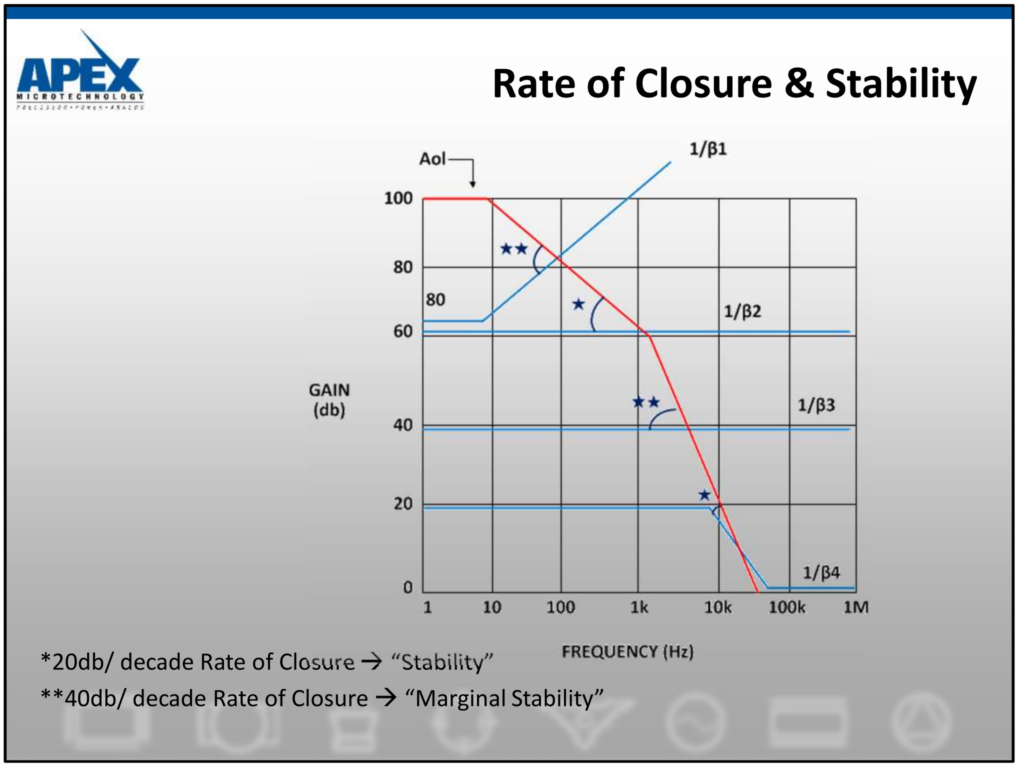
$$Vfb = \beta\ Vout \qquad Aol = \frac{Vout*Aol\beta}{Vout*Vin}$$

$$\beta = \frac{Ri}{Ri+Rf} \qquad \frac{Vout}{Vin}=\frac{Aol}{1+Aol\beta}=\frac{1}{\beta}$$

Control theory is applicable to closing the loop around a power op amp. The block diagram above in the right consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the β represents the feedback network. The value of β is defined to be the fraction of the output voltage that is fed back to the input. Therefore, β can range from 0 (no feedback) to 1 (100% feedback).

The term Aolβ that appears in the Vout/Vin equation above has been called loop gain because this can be thought of as a signal propagating around the loop that consists of the Aol and β networks. If Aolβ is large there is lots of feedback. If Aolβ is small there is not much feedback (for a detailed discussion of this and other useful topics related to op amps refer to: Intuitive IC Op Amps, Thomas M. Frederiksen, National's Semiconductor Technology Series, R.R. Donnelley & Sons).

Ref. AN19

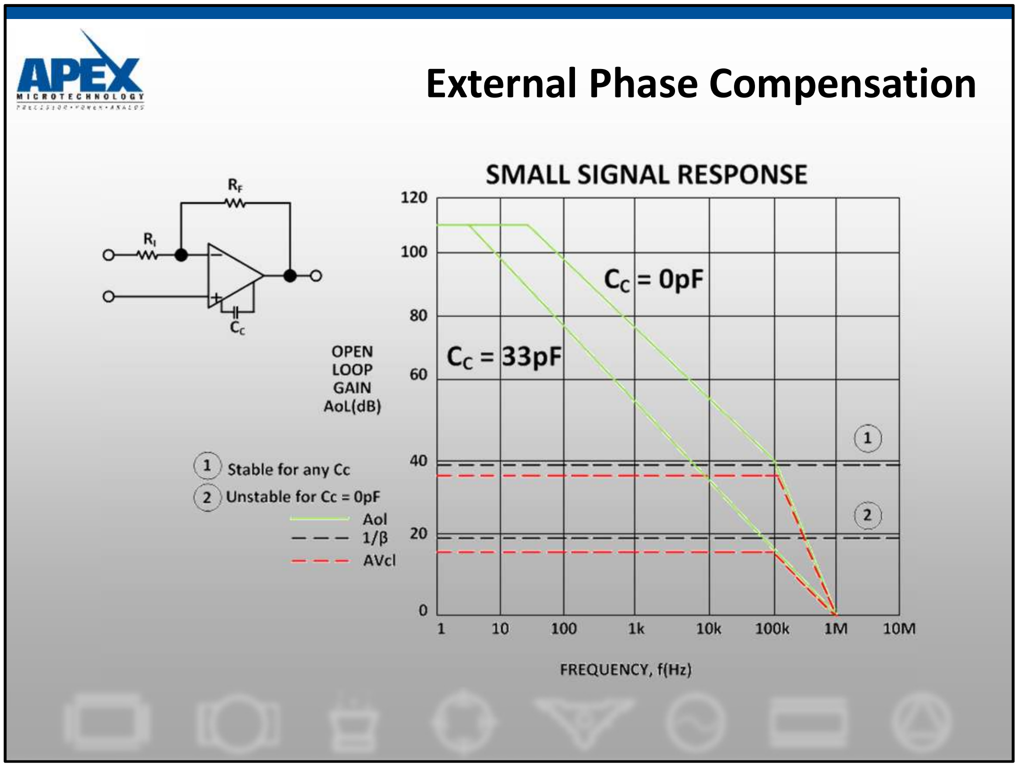


Aol is the amplifier's open loop gain curve. 1/β is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/β curve is the loop gain. Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure that when loop gain goes to zero, that is where the 1/β curve intersects the Aol curve, open loop phase shift must be less than 180 at the intersection of the 1/β curve and the Aol curve the difference in the slopes of the two curves, or RATE OF CLOSURE is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

A 40 dB per decade RATE-OF-CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Above examples indicate several different cases for both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

Ref. AN19, AN38

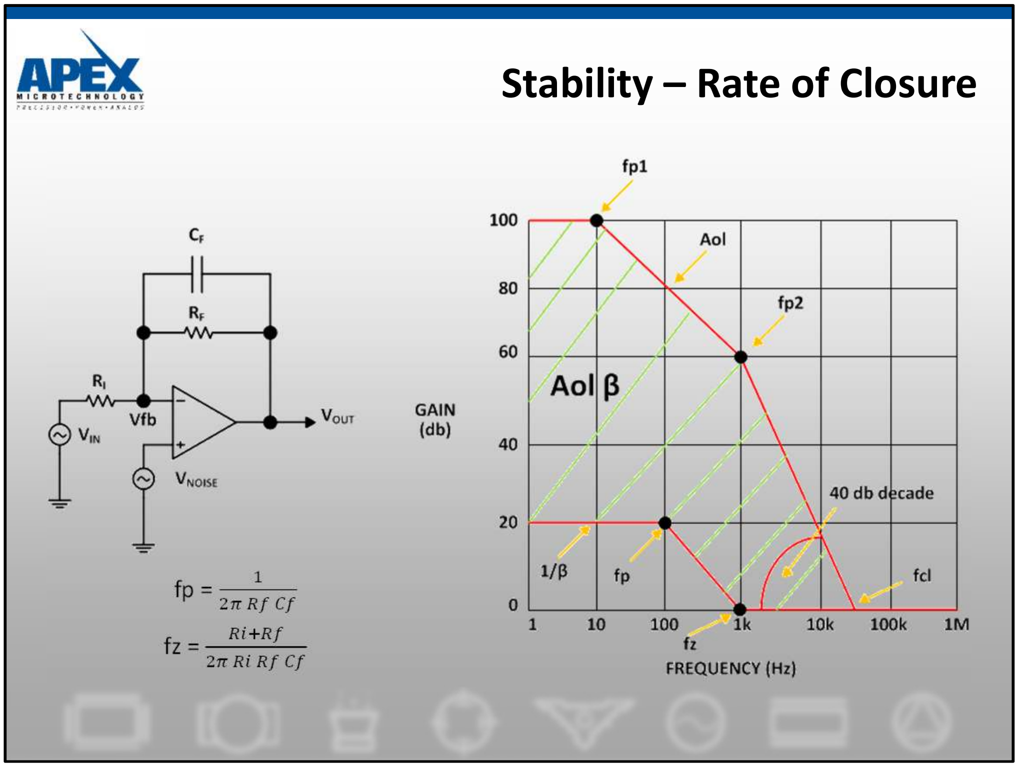


External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the amplifier. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of $I=CdV/dt$ that a lower value of capacitance will yield a faster voltage slew rate.

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In the figure above we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc=33pF to a two pole response with Cc=0pF. Curve 1 illustrates that for 1/β of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc=33pF or Cc = 0pF).

Curve 2 illustrates that for 1/β of 20 dB and Cc=0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc=0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

Ref. AN19, AN38



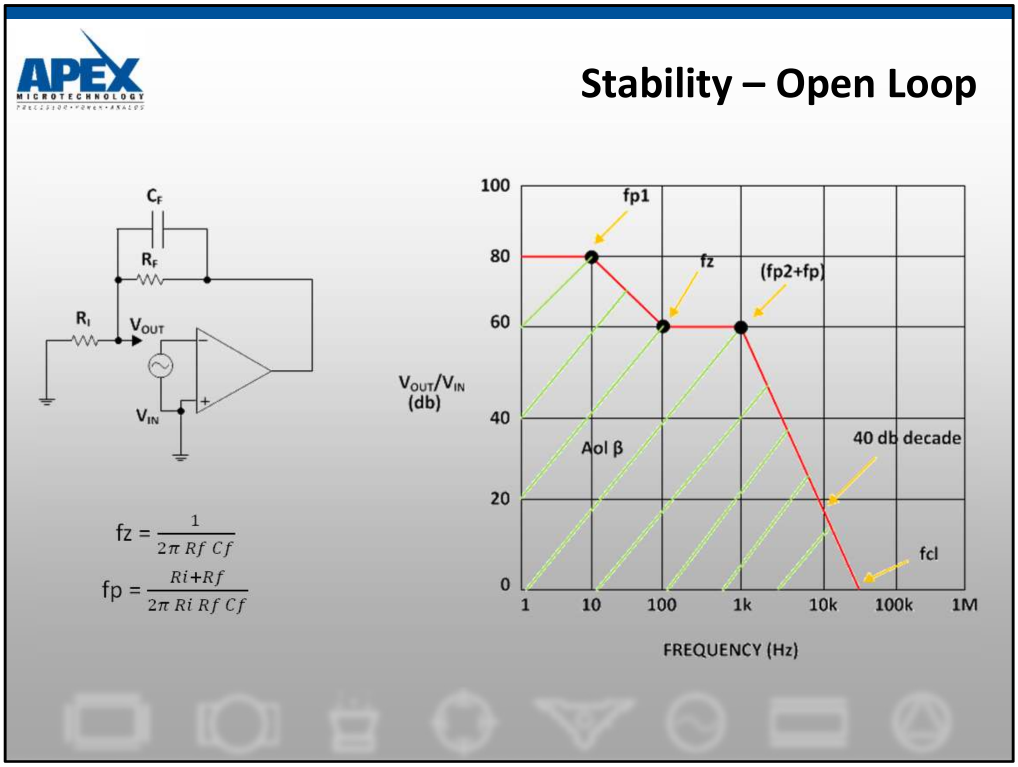
The example above shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional Vnoise voltage source shown at the + input of the op amp. This is shown to aid in conceptually viewing the 1/β plot.

An inverting amplifier, with its + input grounded, will always have potential for a noise source to be present on the + input. Therefore, when one computes the 1/β plot, the amplifier will appear to run in a gain of 1 + Rf/Ri for small signal AC. The Vout/Vin relationship will still be -Rf/Ri.

The plot above shows the open loop poles from the amplifier's Aol curve as well as the poles and zeroes from the 1/β curve. The locations of fp and fz are important to note as when we look at the open loop stability check we will see that poles in the 1/β plot will become zeroes and zeroes in the 1/β plot will become poles in the open loop stability check.

Notice that at fcl the RATE-OF-CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/β curve is labelled Aolβ which is also known as loop gain.

Ref. AN19, AN38

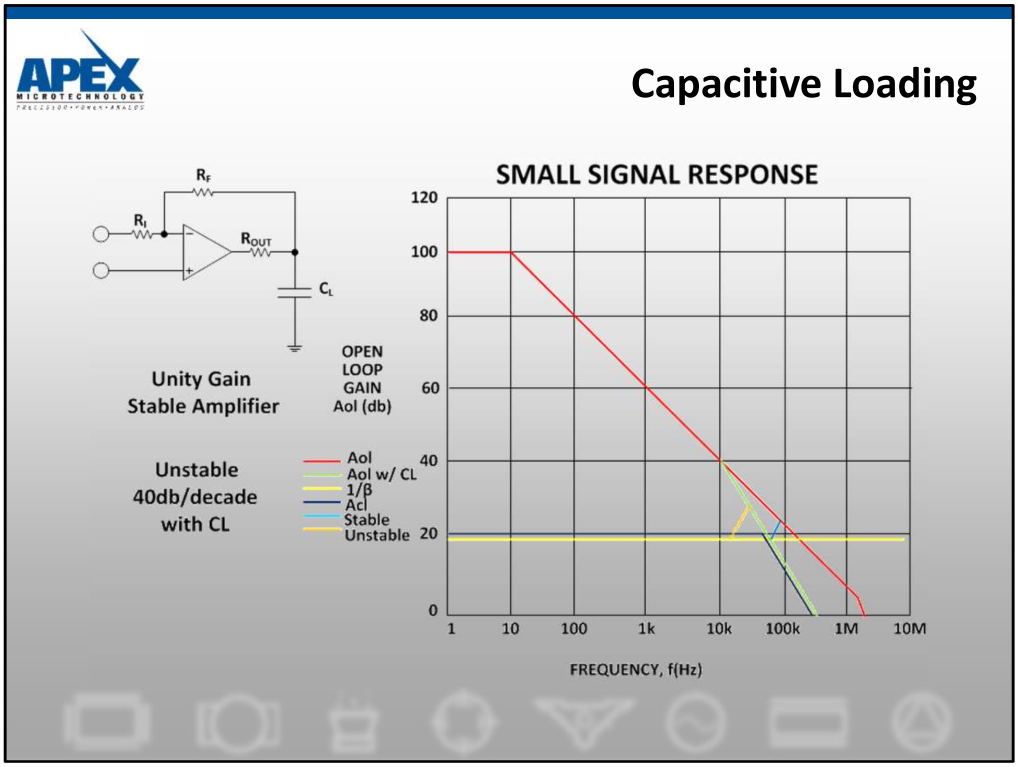


Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure that the open loop phase does not dip to -180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180 the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice that this open loop plot is a plot of Aol β. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/β plot became a pole in the open loop plot and the pole from the 1/β plot became a zero. We will use this knowledge to plot the open loop phase plot to check for stability. This plotting of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/β curve and the Aol curve.

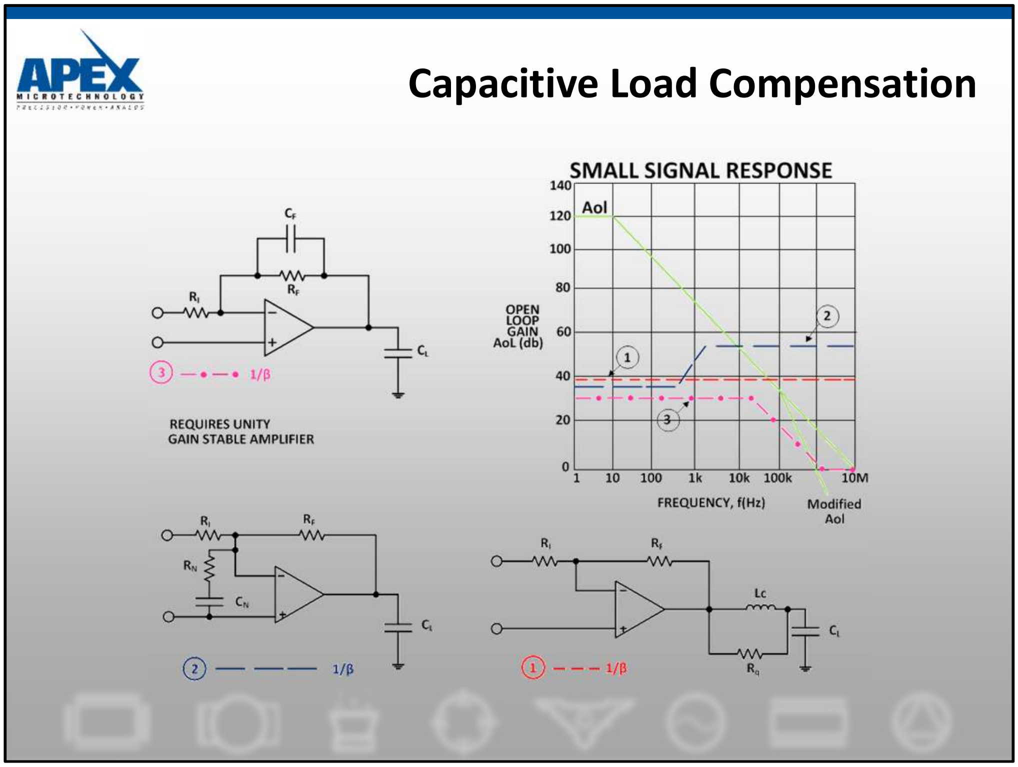
Ref. AN19, AN38



Even when using a unity gain stable amplifier, capacitive loads react with amplifier output impedance, which has the effect of introducing a second pole into the amplifier response which occurs below the unity gain crossover frequency.

If the amplifier is used at a low enough loop gain, this will result in the unstable condition shown in this graph. One simple solution is to increase the close loop again

Ref. AN19, AN25, AN38



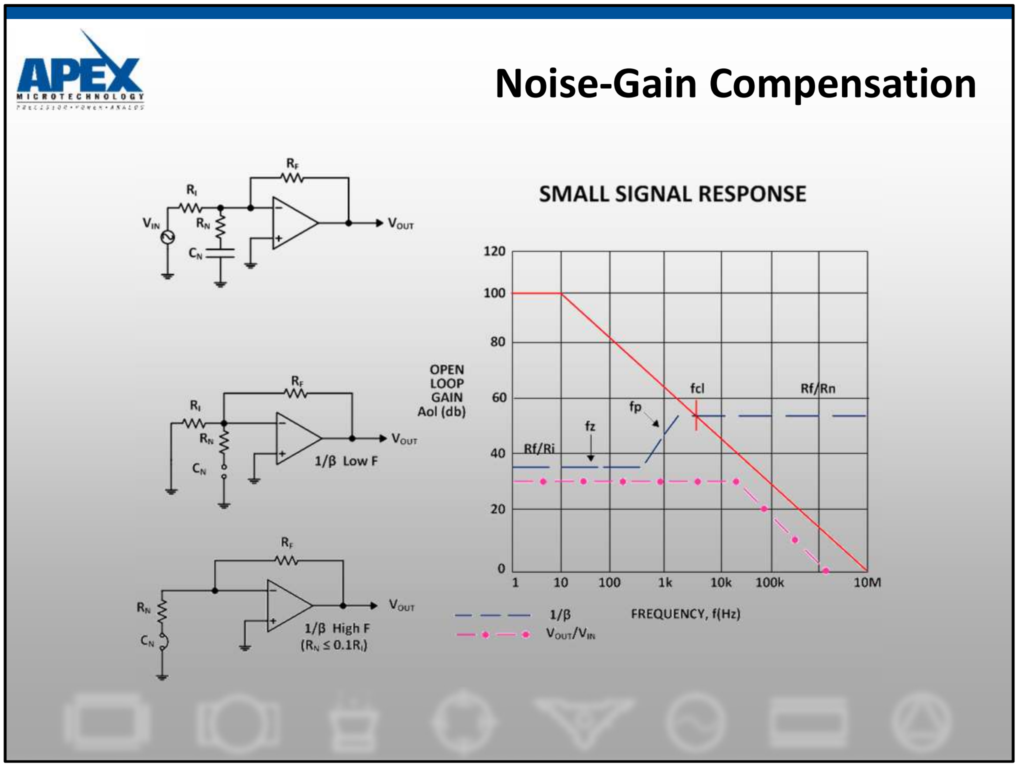
If it’s necessary to use low gains with capacitive loads, or in the unlikely event they are a problem at higher gain, these techniques can help solve stability problems caused by capacitive loads.

Method 1 uses a parallel inductor-resistor combination in series with amplifier output to isolate or cancel the capacitive load. Feedback should be taken directly from the amplifier's Aol output. In the graph, this has the effect of restoring the amplifier response to 20db/decade. This method has the advantage that with proper component selection, it can produce an overdamped or critically damped response to a square wave. The inductor is typically 3 to 10µH, and the resistor from 1 to 10 ohms; although a higher voltage, lower current amplifier like PB58 needs about 35µH and 20Ω.

Method 2 uses ”noise gain compensation” to enhance stability. This method will work in virtually all cases. The idea is to set the ratio of RF/Rn for a gain high enough to insure crossing the Aol line at a stable point. The capacitor, Cn, is selected for a corner frequency one-tenth the Aol crossover.

Method 3 uses a capacitor in the feedback path to cause a phase lead in the feedback which cancels the phase lag due to capacitive loading. This technique requires careful selection of capacitor value to ensure 1/β crosses the modified Aol before unity gain, unless a unity gain stable amplifier which has a good phase margin is used.

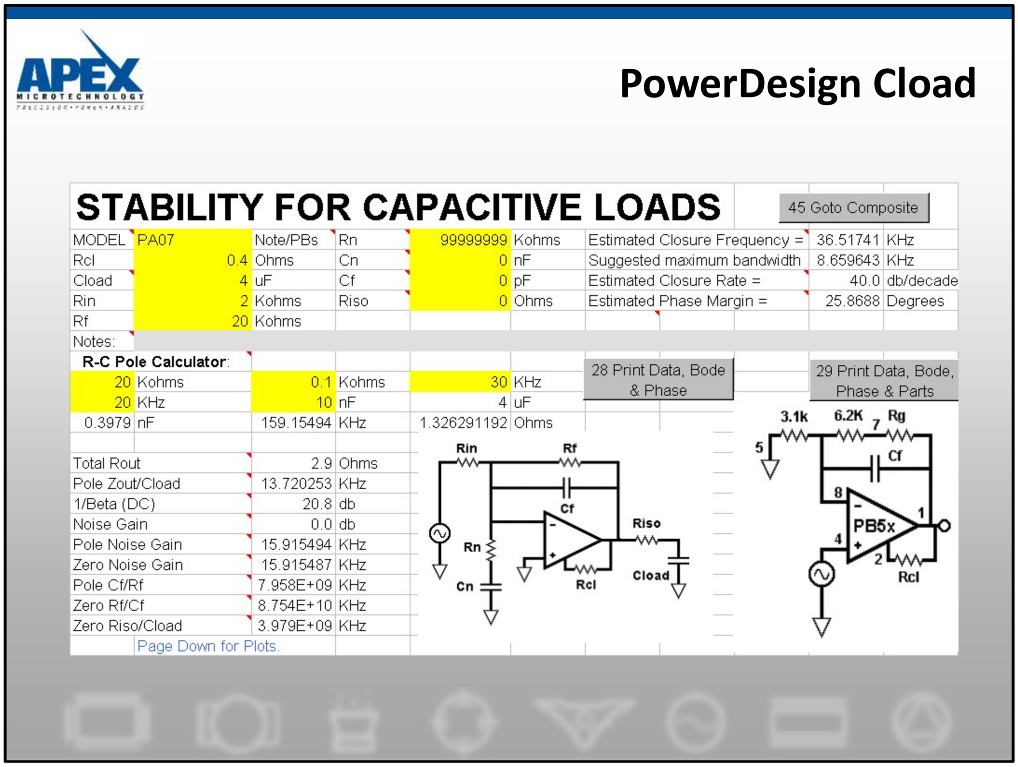
Ref. AN19, AN25, AN38



This plot illustrates how Noise Gain Compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is Vin and the other is a noise source summed in via ground through the series combination of Rn and Cn. Since this is a summing amplifier, Vo/Vin will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/β plot of the feedback as when Cn becomes a short and if Rn<<RI the gain will be set by RF/Rn. The figure above shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in the plot above that the Vo/Vin relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the Vo/Vin curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/β plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency, flat part of the noise gain no higher in magnitude than 20dB greater than the low frequency gain. This will force fp and fz in the above plot to be no more than a decade apart. This will also keep the open loop phase from dipping below –135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional –90 degrees in the open loop phase plot. Keep fp one-half to one decade below fcl to prevent a rate of closure of 40dB per decade and prevent instability if the Aol curve shifts to the left which can happen in the real world. Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/β plot. For completeness here are the formulae for noisegain poles and zeroes:

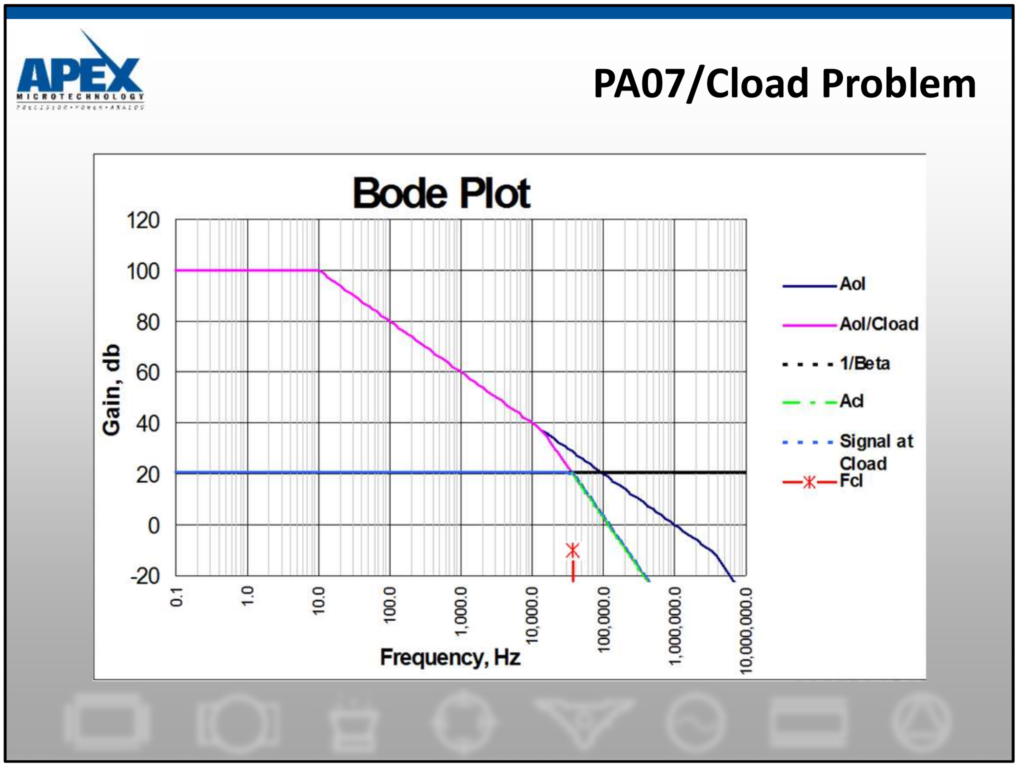
fp = $\frac{1}{2\pi Rn}$ fz = $\frac{RF+RI}{2\pi\,(Cn)(RFRI+RFRn+RIR\ \ )}$ Ref. AN19, AN25, AN38



This basic circuit will demonstrate how each of the capacitive load compensation techniques can work independently to solve the large C load stability problem.

This screen sets up the problem. Enter values describing the circuit being sure to assign open values to components not yet in the circuit. To the right we see a 40db closure rate and less than 30°phase margin. We don't need them yet but please note the three windows of the R-C Pole Calculator . The first window tells us 398pF will yield a pole at 20KHz when paralleled with 20K. The last window tells us 1.3Ω will place the corner frequency at 30KHz when in series with 4µF.

Ref. AN38

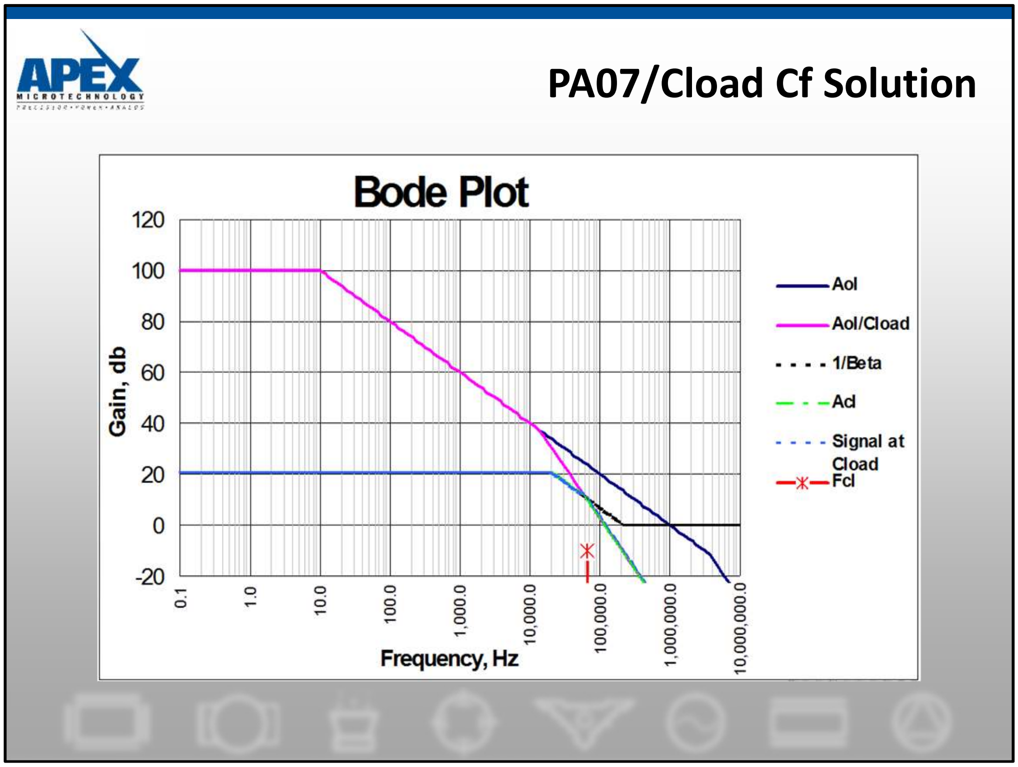


This picture is the first part of the problem. The output impedance of the PA07, plus the current limit resistor along with the big capacitive load, have added an additional pole to the open loop response of the amplifier. This degrades closure rate to 40db per decade--a warning flag. Its too bad we can't use a gain of 100 (40db) where closure rate would have been OK.

Here's the beauty of this system: Visualize or hold anything with a straight edge up to the graph in the area where we just learned a roll-off capacitor fixes these problems. Hold the edge parallel to the original open loop response curve and move it around to achieve intersection with the modified response about ½ way between 0 & 20db. Read the frequency where the straight edge crosses 20db. Remember the 20KHz in the R-C Pole Calculator? This is the origin. The spreadsheet makes it very easy to play "what if".

For noise gain compensation, visualize the upper flat portion of the curve being 20db up from the DC gain. Setting Rn = Rin/9 will put you about where it should be. On the open loop gain curve, read frequency where the imaginary line crosses. Enter one tenth this frequency and the Rn value in the R-C Pole calculator to set Cn. Again, play what if to optimize the circuit.

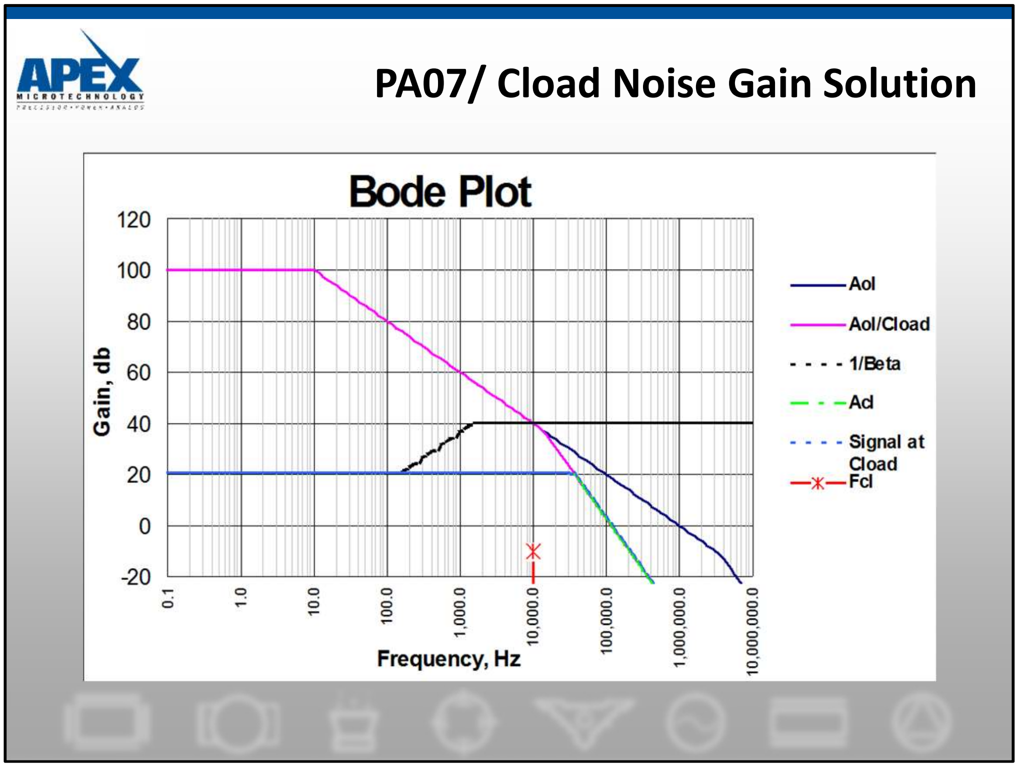
For Riso pick a frequency a little lower than the intersection of DC gain and the modified open loop gain. It looks like 30KHz is about as high as we should go. Use the R-C Pole Calculator, plug in values and optimize.
Ref. AN38



A 390pf capacitor yields 61 ° phase margin.

Time to use or vision again to discover a very important trap NOT to fall into.
The trap: If a little capacitor is good, a bigger one should be better.
The problem: 1/β never goes below 0db.

Visualize a line segment for 3.9nF capacitor starting down at 2KHz, then turning horizontal at 0db. Intersection rate is again 40db/decade and phase margin will drop to 16°!

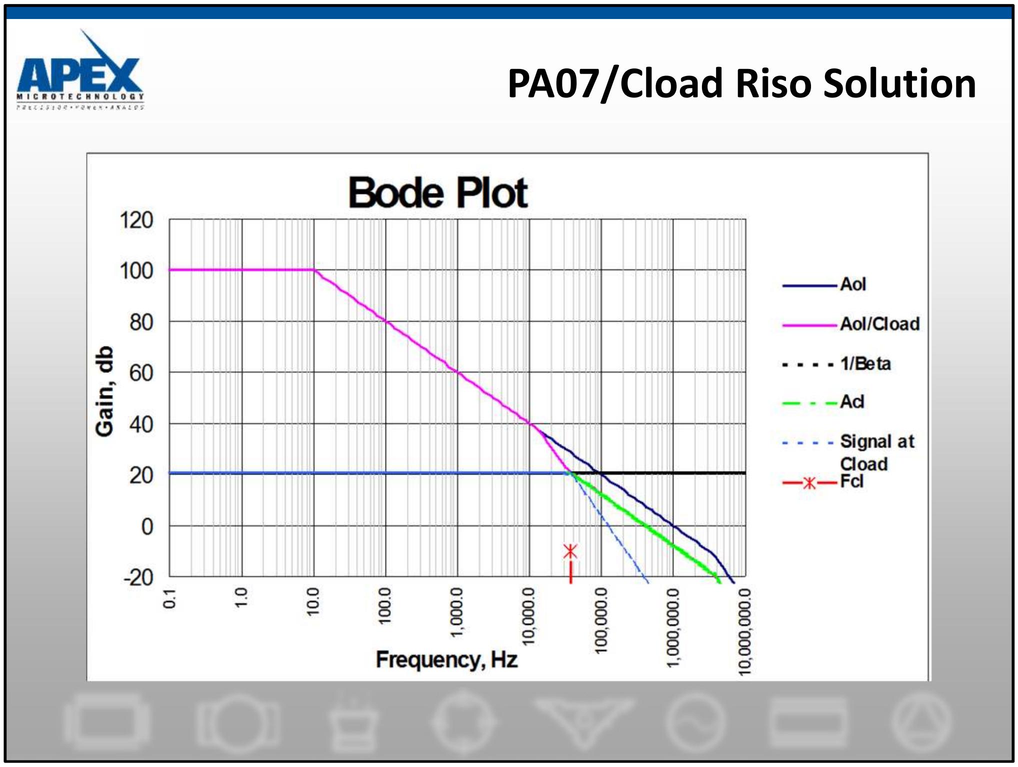


An important point one more time:

The closed loop curves here 1/β curves

They are obviously related to signal gains but are stability analysis tools which always assume non-inverting gain. A signal gain of -1 will plot as 2 in 1/β format. The signal gain does not increase between 150Hz and 1.5KHz.

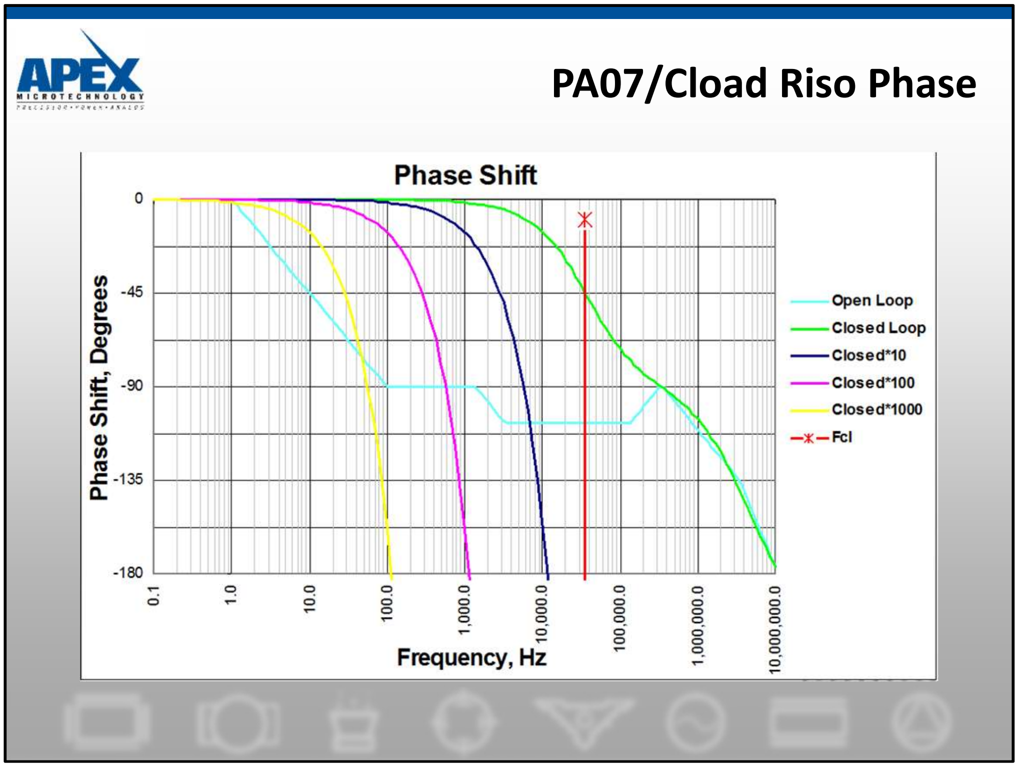
Ref. AN38



Notice the difference between the curve showing the Signal at Cload and the Acl curve. This is the voltage loss across Riso which is outside the feedback loop and therefore not corrected for amplitude loss. The picture says we really aren't loosing much at usable frequencies. Lets look at another error between 10KHz and closure frequency.

Op amp theory says output impedance is reduced by the loop gain. Our data entry screen told us Zout for the PA07 was 5Ω. This graph tells us loop gain goes from 10 to zero in our band of interest. This means uncorrected output impedance goes from 0.5 to 5Ω in this band. The losses across the 1.2Ω Riso now seem even more trivial.

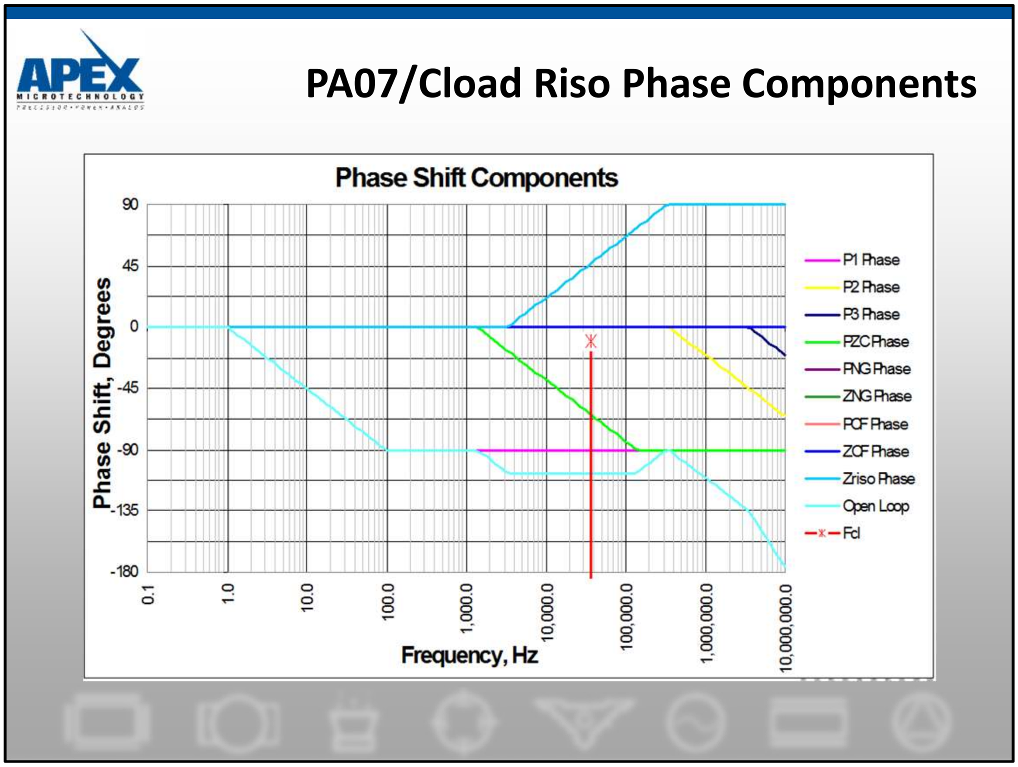
Ref. AN38



The first thing usually pulled from this graph is phase margin; 45°is good, 30°is pushing things. Here we see the open loop phase crossing Fcl (closure frequency) at 107¼°(Excel97 gives you the number if you place the cursor on the curve). Phase margin = 180°- open loop phase shift, or 72.75°in this case.

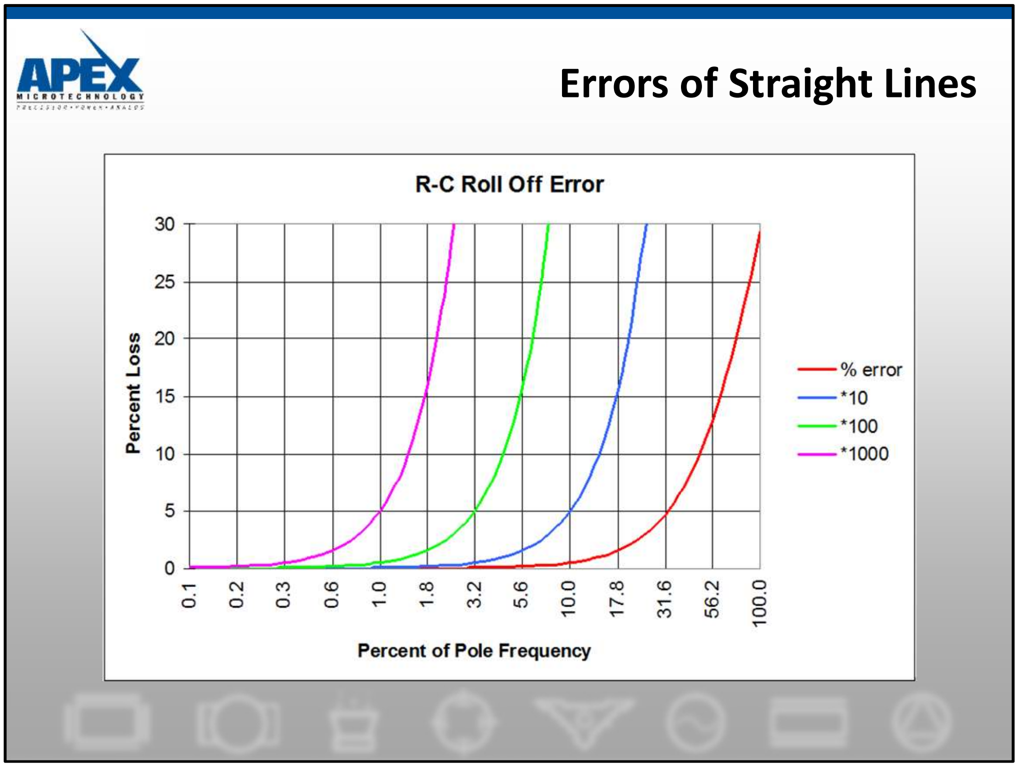
Sometimes we need to know the closed loop phase shift at a particular frequency. Suppose 1KHz is the point of interest. We can tell from the un-scaled curve this shift is not zero but resolution stinks. The curve with best resolution at 1KHz is the one scaled times 100. This curve crosses 1KHz at 158.66°for an open loop phase of about 1.6°.

Ref. AN38



Here are all the pieces making up the total open loop phase shift. Each segment is based on component values and the plotting rules detailed in Application Notes 19 and 25. P1 Phase (first pole in the bode plot) appears to be missing. Power Design shows only one curve when two or more coincide. Notice that P1 Phase does show up roughly between 1KHz and 100KHz. Open loop Phase is simply the sum of all the segments. Some segments show only partially or not at all because they are off scale, usually because of the open values entered.

Ref. AN38

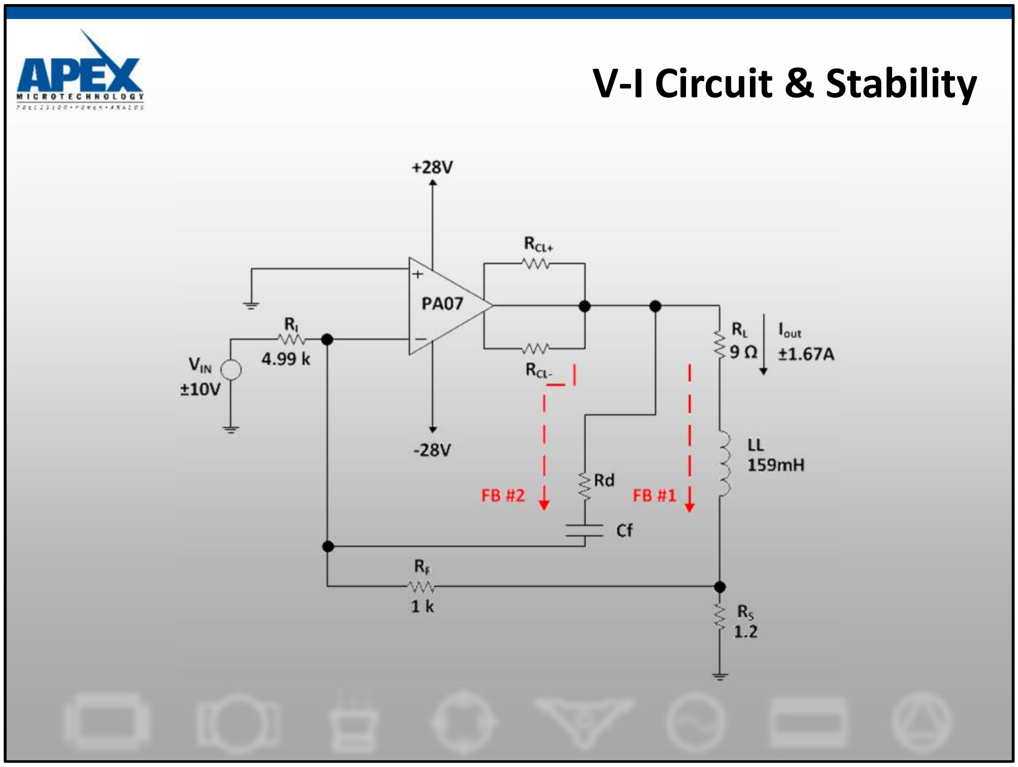


Straight line approximation is a great way to visualize location of corner frequencies but information is lost about attenuation near the corner. In db terms, the errors are small numbers and most circuits have enough frequency margin such that we see no problems.

In more exacting circuits, this graph indicates about 30% low amplitude right at the corner frequency, a 10.6% error at half the corner frequency, 3% at onequarter, and so on.

These errors apply to both the use of an isolation resistor and to a roll-off capacitor in the feedback loop.

Ref. AN38



This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

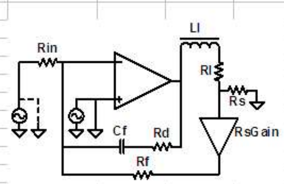
The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply –RF/RI which translates to (–1K/4.99K = –.2004). The Iout/Vin relationship is then VRs/Rs or Iout = –Vin(RF/RI)/Rs which for this circuit is Iout = –.167Vin .

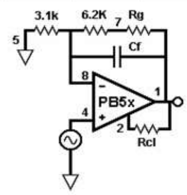
We will use our knowledge of 1/β, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

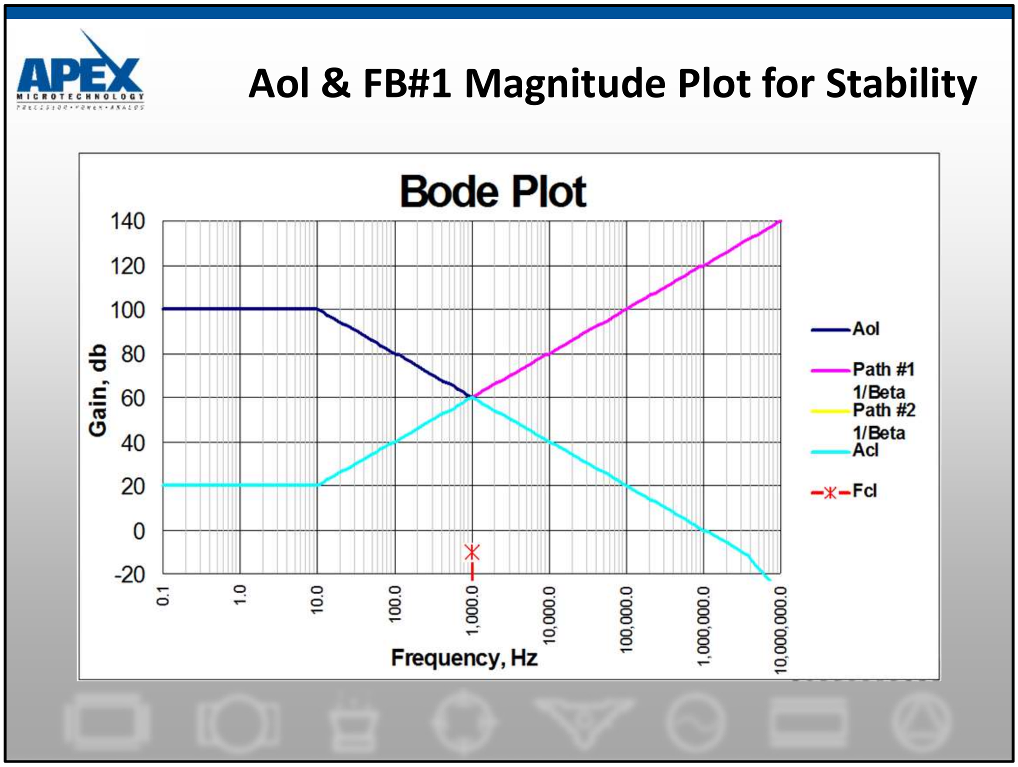
Ref. AN19

PA07 Inductive Load Problem Entry

	A	B	C	D	E	F	G	H	I	J	K	L
1	STABILITY FOR INDUCTIVE LOADS											
2	MODEL	PA07	Note/PBs	Rin	4.99	Kohms	Estimated Closure Frequency =			1	KHz	
3	Rs	1.2	Ohms	Rf	1	Kohms	Suggested maximum bandwidth			562.3413	Hz	
4	Lload	159	mH	Cf	99999	nF	Estimated Closure Rate =			40.0	dB/decade	
5	Rload	9	Ohms	Rd	999999999	Kohms	Estimated Phase Margin =			0.41	Degrees	
6	Rs Gain	1	Is this a Composite?		No							
7	Notes:											
8	R-C Pole Calculator +:		Value Suggestions:									
9	45	Kohms	Rd Kohms	82.47245	AC gain dB	22	28 Print Data, Bode & Phase		29 Print Data, Bode, Phase & Parts			
10	8	Hz	Rd Kohms	10	Rd Kohms	9.654487						
11	442.1	nF	Cf nF	1.11E-06								
12												
13	Ri/(Ri+Rf)		0.833055092									
14	Equiv Z @ Rs		1.2	Ohms								
15	Requiv/(Rl+Requiv)		0.117647059									
16	DC Beta		0.098006481									
17	DC Gain		20.17490405	dB								
18	Zero R/L		10.20993975	Hz								
19	Rin||Rf		0.833055092	Kohms								
20	Zero Rd/Cf		1.59157E-09	Hz								
21	AC Gain		181.5865255	dB								
22	Zero Cross		1000	Hz								





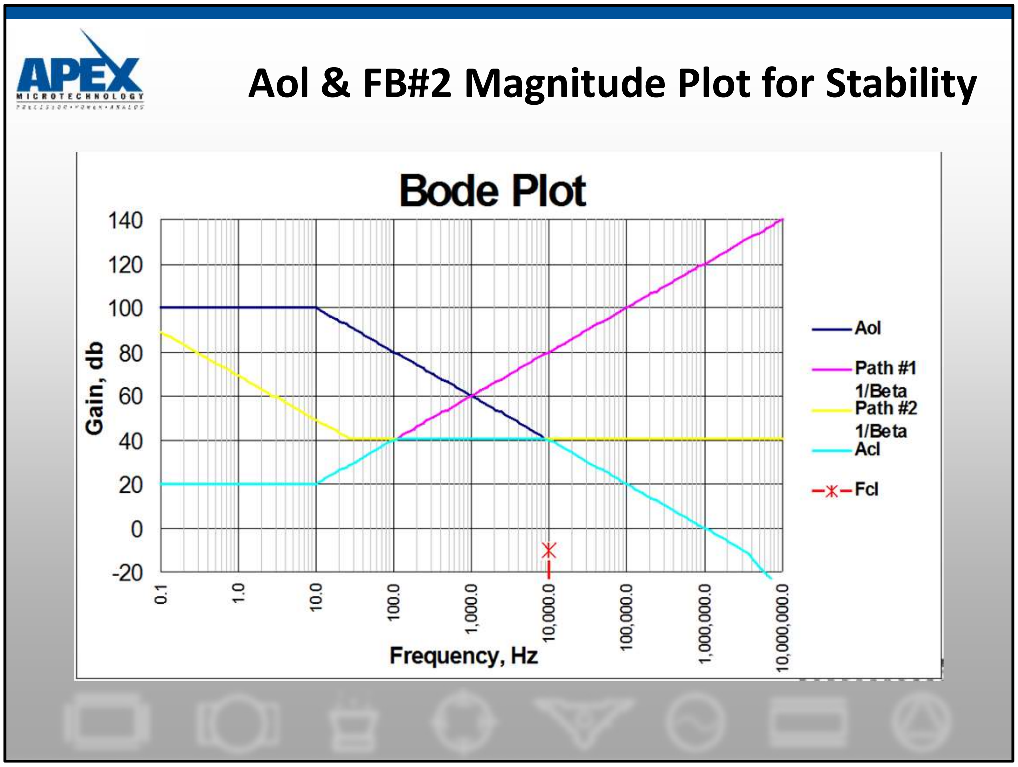


As frequency increases, impedance of the inductor increases and being inside the feedback loop it is causing closed loop gain to increase. Another way to view it: The amplifier's job is to drive constant current but as frequency goes up it needs more voltage to maintain that constant current, so voltage gain is increasing with frequency.

Open loop gain is decreasing 20db per decade and closed loop gain is increasing 20db per decade. This intersection rate of 40db per decade is the problem.

What if we could invent a circuit to make the open loop gain stop increasing? The precise function of feedback path #2! As soon as we enter this in the data entry screen, we see 20db per decade and phase margin of 45°.

Ref. AN19,AN38



Here's a way to start:

1. Select Rd for an AC gain either 20db below gain at the intersection or 20db above the DC gain of the current feedback (Path 1). These two points are the two suggested Rd values on the data entry screen. We can also read 40db from the graph and enter it as AC gain. An 82K should work well.

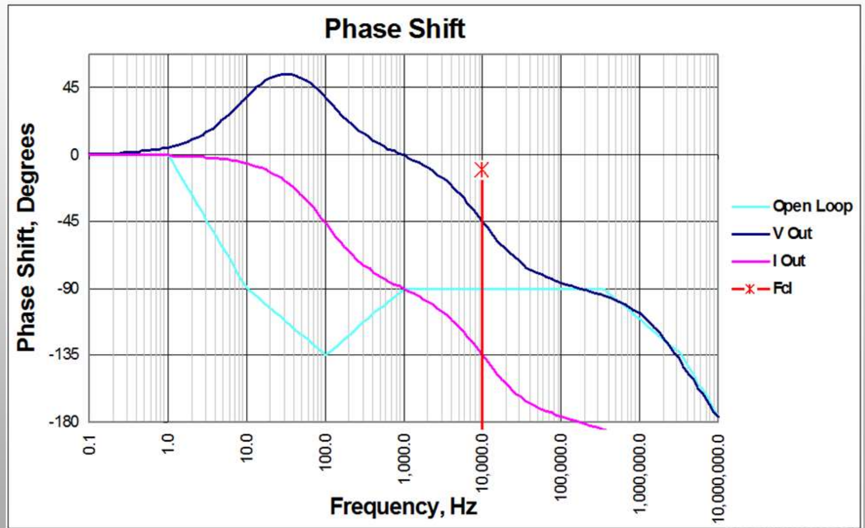
2. Select Cf for a corner frequency ½ to 1 decade below the intersection frequency. Giving the calculator pad 82K and 30Hz allows it to suggest a standard value of 68nF (with a little help from you). After entering 82K for Rd, the data entry screen will suggest a capacitor based on 1 decade below the intersection frequency.

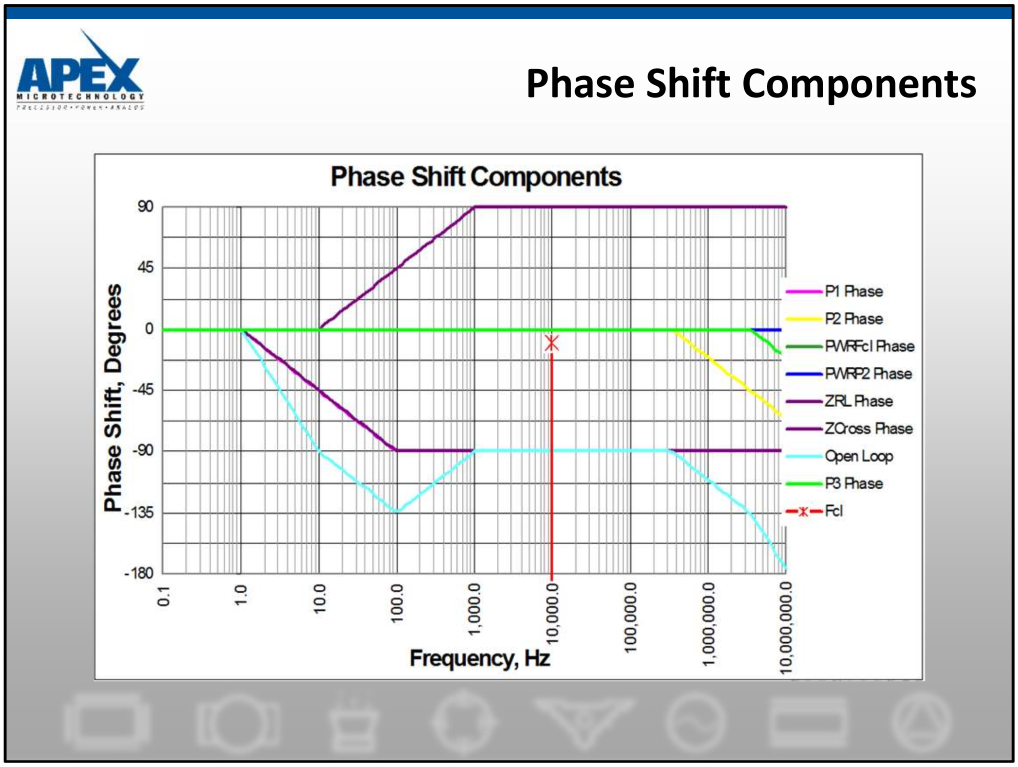
3. Play "what if" with the circuit.

4. If trying to achieve higher bandwidth, try increasing the value of Rs.

Ref. AN19,AN38

Phase Plot for Stability



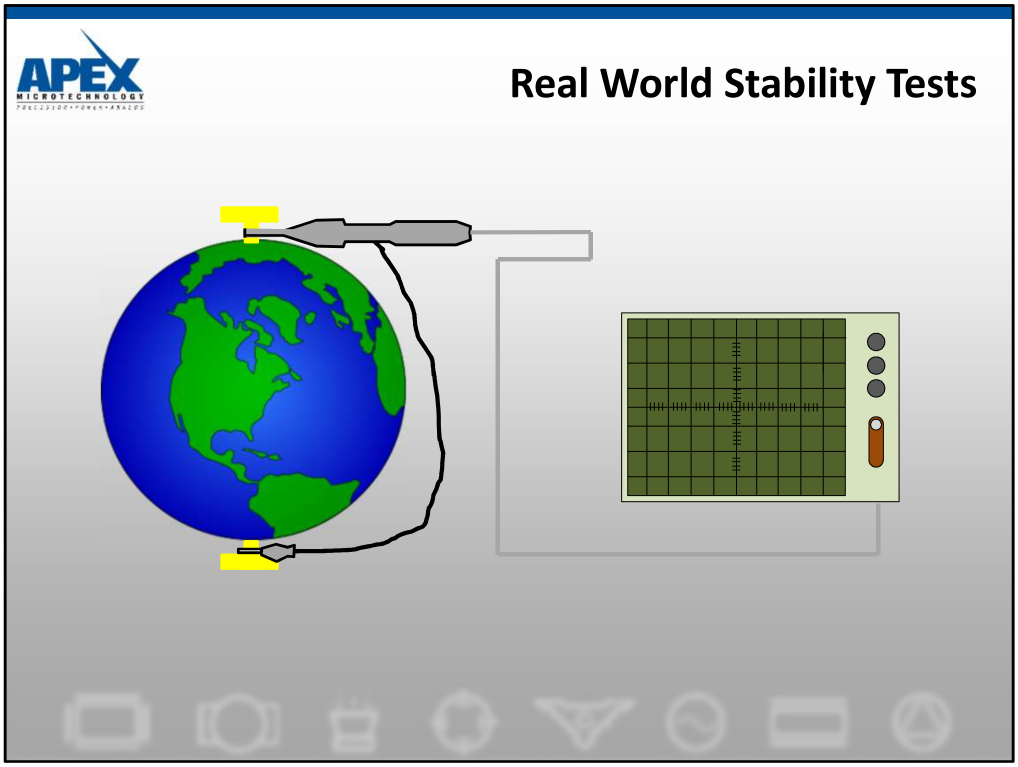


Here are all the pieces going into the previous phase plot. Again, Application Note 19 is the reference.

Stability Troubleshooting Guide

	Oscillates unloaded?	Oscillates with $V_{in} = 0$	Loop check† fixes oscillation?	Probable Cause (In order of probability)
CLBW ≤ fosc ≤ UGBW	N	Y	N	A,C,D,B
CLBW ≤ fosc ≤ UGBW	Y	Y	Y	K,E,F,J
CLBW ≤ fosc ≤ UGBW	-	N	Y	G
fosc ≤ CLBW	N	Y	Y	D
fosc = UGBW	Y	Y	N*	J,C
fosc << UGBW	Y	Y	N	L,C
fosc > UGBW	N	Y	N	B,A
fosc ≤ UGBW	N	N**	N	A,B,I,H

Previous sections have covered the major stability issues for more details and further explanation to use the Stability Troubleshooting Guide, refer to Application Note 1 “General Operating Considerations”
Ref. AN1 STABILITY



We have devoted much text to discussing and learning how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

When performing these tests, use actual production hardware. Supplies, harnesses, mechanical loads, fluid load and others all make a difference. The time spent here may save days of troubleshooting 6 months after the design is in production.

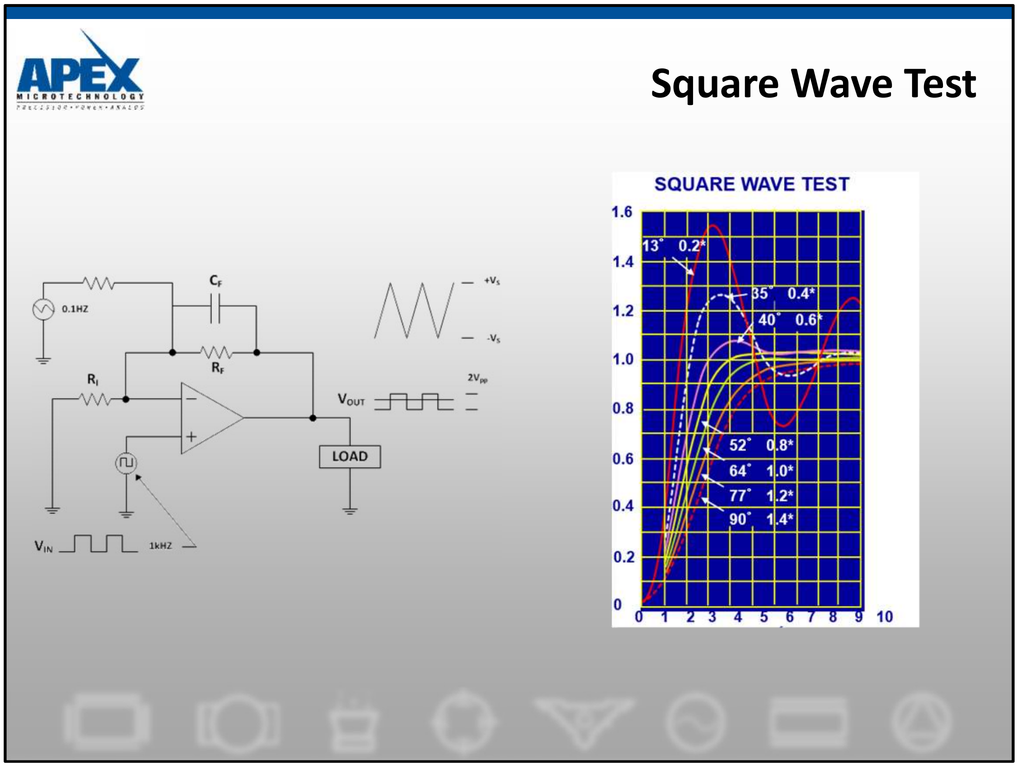


Figure 40 illustrates the Square Wave Test for measuring open loop phase margin by closed loop tests. The output amplitude of the square wave is adjusted to be 2 Vpp at a frequency of 1 kHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can be compared to the graph in Figure 40 to yield open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use

Ref. AN19

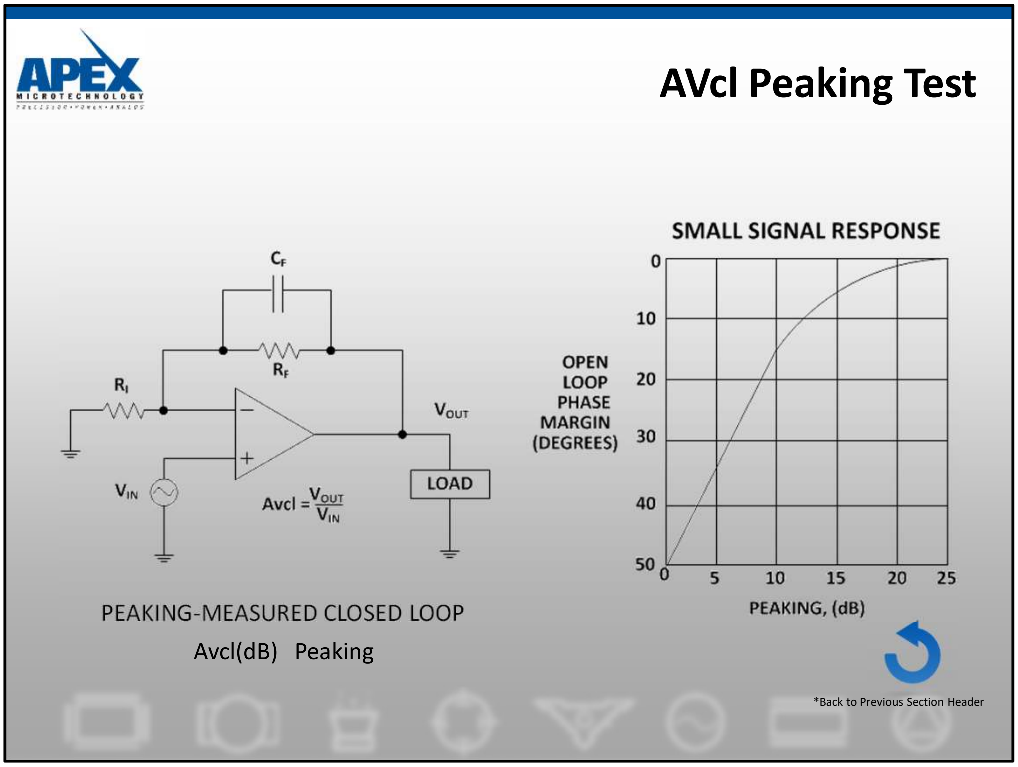


Figure 39 illustrates the AVcl Peaking Test for measuring open loop phase margin in the real world closed loop domain. From the closed loop Bode plot, we can measure the peaking in the region of gain rolloff.
This will directly correlate to open loop phase margin as shown.

We are often asked to generate data resembling this test. Why not look up the graph and translate to degrees of phase margin?

Ref. AN19

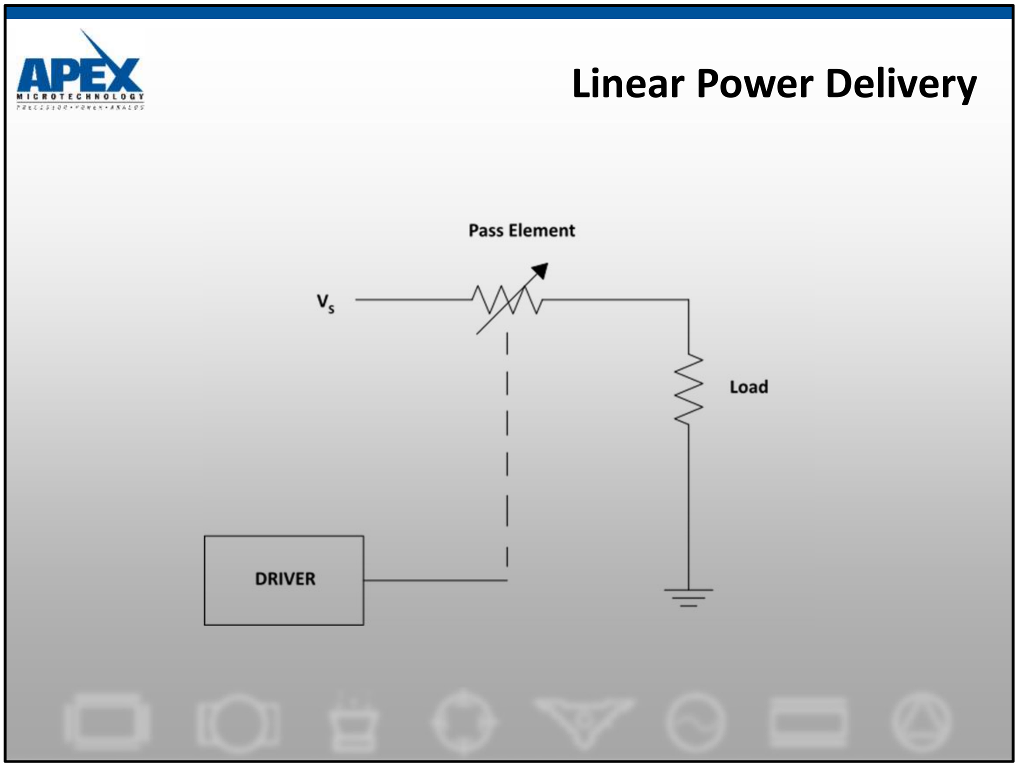
PWM BASICS

PWM

Pulse Width Modulation

- More Work
- Less Waste

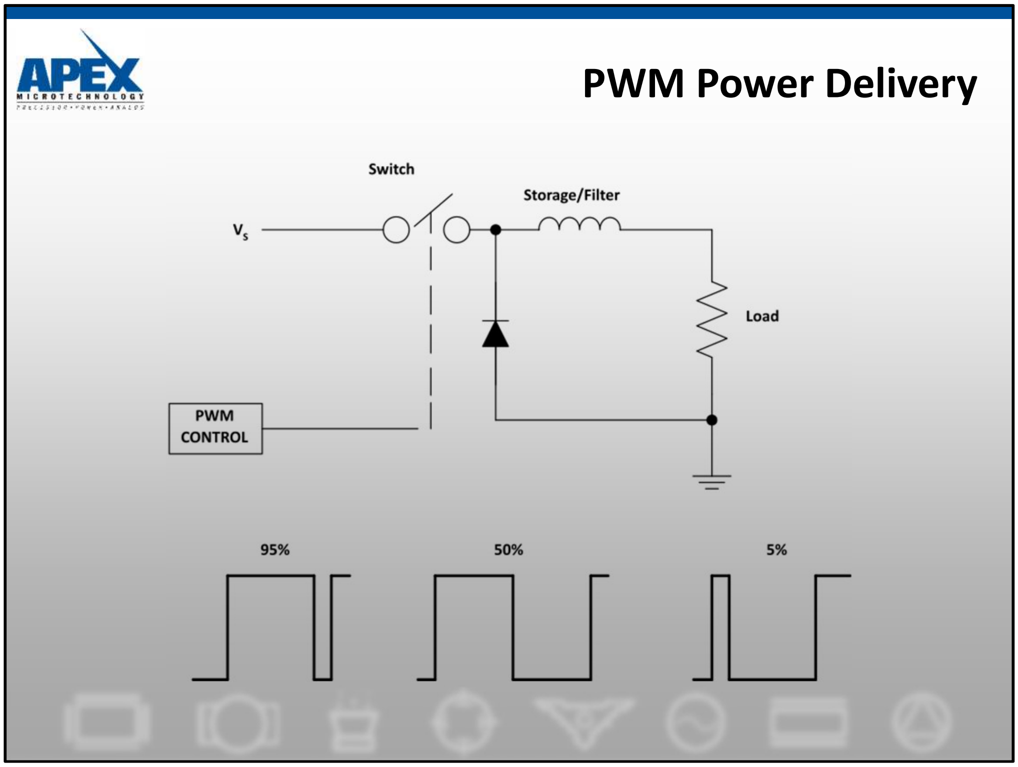
As delivered power levels approach 200W, sometimes before then, heatsinking issues become a royal pain. PWM is a way to ease this pain.



As power levels increase the task of designing variable drives increases dramatically. While the array of linear components available with sufficient voltage and current ratings for high power drives is impressive, a project can become unmanageable when calculation of internal power dissipation reveals the extent of cooling hardware required. Often the 20A drive requires multiple 20A semiconductors mounted on massive heatsinks, usually employs noisy fans and sometimes liquid cooling is mandated.

This slide illustrates the linear approach to delivering power to the load. When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level, losses in the linear circuit are relatively low. When zero output is commanded the pass element approaches infinity and losses approach zero. The disadvantage of the linear circuit appears at the midrange output levels and is often at its worst when 50% output is delivered. At this level, resistance of the pass element is equal to the load resistance which means heat generated in the amplifier is equal to the power delivered to the load! We have just found the linear circuit to have a maximum efficiency of 50% when driving resistive loads to mid-range power levels. When loads appear reactive, this efficiency drops even further.

Ref. AN30



These figures illustrate the most basic PWM operation. The PWM control block converts an analog input level into a variable duty cycle switch drive signal. If high output is commanded, the switch is held on most of the period. The switch is usually both on and off once during each cycle of the switching frequency, but many designs are capable of holding a 100% on duty cycle. In this case, losses are simply a factor of the on resistance of the switch plus the inductor resistance. As less output is commanded, the duty cycle or percent of on time is reduced. Note that losses now include heat generated in the flyback diode. At most practical supply voltages this diode loss is still small because the diode conducts only a portion of the time and voltage drop is a small fraction of the supply voltage.

The job of the inductor is both storing energy during the off portion of the cycle and of filtering. Inductors make their living by demanding continuous current flow; they become the energy source during the off time. In this manner the load sees very little of the switching frequency, but responds to frequencies significantly below the switching frequency. When the load itself appears inductive, it is often capable of performing the filtering itself.

With the PWM circuit, the direct (unfiltered) amplifier output is either near the supply voltage or near zero. Continuously varying filtered output levels are achieved by changing only the duty cycle. This results in efficiency being quite constant as output power varies compared to the linear circuit. Typical efficiency of PWM circuits range from 80 to 95%.

Ref. AN30

Contrasting Discrete Linear, Hybrid Linear and Hybrid PWM 1KW Designs

	Discrete Linear	Hybrid Linear	Hybrid PWM
Wasted Heat	500W	500W	100W
$/Year[1]	$438	$438	$88
Package Count[2]	8 x TO-3	2 x PA03	1 x SA01
Heatsink	0.11°C/W	0.11°C/W	.55°C/W

Almost all power amplifiers (low duty cycle sonar amplifiers are a notable exception) must be designed to withstand worst case internal power dissipation for considerable lengths of time compared to the thermal time constants of the heat sinking hardware. This forces the design to be capable of cooling itself under worst case conditions. Conditions to be reckoned with include highest supply voltage, lowest load impedance, maximum ambient temperature, and lowest efficiency output level, and in the case of reactive loads, maximum voltage to current phase angle.

Consider a circuit delivering a peak power of 1KW. A 90% efficient PWM circuit generates 100W of wasted heat when running full output, and around 50W driving half power. The theoretically perfect linear circuit will generate 500W of wasted heat while delivering 500W. Table 1 shows three possible approaches to this type design. In all three cases it is assumed ambient temperature is +30°C and maximum case temperature is +85°C. It also assumes power ratings of the TO-3 devices to be 125W each. Heatsinks for linear designs require multiple sections mounted such that heat removed from one section does not flow to other sections.

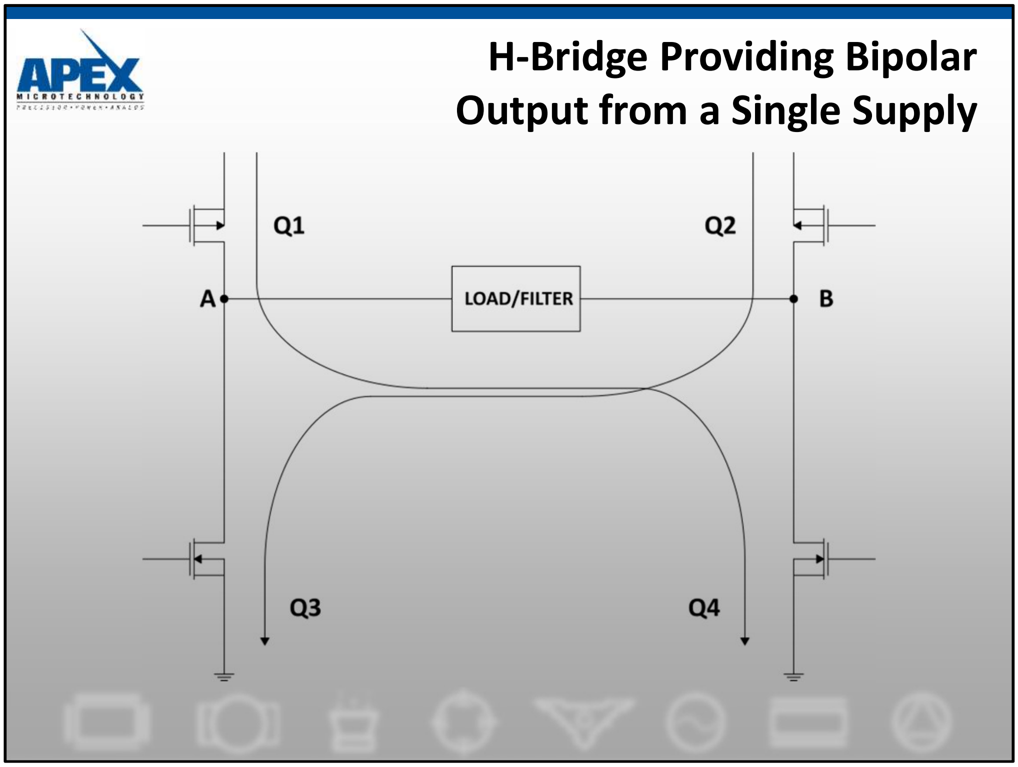
Ref. AN30

1 Continuous operation at a cost of $.10/kWH. If equipment is located in a controlled environment total cost will be considerably higher.

2 Package count must be doubled for the discrete design if bipolar output is required.

Benefits Resulting from PWM Efficiency

- Operating cost savings
- Capital cost savings
- Reduced heatsinking 5:1
- Smaller, lighter finished product

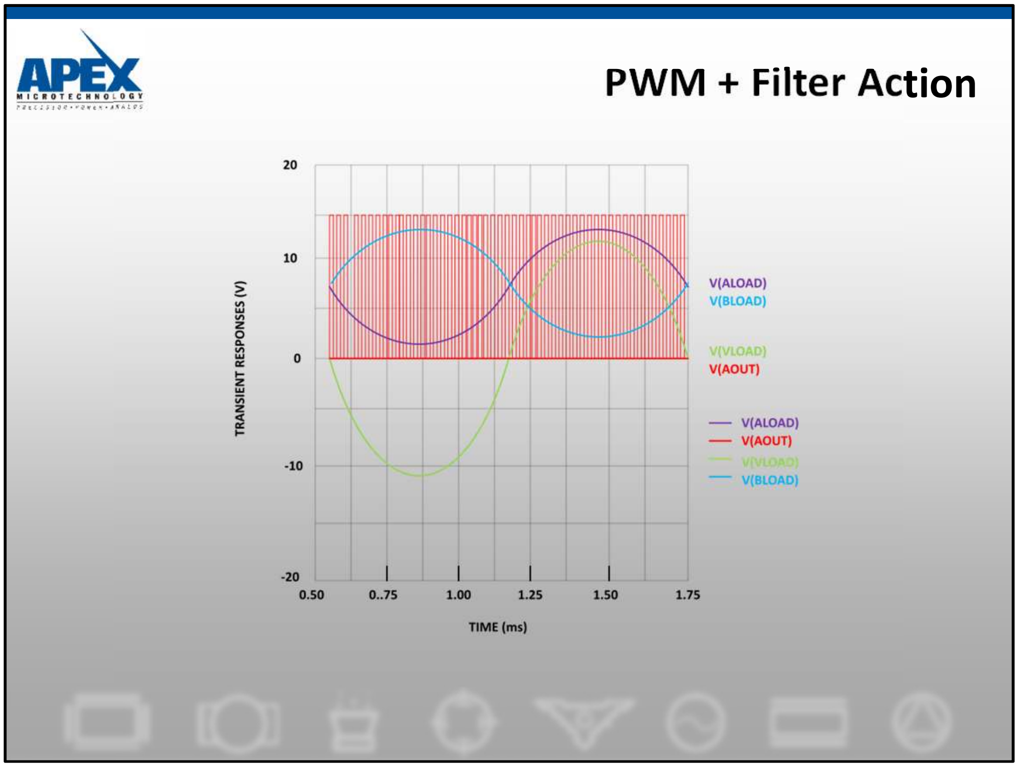


The simple form of a PWM circuit examined thus far is very similar to a number of switching power supply circuits. If the control block is optimized for producing a wide output range rather than a fixed output level, the power supply becomes an amplifier. Carrying this one step further results in the PWM circuit employing four switches configured as an H-bridge providing bipolar output from a single supply. This does mandate that both load terminals are driven and zero drive results in 50% of supply voltage on both load terminals.

The H-bridge switches work in pairs to reverse polarity of the drive even though only one polarity supply is used. Q1 and Q4 conduct during one portion of each cycle and Q2 and Q3 are on during the remainder of the cycle.

Note that if Q1 and Q3 turned on simultaneously, there is nothing to limit current. Self-destruction would be only microseconds away. The fact that these transistors turn on faster than they turn off means a “dead time” needs to be programmed into the controller.

Ref. AN30,AN39

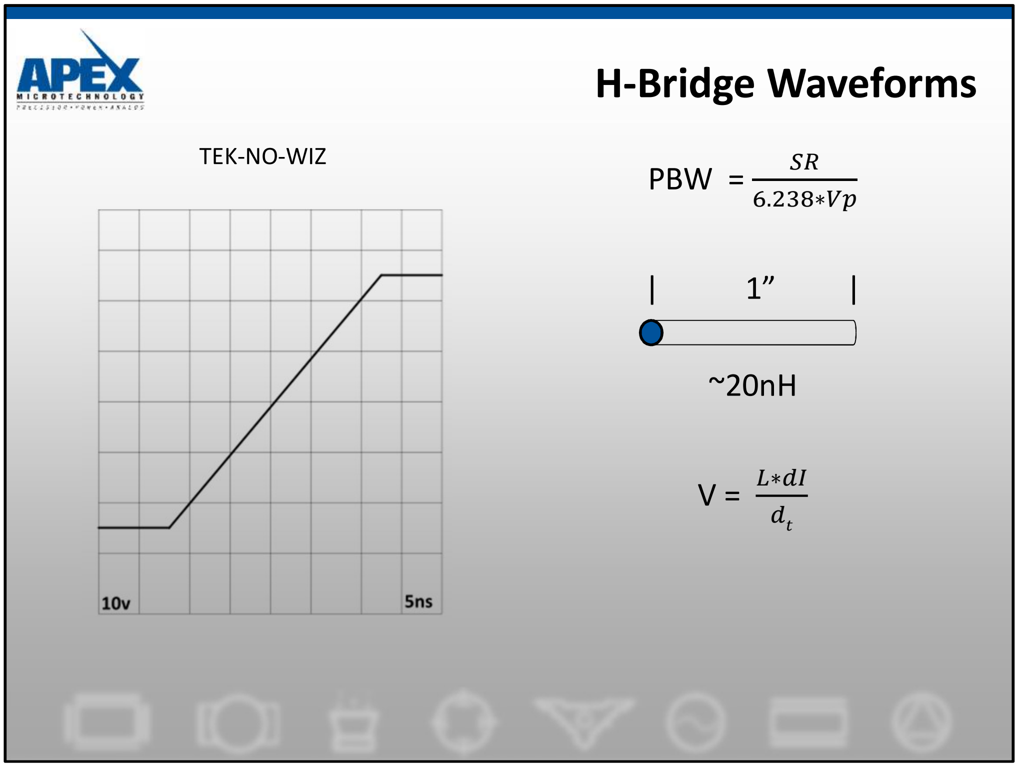


This picture shows the B output, switching at 42KHz, modulated at a 1KHz rate, along with the two filtered outputs and voltage as seen by the load.

As the A output spends most of its time in the low state, its filtered counterpart is swinging low. At the same time the A output (not shown, but out of phase with B) is mostly high and results in the filter A voltage swinging high.

With the load looking at the two filtered outputs differentially, it swings plus and minus. If you would zoom in on a ripple, it would be visible.

Ref. AN30.AN39



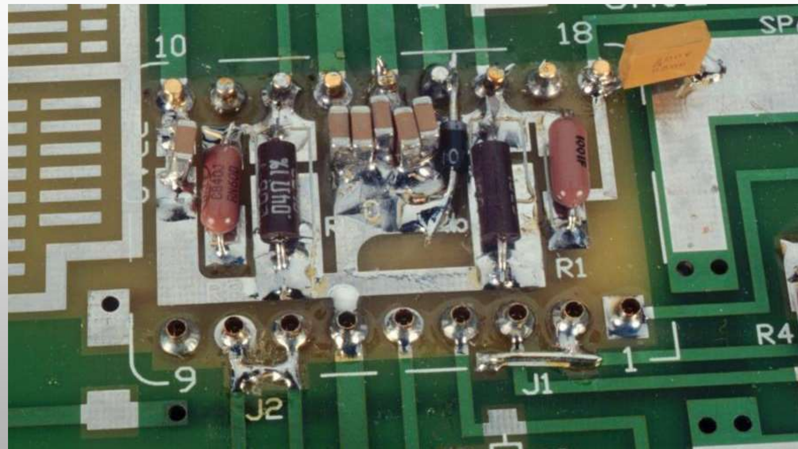
National had their FAST and DAMN FAST buffers, but they can’t hold a candle to these guys. In fact, that’s the problem with switchers- -they move voltages and currents around so fast it’s difficult to keep the noise down. Here are a few items you may not have had a chance to use lately.

From the analog world we borrow the equation relating slew rate to power bandwidth. If your PWM amplifier switches 50V in 25ns, the slew rate is 2000V/us. With peak voltage of 50V, this is over 6MHz. With 5 or 10 amps flowing, those transitions contain RF energy similar to a moderate radio transmitter. Spending a few minutes thinking like an RF designer may be worthwhile.

Currents are also changing very rapidly in these circuits. The picture above is of voltage, but keep in mind this voltage is on one end of an inductor where a power MOSFET just interrupted current flow. Look at the positive going transition: the lower MOSFET was conducting and the inductor is driving the voltage positive, above the positive supply, to maintain the previous current flow. The path will be through the body diode of the upper MOSFET, into the supply bypass capacitor. If current changes 5A in the same 25ns, two 1 inch capacitor leads will develop an 8V spike. On high speed PWMs this spike will cause the controller to freak out, rendering the circuit useless.

Ref. AN30, POWER SUPPLY BYPASS

Layout Sensitive? You Bet Your…



Apex has an Evaluation Kit for every PWM model

Evaluation Kits for PWM amplifier prototyping are a must. A bad layout will produce ample frustration and can cause dead amplifiers!

At a minimum, each kit provides a PC board, a way to get the amplifier plugged in, a moderate sized heatsink, and enough hardware to get it all put together. Several models also provide chip capacitors for low inductance bypass of the supplies.

In this example, the amplifier is on the opposite side of the board. Note the chip capacitors DIRECTLY between supply and ground pins of the amplifier. The two large black resistors are the current sense resistors which need to be a noninductive type.

Separate high current traces from low level traces as much as possible. Include ground plane under low level traces, but NOT under high current traces. Do NOT run high currents through the ground plane. Specify at least 2 ounce copper for the PC board. Make the ground pin of the amplifier be the center of the star ground system.

Ref. AN30

Does every low level scope observation yield the same spike-laden waveform? Here are a few causes and helpful hints.

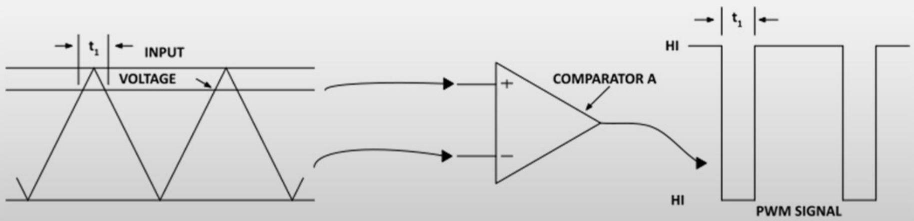
The typical 3” to 6” ground clip on the probe has to go because it is forming an inductive pickup loop. If luck holds, the scope accessory kit will yield an RF adaptor capable of providing a ground lead about ¼” long. If not, consider buying one or making your own by winding a length of spring wire (check for piano wire at your local hardware store) on a shaft slightly smaller than the probe tip (a set of drill bits would be handy).

The ground at the amplifier contains high levels of high frequency signal relative to the ground at the scope and common mode rejection of the scope is limited. Disconnect all other signal cables from the scope. Use a battery operated scope or a ground breaker on the power cord. Use a high frequency toroid to construct a low pass common mode filter for the probe as shown.

Fast slewing signals can easily be coupled to high impedance or unshielded probes. Use only probes with nearly complete shielding. Forget the grabber clips, extenders or any single conductor connections to the scope.

Ref. AN30

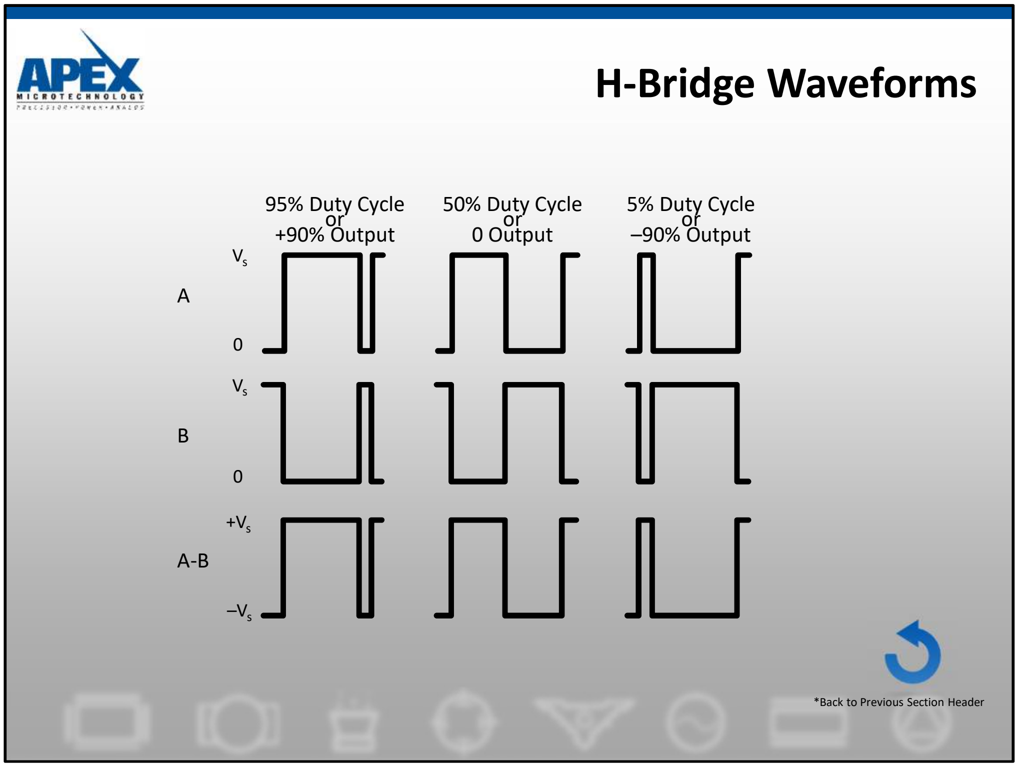
PWM Waveforms



HOW A PWM SIGNAL IS GENERATED

This picture illustrates basic control of one diagonal pair of switches. As the input voltage rises toward the upper peak of the triangle wave, the high portion of the waveform increases. Pure theory dictates that any duty cycle can be programmed, but propagation delay, rise and fall times and hysterias pose practical limits to how narrow a pulse can be. Typical minimums range from about 100ns to 1us. This typically translates into a 1 to 5% band on each end of the duty cycle range which cannot be sustained. Let us assume the signal is 90% and increasing. When the band is encountered, modulation will jump to 100%. On the way back down, there will be a jump from 100% to just under the band (down to 99 to 95% typically).

Notice that there is no discontinuity in the middle of the range (50/50 duty cycle and zero volts out for a full bridge. This is an advantage over another popular modulation scheme, sign magnitude modulation where different switches are turned on and off for positive and negative outputs. Borrowing from the linear world, this is similar to the difference between class A-B output stages and Class B output stages where Class B designs have a dead band (crossover distortion) where the circuitry changes output drive transistors. On the down side for locked anti-phase modulation, is the fact that near 50/50 duty cycles, the filter must do more work (efficiency at midrange is lower than sign magnitude modulation). This is generally only a concern when the system spends a large portion of the time driving very low currents.



To help understand the conversion of the time modulated data to analog levels, visualize each waveform segment of Figure 2 run through a low pass filter whose cutoff frequency is at least 10 times lower than the switching frequency. The A and B voltages of the 50% duty cycle waveforms will both be equal to 50% of the supply voltage. With both terminals of the load connected to the same voltage, the load sees 0V across itself. The A-B waveform represents this differential connection of the load, and the filtered voltage of this waveform equals zero.

To examine the 95% duty cycle waveforms, lets assume a supply voltage of 100V. The filtered A value will be 95V, B will be 5V, and the load will see 90V; the same as the filtered value of the A-B waveform. When the duty cycle shifts to 5%, the filtered A value will be 5V, B will be 95V, and the load will see –90V, again matching the filtered value of the A-B waveform.

Changing duty cycle through 50% is a continuous function, meaning there is no inherent discontinuity as exists in sign magnitude modulation. This is analogous to the much improved distortion levels of class AB linear stages versus class B linear stages where zero current crossing brings a discontinuity or dead spot usually referred to as crossover distortion.

Ref. AN30,AN39

BASIC PWM TRANSFER FUNCTION

Basic PWM Transfer Function

- $V_O = \frac{V_{mid} - Vi}{V_{pk}} * V_S - I_O * R_{on}$

- V_O = output voltage
- V_{mid} = ramp midpoint
- V_{in} = input voltage
- V_{pk} = ½ ramp V_{p-p}
- V_S = supply voltage
- I_O = output current
- R_{on} = total on resistance

$-1 \leq \frac{V_{mid} - Vin}{V_{pk}}$

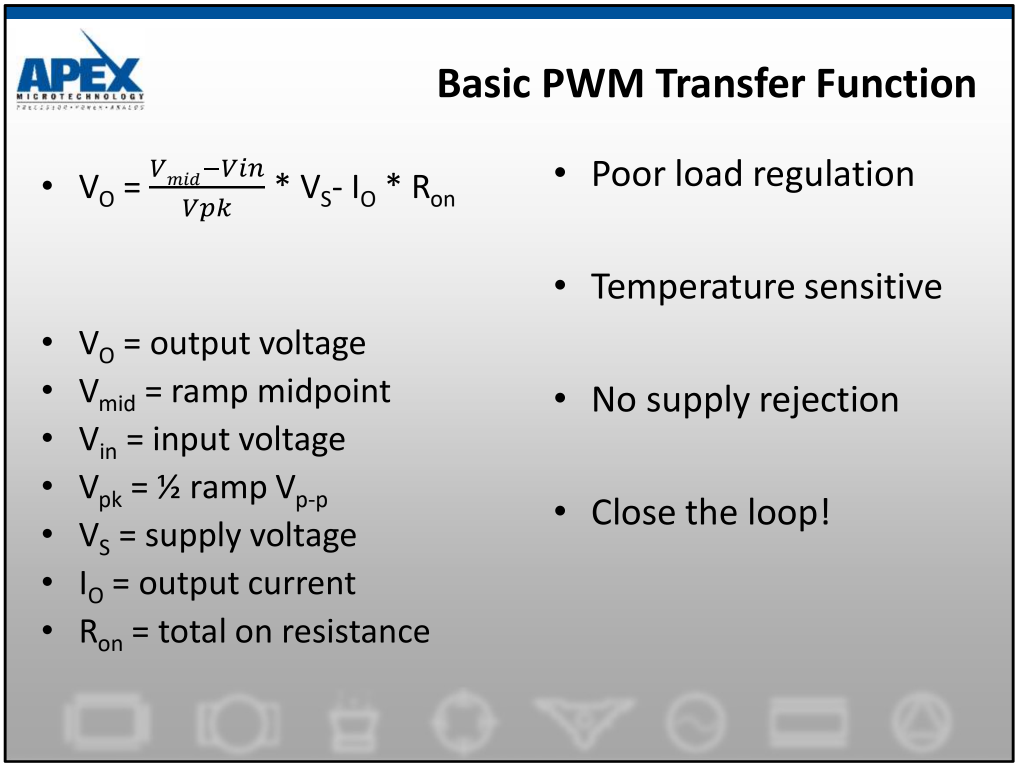
$\text{Gain} = \frac{2 * VS}{V_{ramp\,p\_p}}$

Speaking of a full bridge FET amplifier:

The first term of the output equation concerns duty cycle and is arranged to numerically yield a range from –1 to +1.

Multiplying by the second term yields +Vs to –Vs (even though there is no –Vs). For IGBT amplifiers, forward drop would be subtracted from Vs prior to multiplying.

The last two terms represent internal loss in the switches. Manipulating the equations a little tells us gain is the ratio of twice the supply to the ramp peak-to-peak amplitude. This is important for stability evaluation.



Op amps are very seldom run open loop because the gain is unmanageable. With a much lower gain, there is a temptation to run PWM amplifiers open loop. Here are the major limitations of open loop PWM operation.

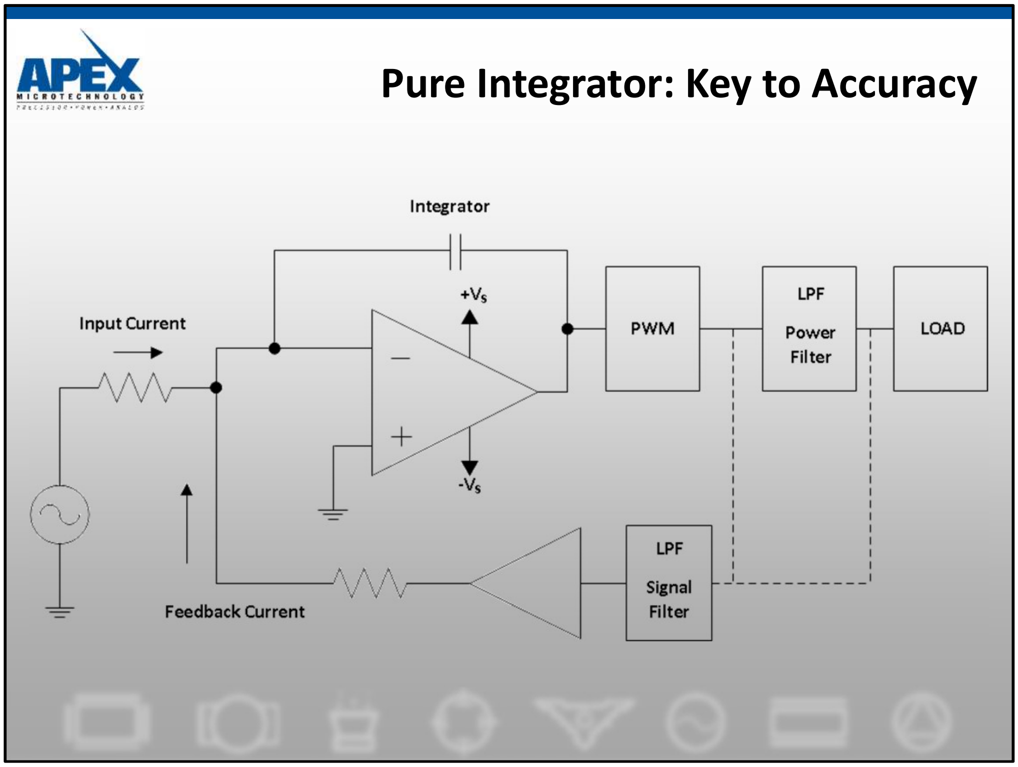
We tend to not worry about op amp output impedance because it is reduced to an insignificant level by the loop gain of the amplifier. On resistance of PWM amplifiers ranges from about 0.16Ω (30A model) to 0.5Ω (10A model) resulting in load regulation errors up to several volts.

To make matters worse, these on resistances increase by about 2 times between JUNCTION temperatures of 25°C and 150°C!

Those of us accustomed to working with power op amps take power supply rejection for granted; at least at low frequencies, so supply voltage changing a few percent is of no concern. The open loop PWM circuit offers NO supply rejection.

Accuracy and open loop operation of a PWM amplifier do NOT go together.

Closing this loop can be done locally in the voltage mode and with most models in the current mode. The alternative is closing the loop with system components. This often involves mechanical components, velocity or position sensors and a computer

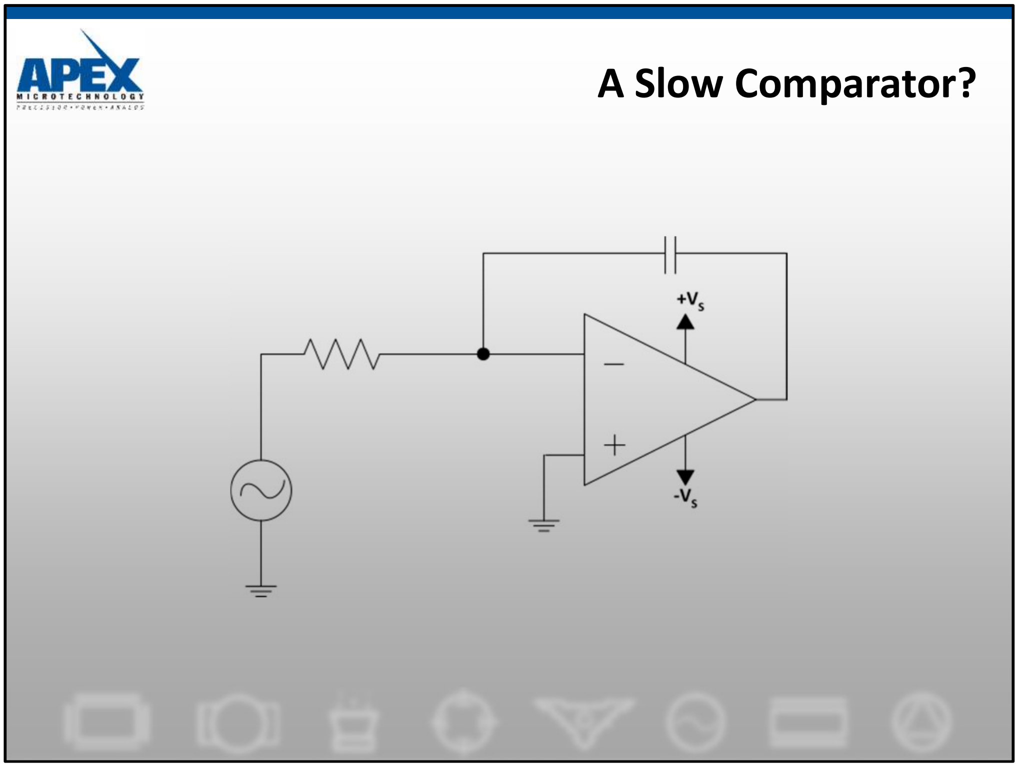


Here is very general look at closing a PWM amplifier locally. The PWM output is filtered and delivered to the load as a power analog signal (occasionally a load may do its own filtering). A feedback circuit usually contains a low pass filter and often an amplifier. It has multiple topology options to monitor voltage, current or process variables such at position or temperature. The feedback circuit provides a voltage representation of the job actually being done.

The integrator now drives the PWM input where ever required to force input and feedback currents to be equal and opposite. Considering the job of the feedback circuit, the integrator forces the job being done to follow the input voltage command.

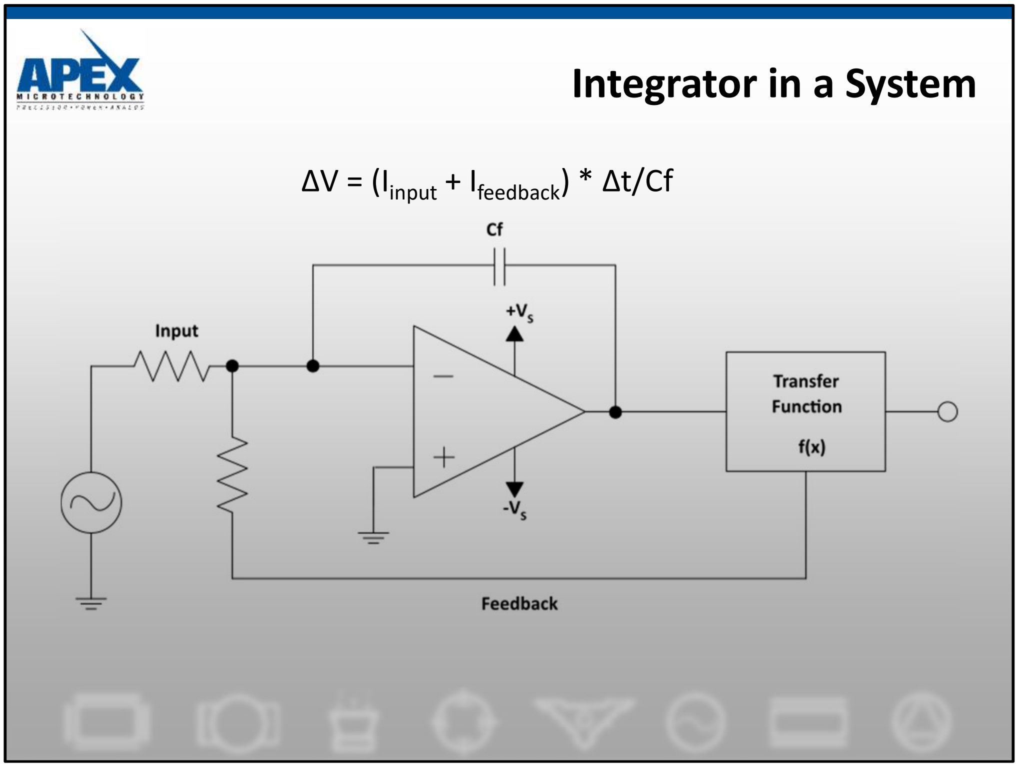
When the loop is closed, output voltage changes due to variations in load, supply and temperature are greatly reduced.

Ref. AN39



No, this slide is not a mistake, its just a way to examine the basic operation of the op amp integrator.

Any one for a slow comparator? That’s what we find here, where the feedback capacitor slows down the transition time. During the transition, the op amp is likely operating in a linear closed loop fashion. The input signal sets a current in RIN because of the virtual ground property of the inverting input. With no current in or out of the op amp input pins, the input current path is through the feedback capacitor to the op amp output. Voltage is developed across a given capacitor, governed by the time and magnitude of the input. Linear operation ceases when the output of the op amp cannot meet the current requirement. This happens when the op amp slew rate, current capability or most often, voltage swing capability is exceeded. This is fine, the comparator has done its job of switching, with a controlled transition rate.

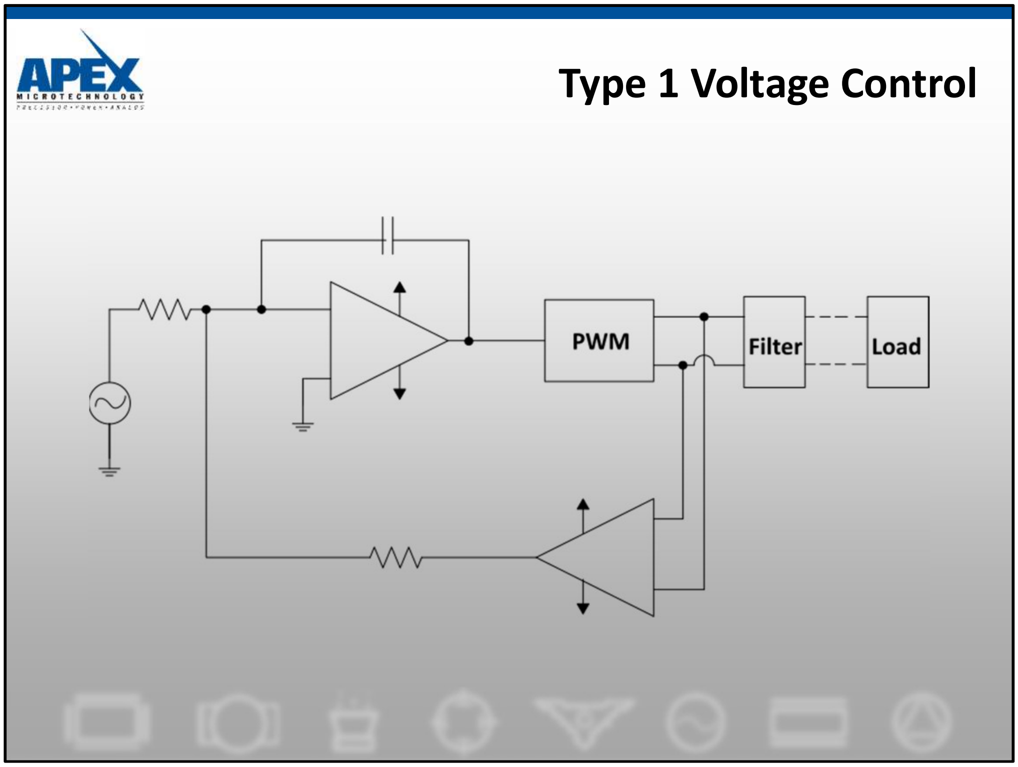


With a little modification, we can transform this switching circuit into a very useful linear tool. What is required is a form of feedback to maintain operation in the transition area, or the linear area. This figure shows a generalized form of this where ƒ(X) is non-inverting. This function is often non-linear, but seldom contains step functions.

Confining our analysis to linear operation, there is no current in the op amp input pins. Looking at the summing junction with three connections, current in any given path must equal the sum of the other two paths. Therefore, capacitor current will be the algebraic sum of the input and feedback currents.

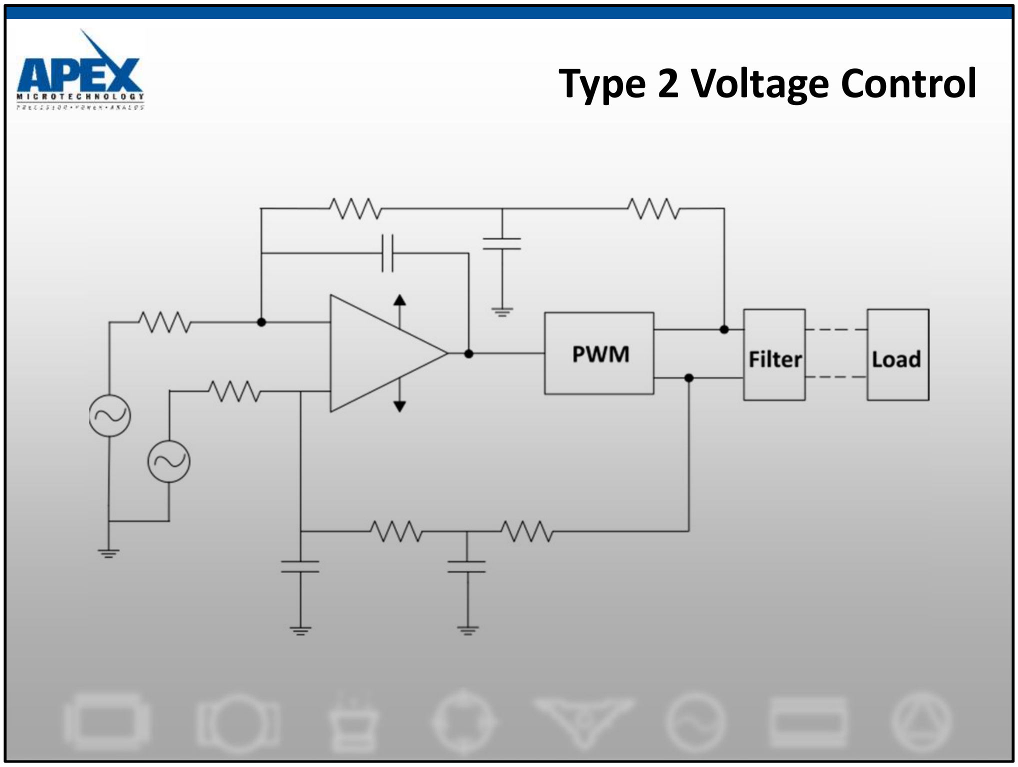
If I_{IN} and I_{FDBK} are equal and opposite, the output does not move.

Notice that our rule on movement of the output does NOT predict absolute level, only direction and rate of movement. This can be a magical elixir for many ƒ(X) functions.



This simple voltage control circuit illustrates that in addition to improving accuracy over open loop operation, the integrator simplifies circuit design. Assume the input and feedback resistors are equal and that the gain of the differential feedback amplifier is 1/10. This tells us right away that the circuit gain is 10.

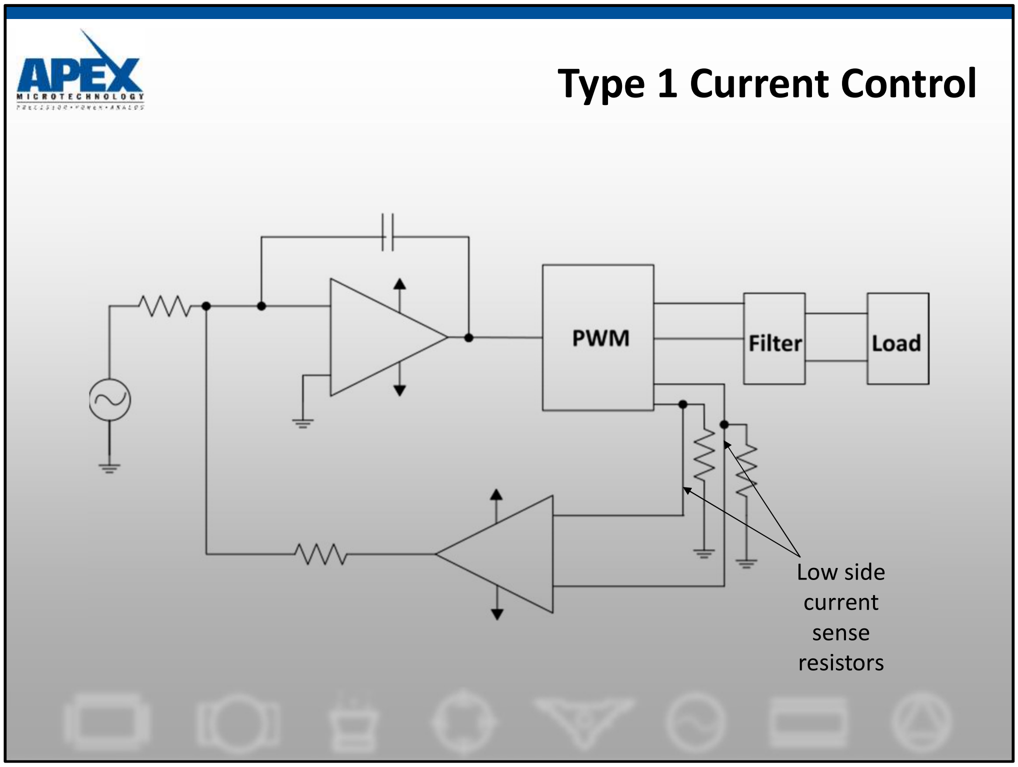
The function of this circuit can be determined using simple op amp rules- -without ever having to calculate a duty cycle. The idea is to let the PWM handle the power and let the op amp(s) handle signal control- -the brawn, and the brains.



By substituting a second PWM output for the voltage reference of the previous circuit, and adding a low pass power filter, we have simple control of a high power drive with a minimum component count.

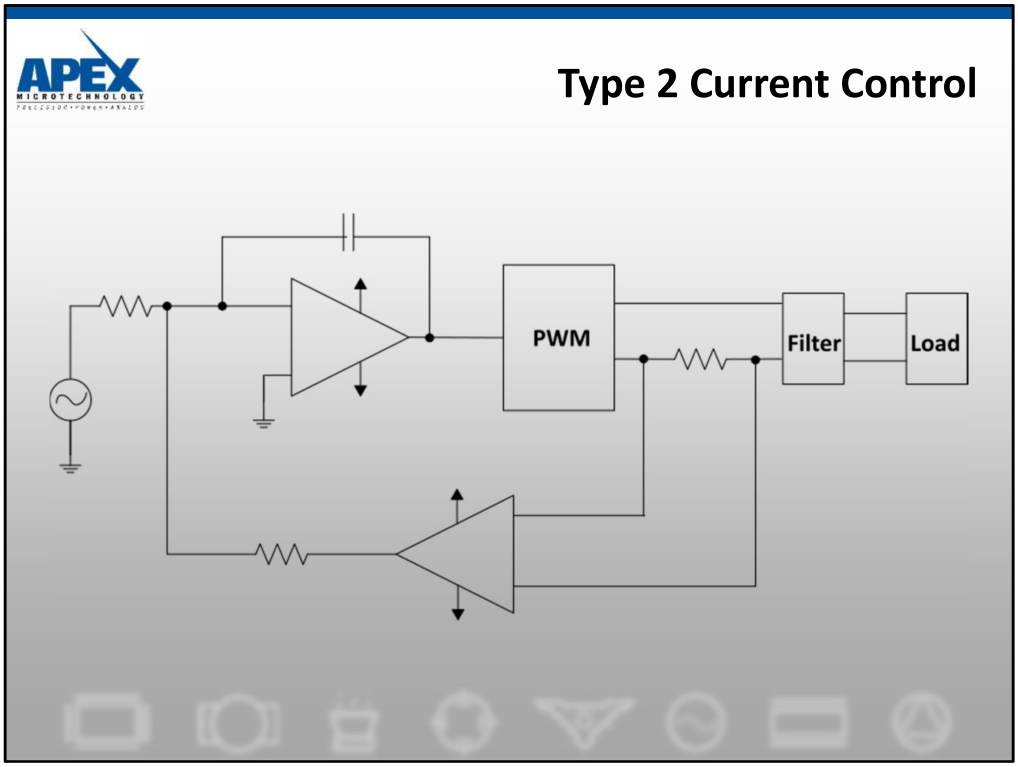
Note that we have split Rf into two resistors to facilitate the addition of a low pass small signal filter so the op amp does not have to contend with large square waves at the switching frequency.

Just as in the previous circuit, the components on the plus and minus sides need to be matched.



Remember the four switches configured as an H-bridge? Underneath the two lower switches, we insert low value sense resistors to monitor current. As the load current changes polarity, the current path switches resistors. With a differential amplifier looking at both resistors, it will output a bipolar voltage corresponding to the bipolar current in the load.

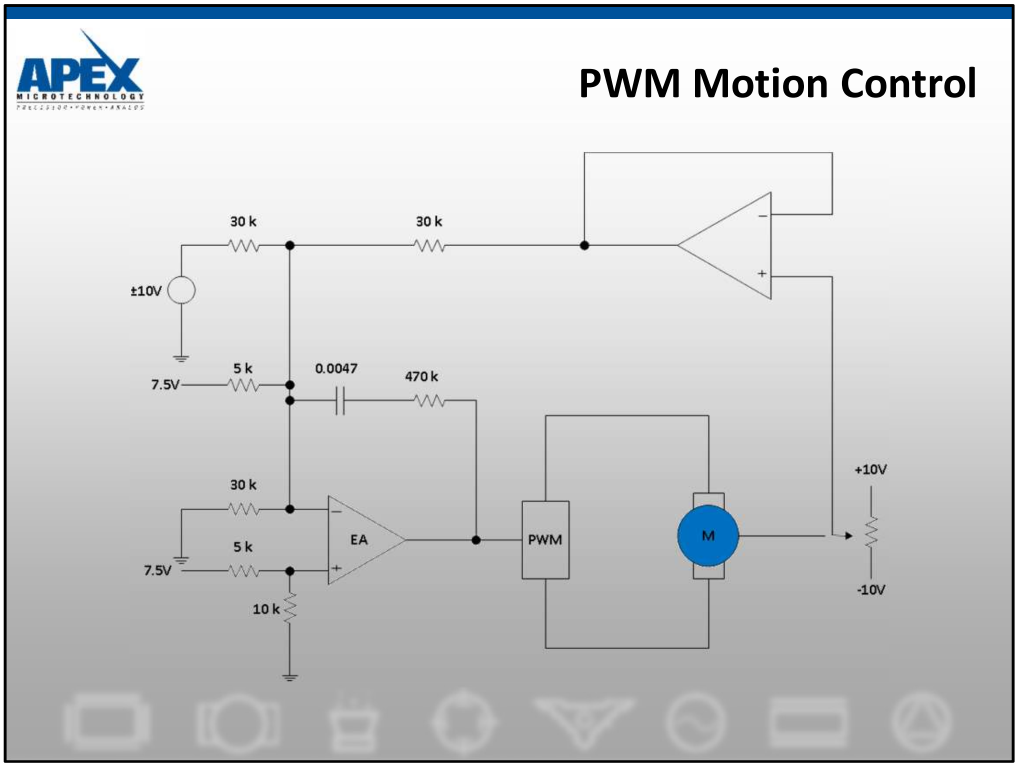
Again, we find simple op amp rules controlling the high power PWM amplifier.



In our business, almost everyone likes smaller packages. However, pin count comes down with size and this leaves a couple models with the two current sense points tied inside the package to save a pin. Magnitude information is present and can be used for current limiting, but direction information is lost.

In this case a sense resistor in series with the load, plus a differential amplifier can get a current control circuit up and running.

Beware the common mode voltage fed to this difference amplifier will be up to the main supply voltage of the PWM amplifier.



While one of the simplest forms of position sensing is shown here, options such as optical encoders, LVDT sensors, tachometers and variable capacitance transducers are all viable ways to sense speed or position. In a wider sense, this basic circuit can be adapted to control a wide variety of process variables such as temperature, flow rate, pressure, light intensity…………..

The key elements in all these possible variations are the same:

The PWM amplifiers controls the power
The feedback circuit monitors the job
The integrator forces the job to follow the command input

Note that the motor (and its load) are inside the feedback loop in this circuit. This means the frequency characteristics of these mechanical elements is inside the feedback loop and need to be considered when analyzing response and stability of the circuit.

Ref. AN30

Compare: PWM & Linear Amps

V or I input	OK	OK
V or I output	OK	OK
Supplies	Single	Single/Dual
Max Power	Several KW	Fractional KW
Efficiency	High	Low
Noise	High	Low
Speed	Low	High

*Back to Previous Section Header

Think about the two previous pages a moment.

They are both basically op amp circuits where the driving op amp has a specialized output stage labeled PWM. In fact there are many applications where linear and PWM solutions would both work. The keys to the decision may be on the last two lines above: IF THE APPLICATION DOES NOT REQUIRE LOW NOISE AND HIGH SPEED, PWM AMPLIFIERS CAN PROVIDE A SOLUTION.

The next item to consider is cost. On a cost per watt capability basis, PWM amplifiers are generally less expensive than linears. With PWM capability starting at 200W, they are not the most likely candidates for a 5W job. At a few hundred watts, PWM amplifiers are very attractive. In between these levels, you may want to think more about the options because both linear and PWM amplifiers will likely work.

Ref. AN30

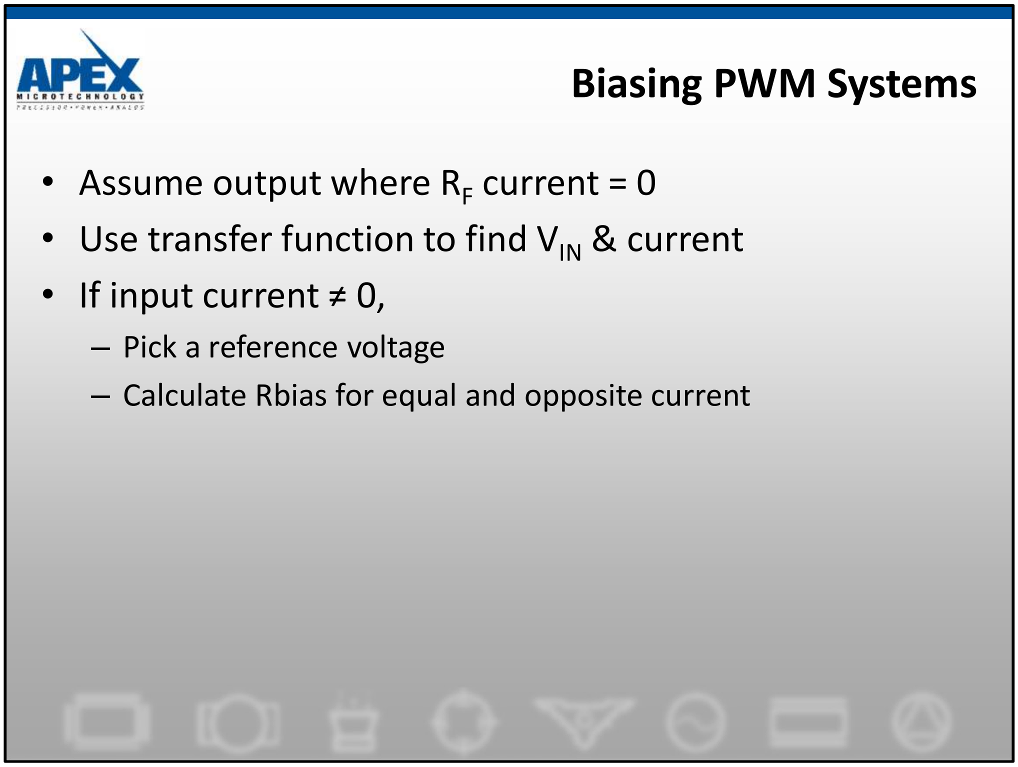
BIASING PWM SYSTEMS

Biasing PWM Systems

- Needed if:
  - 0 to 100V input, ±symmetric output
  - Bipolar input, half bridge amplifier
  - Single supply systems
- Reference Voltage
  - Common Mode Voltage limits
  - Allows ±swing of diff. amp relative to V_{REF}

When input, output and feedback voltages are all symmetric bipolar signals with respect to ground, no biasing is required.

More frequently, one of the items in this slide will be the case and biasing (offsetting or level shifting) will be required. The key to setting up biasing is to remember the integrator slides where a stable operating point is achieved when all currents to the summing junction total zero.



In the case of full bridges, current in the feedback resistor is usually zero when the bridge output is zero. The transfer function is simply the relationship from input voltage to bridge output voltage.

When feedback current is zero, the reference voltage and bias resistor need to feed the summing junction a current equal but opposite the current fed by the input signal and input resistor.

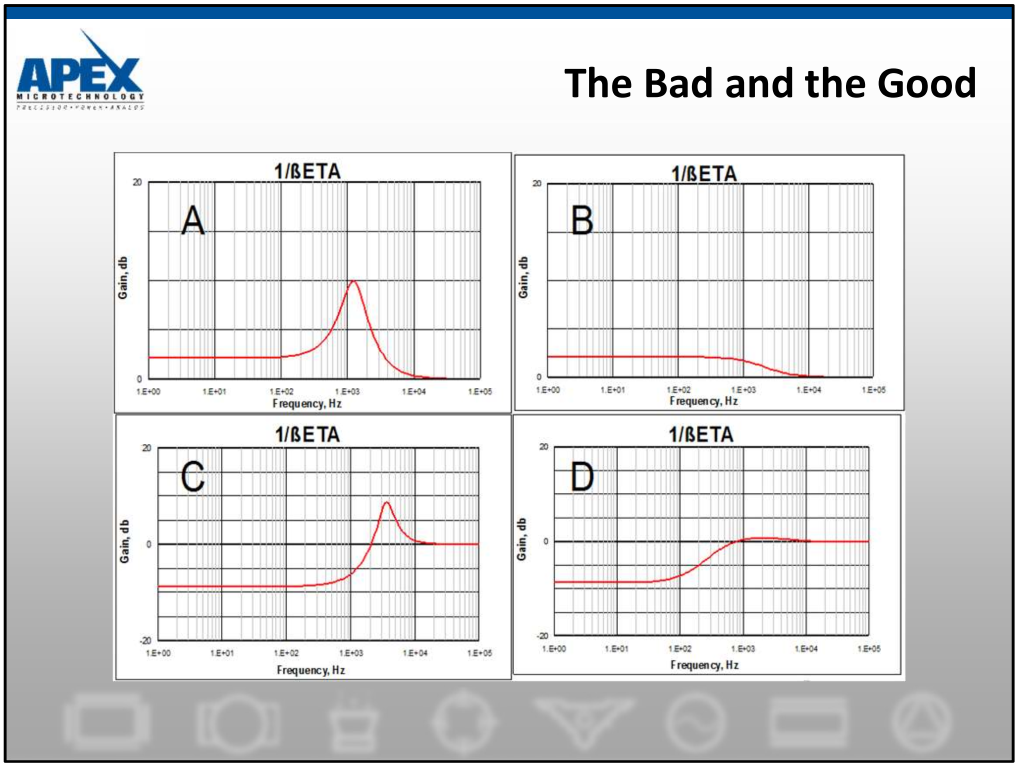
PWM Amplifiers & Stability

- Observe the integrator
- Calculate & plot 1/βeta, the feedback factor
  - βeta can be greater than 1
- Space poles & zeros to avoid high peaking
- Check the bandwidth

Linear design experience has taught many of us that as the number of stages or gain blocks in a loop increases, the probability of encountering a stability problem also increases. In a PWM system we typically have an integrator, the PWM power delivery block, a low pass feedback filter and often a feedback amplifier. This all implies that we need a technique to achieve a good design.

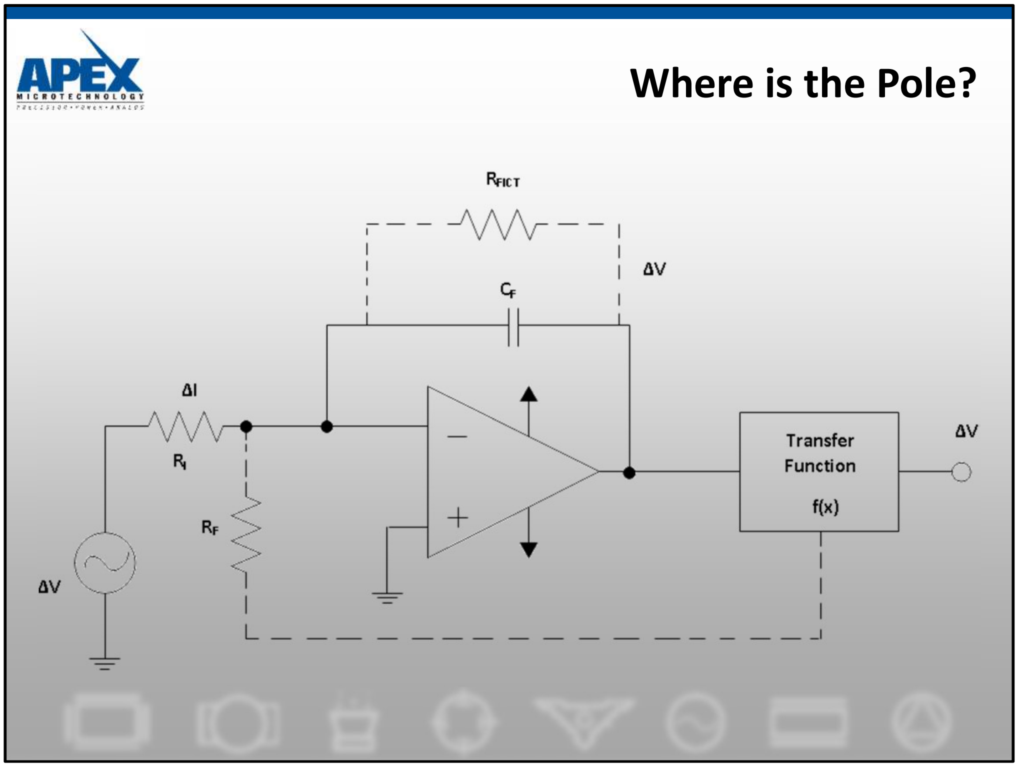
Our technique will be to calculate and plot 1/ßeta over frequency, and then minimize peaking. Assign an amplitude of one to the integrator output. Use the PWM transfer function to calculate the theoretical PWM output – ignore the fact that these are switching waveforms. Calculate around the feedback loop to the input of the integrator to find ßeta, the fraction of the output fed back. If there is a feedback path to the positive input, subtract this from the negative side feedback to find total feedback. Because there are gain stages in the feedback loop, it is possible to have a ßeta greater than one!

The major factor producing peaking is placement of the integrator pole too close to the poles in the feedback path. The integrator pole must be the dominant pole in the system. Setting the integrator pole frequency at 40% of the feedback pole frequency will provide good phase margins in low voltage circuits. With high voltage circuits, this percentage must decrease further.



Plots A and B examples of both peaking and non-peaking performance. Plot A resembles an op amp circuit with problems; low frequency 1/ßeta is positive, the peak spells trouble, and 0dB is approached at high frequency. Plot B is more what we want to see to insure stability; if bandwidth is not a concern, no peaking is desirable. When speed is a significant concern, some peaking will help, but at the expense of phase margin. For this case, peaking is defined as rise above the low frequency value.

Plots C and D are again bad and good, but for the case where low frequency 1/ßeta is negative. This will occur more often with the higher voltage amplifiers and it will be more difficult to eliminate all peaking without a severe penalty in bandwidth. The rise from the initial negative value to 0dB at high frequency is not part of the peaking we are looking for. For this case peaking is defined as only the rise above 0dB.

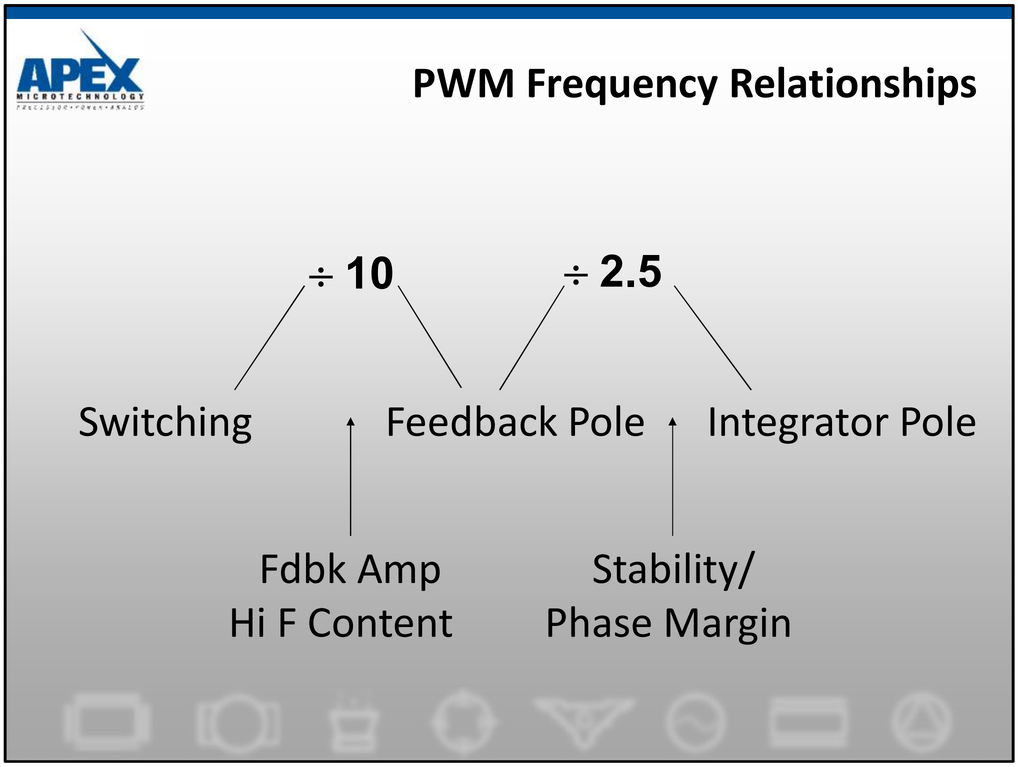


So, just where is the pole created by the integrator capacitor? As there is no resistor directly in parallel with this capacitor, the traditional calculation for an op amp roll off capacitor will not work. However, if such a resistor were in place (rather than our complex feedback loop), what would its value be? This fictitious value would result in the same change of integrator output voltage for a given change of input voltage, as occurs in the real system. To rephrase, if we know Δinput current to the integrator, Δoutput voltage of the integrator, then Ohms law dictates the effective feedback resistance must be ΔVOUT/ΔI IN. To answer these questions we need to know the input signal, the input resistor and how much the output of the integrator will move in response to the input signal.

To find this fictitious feedback resistor, assume a convenient input and use the given overall transfer function to find the PWM output voltage. Now divide by PWM gain to find movement of the integrator voltage.

$$R_{\mathbf{FICTITIOUS}} = R_{\mathbf{IN}} * \Delta\text{integrator} / \Delta\text{input} \quad (2)$$

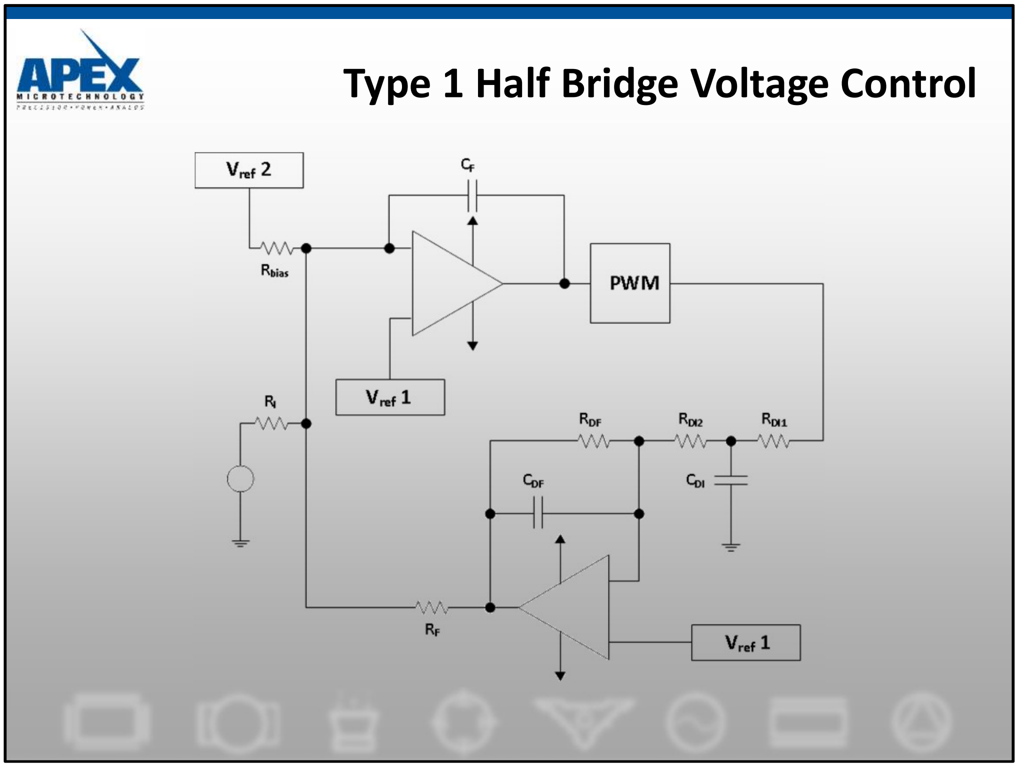
Using this fictitious feedback resistor, the pole frequency can be calculated just as if it were an op amp with parallel R-C feedback. When powering the SA01 (full bridge and 5V p-p ramp) on 75V, gain of the PWM block is 30. If the circuit is configured for a gain of 10 (say, ±5Vin, ±50Vout) and the input resistor is 5K, Δout =100, Δintegrator = 3.333, Δinput = 2, and the fictitious resistor is 1.67K. Even though the real RF may be 5KΩ, a 0.1µF capacitor produces a pole at 953Hz.



A reasonable starting place is to allow at least a decade between the switching frequency and the feedback pole frequency. This usually places the cutoff frequency of the power filter and the pole frequency of the feedback circuit at the same point.

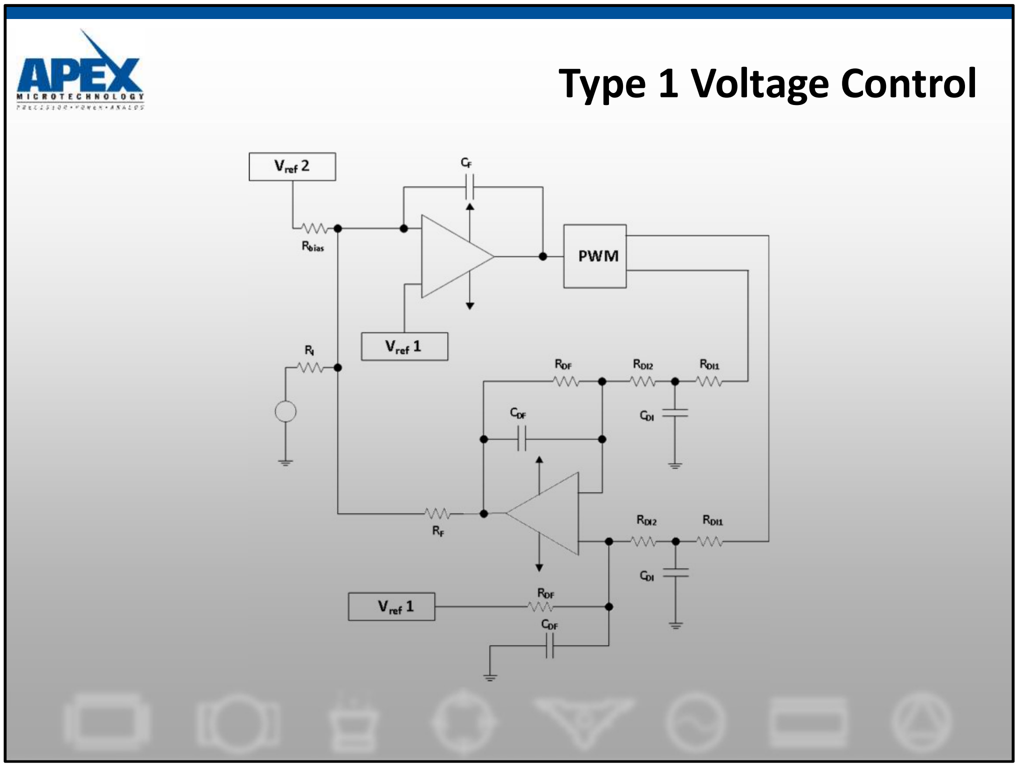
The low pass signal filter consists of one or more R-C pairs. If feedback is taken directly at the PWM output (by far the most common method), this filter sees a square wave input with peak-to-peak amplitude nearly equal to Vs. If feedback is taken after the power filter, phase shift of the power filter is added to the loop response. For this reason, a power filter inside the loop will be low Q and low attenuation.

The integrator pole frequency will be a fraction of feedback pole(s), the higher the supply voltage, the smaller the fraction that should be used.



Presently, Apex does not carry any more half-bridge PWM amplifiers in its products offerings; however, the slide is kept for explanatory purposes only

The voltage references shown are usually required when operating on single supplies, and may be required even when using dual supplies. Vref1 provides common mode headroom for single supply circuits and Vref2 handles biasing or level shift duties.



The Type 1 full bridge circuit requires a differential amplifier in the feedback path. Side-to-side component matching for the difference amplifier is VERY important. The impedance of Vref1 needs to be at least two orders of magnitude less than Rdf, AND needs to handle current in both directions. Vref2 may be positive or negative.

Even with the poles of the difference amplifier, it will be subjected to AC voltage at the switching frequency. These high frequency signals should be rejected, and even more importantly, they should not be allowed to create errors which look like voltage offset. Therefore, this op amp needs good high frequency common mode rejection. The LF353 data sheet indicates 80dB rejection at 100KHz, making it a good choice.

Gain of the difference amplifier is almost always less than unity. Swing capability, common mode range and PWM supply voltage place limitations on the maximum gain.

General Operating Levels #1

Desired Values:		Operating points:		Ideal operating:	
Zload	10	Vramp p-p	4	Rdi total KΩ	125
Vout high, V	110	Vin ma p-p	2	PWM gain	43.75
Vout low, V	10				
Vin high, V	10			Actual operating:	
Vin low, V	0			Eff PWM gain	43.061
		Vref1, V	10	O/A gain	10
Vs, V	175	Vref2, V	5	Diff gain	0.04
Ri KΩ	5	diff V high, V	12	1/Diff gain	25
Rdf KΩ	5	diff V low, V	3	Int Vos gain	15
Diff poles KHz	2	Suggestions		diff CMV hi, V	10
Int pole KHz	0.4	0.8		diff CMV lo, V	10
				diff out hi, V	10.4
	Actual	Suggestions		diff out lo, V	3.4
Rbias KΩ	-2.5	-2.5		Rdi leg mA	1.2692
Rf KΩ	2	2		Rdi1 watts	0.6738
Rdi2 KΩ	113.64	113.6363636		Rdi2 watts	0.1831
Rdi1 KΩ	11.364	11.36363636		Eff Rf	1.1429
Cdi nF	7.0028	7.002817496		Diff pole i KHz	2
Cdf nF	15.915	15.91549431		Diff pole f KHz	2
Cf nF	348.15	348.151438		Int pole KHz	0.4
Phase margin °	38.162			Vout hi, V	110
Peaking, dB	2.3068	F @ peak Hz	865.964	Vout lo, V	10

Here's the given data for this example: SA14 half bridge operating on 160 to 175VDC; Switching frequency = 22.5KHz ; VRAMPp-p = 4V; Vcc = 15V; Input signal = 0 to 10V; System does not have a negative supply; Output = 10 to 110V, up to 10Hz
***SA14 is not available, but slide is kept for example purposes**

The topology is Type 1 half bridge and initial data entry into Power Design is shown. The op amp is LF353. That data sheet indicates worst case common mode voltage range of 4V from the rails and minimum output swing of 3V from the rails for a 10KΩ load. The 3V restriction was entered as diff amp high and low limits because common mode voltage for a half bridge will be VREF1. Knowing voltage references for 15V supplies are readily available with 10V outputs and that setting VREF1 close to the upper diff amp voltage limit maximizes its swing capability, 10V was entered for VREF1. It was assumed a lower VREF2 could be easily generated. The 5KΩ values for Ri and Rdf seemed a good starting point. Diff amp poles are often placed a decade below FSW, but in this case they are half that because we have no bandwidth problem and lower pole frequencies mean less high frequency energy fed to the diff amp. The integrator was also set in a conservative manner. The Load Green Suggestions button was used.

Right away, we have a warning in the form of a negative value bias resistor (red). If you keep these in stock, skip to the next slide. The rest of us will make a note to switch our reference voltages. To the right, we find our smaller diff amp input resistor getting a little warm. Simply changing the diff amp feedback resistor can scale these input resistors. Increasing these resistors will also decrease the two diff amp capacitors.

Vref Change Lowers Vos Sensitivity

Vref1, V	5	O/A gain	10
Vref2, V	10	Diff gain	0.0114
diff V high, V	12	1/Diff gain	87.5
diff V low, V	3	Int Vos gain	108.5

A

Vref1, V	7.5	O/A gain	10
Vref2, V	10	Diff gain	0.0257
diff V high, V	12	1/Diff gain	38.889
diff V low, V	3	Int Vos gain	79.889

B

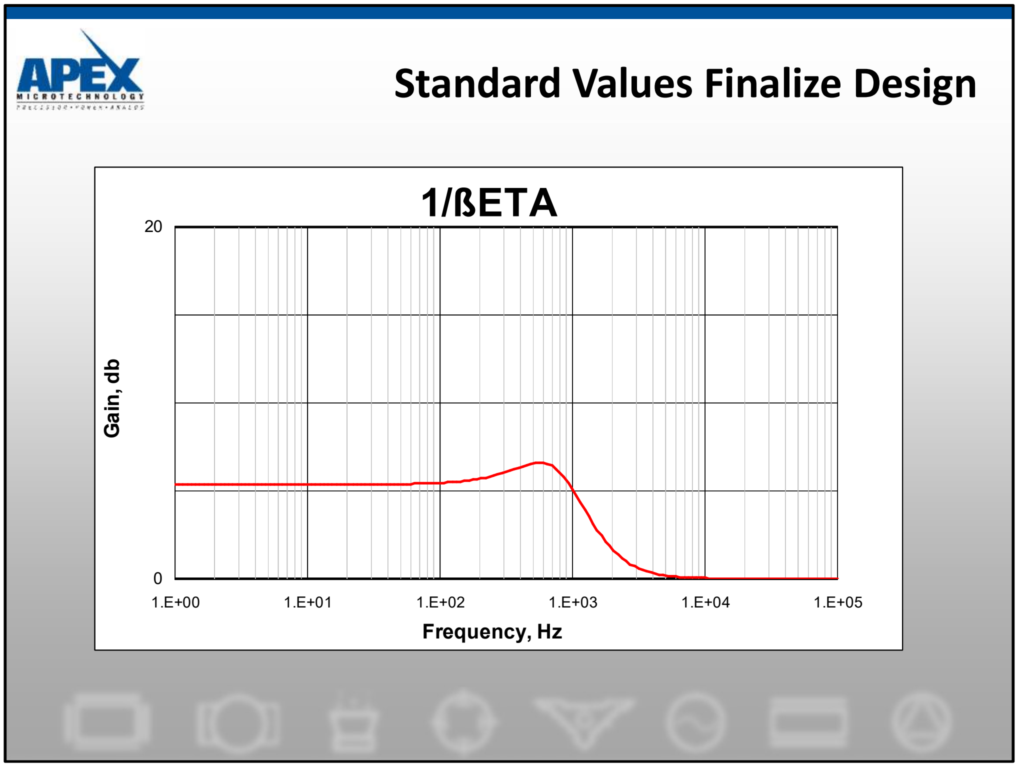
In section A, we find that the switched voltage references will work (after loading green suggestions), but because the resulting diff amp swing is considerably smaller than the available range, our DC error budget is being inflated. Output error due to the voltage offset contribution of each op amp can be calculated with the gain values in the two lower right cells. By changing VREF1 to 7.5V (and loading green suggestions), we reduce the effect of integrator offset about 25% and the effect of the diff amp offset is lowered better than 2:1. There's nothing unique to PWMs here, just DC op amp circuit solutions.

Be aware that while not shown here, all the suggested resistor and capacitor values change when the reference voltages changed.

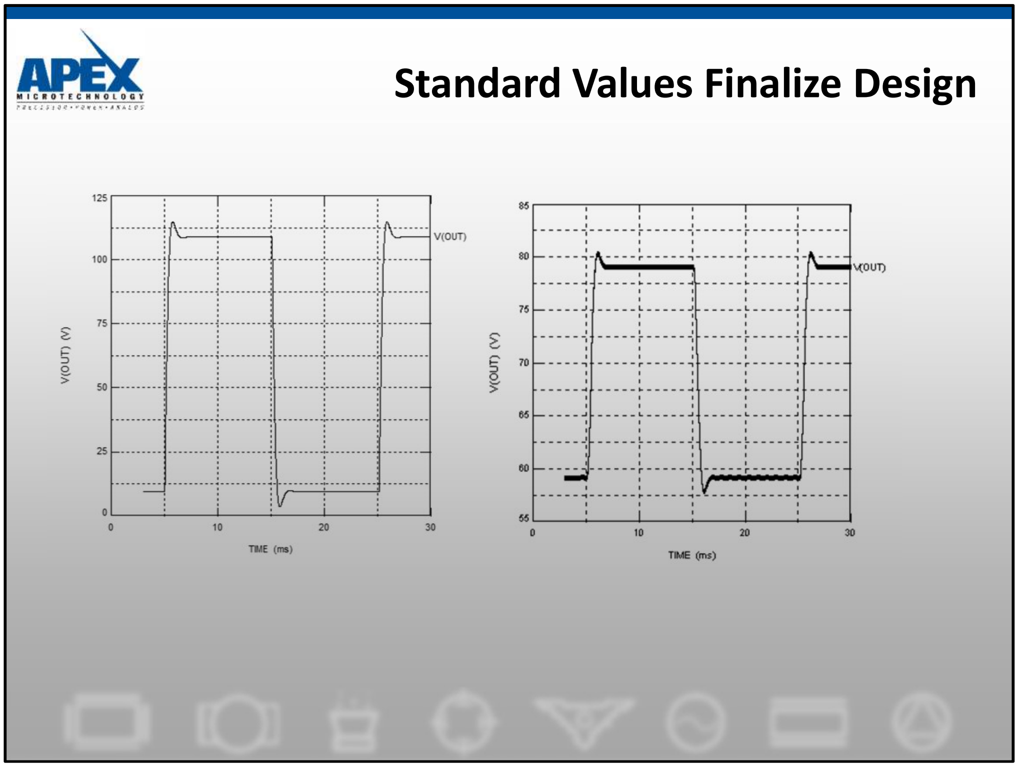
Standard Values Finalize Design

Desired Values:		Operating points:		Ideal operating:	
Zload	10	Vramp p-p	4	Rdi total KΩ	396.67
Vout high, V	110	Vin ma p-p	0.66667	PWM gain	43.75
Vout low, V	10				
Vin high, V	10			Actual operating:	
Vin low, V	0			Eff PWM gain	43.061
		Vref1, V	7.5	O/A gain	9.938
Vs, V	175	Vref2, V	10	Diff gain	0.0257
Ri KΩ	15	diff V high, V	12	1/Diff gain	38.922
Rdf KΩ	10.2	diff V low, V	3	Int Vos gain	79.851
Diff poles KHz	2	Suggestions		diff CMV hi, V	7.5
Int pole KHz	0.4	0.8		diff CMV lo, V	7.5
				diff out hi, V	7.6927
	Actual	Suggestions		diff out lo, V	3.1965
Rbias KΩ	4.81	4.838709677		Rdi leg mA	0.4113
Rf KΩ	3.83	3.857142857		Rdi1 watts	0.2127
Rdi2 KΩ	361	360.6060606		Rdi2 watts	0.0611
Rdi1 KΩ	36	36.06060606		Eff Rf	3.4073
Cdi nF	2.2	2.210485321		Diff pole i KHz	2.0095
Cdf nF	10	7.801712897		Diff pole f KHz	1.5603
Cf nF	100	116.7747883		Int pole KHz	0.4671
Phase margin °	43.324			Vout hi, V	109.82
Peaking, dB	1.2463	F @ peak Hz	562.341	Vout lo, V	10.444

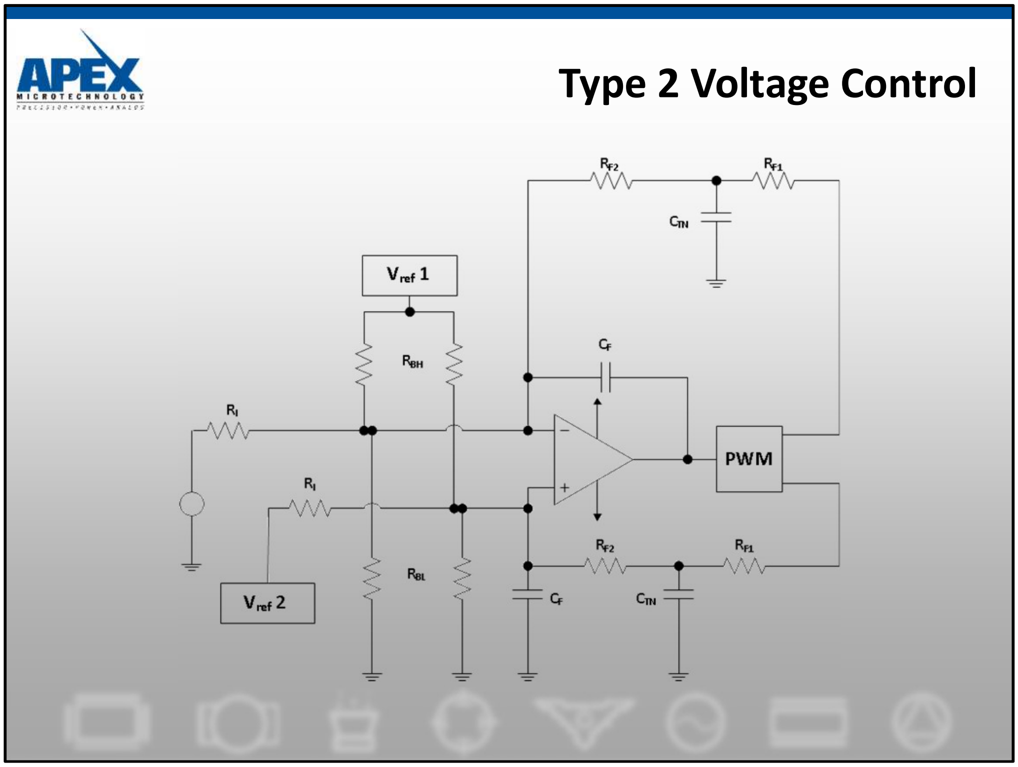
Here are the results of the other changes and working with standard value charts a little. There are many component combinations that could yield DC output accuracy within a few percent and provide adequate phase margin. This design will take advantage of the fact that the smaller diff amp input resistor can be a 5%, ½W type and still only affect gain by about 0.5%. Offset adjustment could be accomplished by varying either reference voltage or by adjusting the bias resistor. It is also possible to include a gain adjustment with the input resistor, the main feedback resistor, the diff amp feed back resistor, or its input resistors. Note that when using a full bridge amplifier, the feedback amplifier is fully differential and gain adjustment is practical in this stage only with difference amplifier circuits having a dedicated single resistor gain adjustment.



Our circuit is quite well behaved. The 1.25dB peaking corresponds to about 43° phase margin.

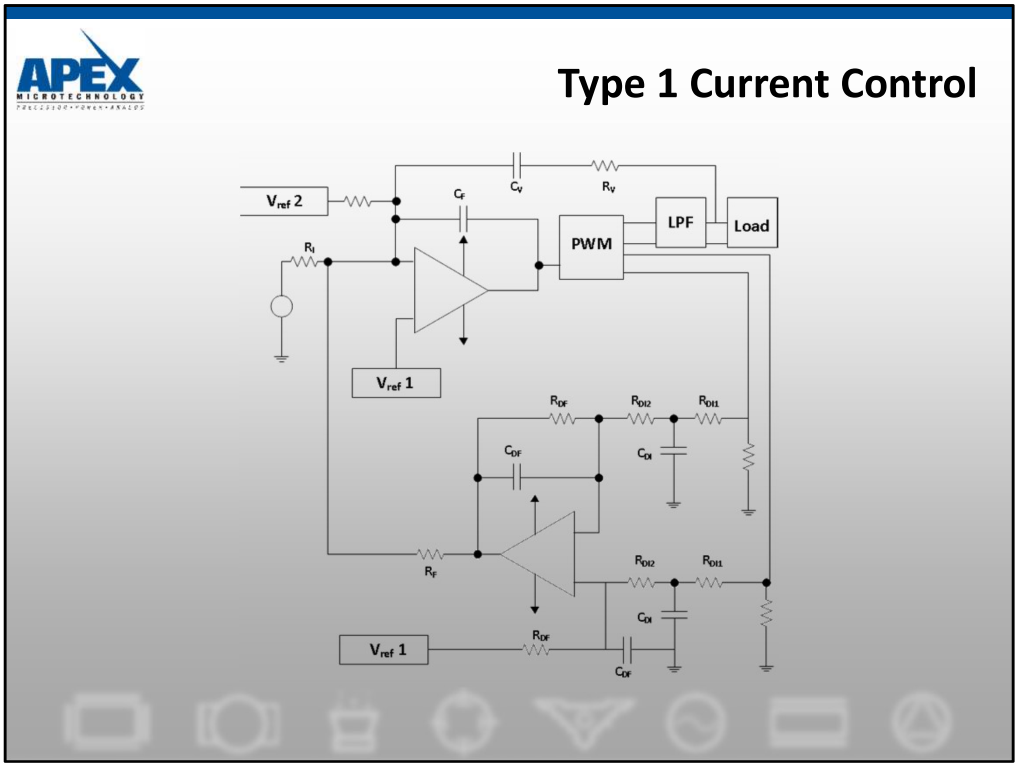


Both of these Spice model simulations agree with Power Design in predicting a stable circuit. On the left is the output of a state average Spice model simulation which took 8 seconds on a 759MHz PC. With this speed, it is painless to run a variety of component values. On the right we see output from pulse-by-pulse macro model requiring 45 minutes to run. Simulation times will vary substantially with machines, Spice platforms and run options. In any event, you will want to zero in closely on low frequency performance prior to attempting to examine switching performance.



The simple voltage control circuit is shown as inverting, but non-inverting or full differential operation is possible as long as common mode voltage for the op amp is analyzed. Just as in the four resistor op amp difference circuit, accuracy concerns demand that the resistors and capacitors on the two sides be matched.

Example 1 in AN41 covers this circuit in detail.



Schematically there are two differences between this current control circuit and the Type 1 voltage control circuit: The difference amplifier connects not to the outputs, but to the current sense pins of the PWM amplifier; and there is an additional voltage feedback path at the top of the schematic.

Operationally, the filter, the matching network and the load are INSIDE the feedback loop and therefore become a significant element of stability analysis. Matching networks are often set to a higher than textbook impedance values (or omitted) because their current is included as part of the controlled output, but this current is not delivered to the load. As the filter contributes negatively in the stability analysis, it is often far from the textbook filter (designed to only knock off sharp edges), and sometimes is omitted altogether, leaving the load to do all the filtering.

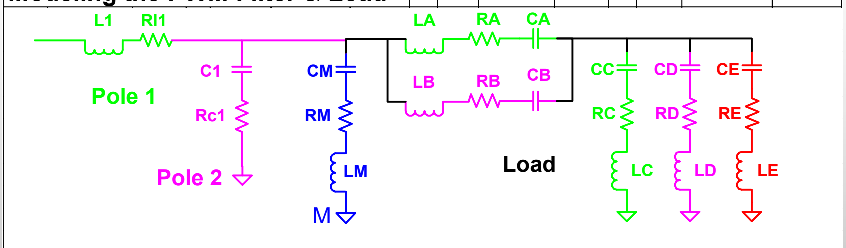
If the load contains moving parts, the mechanical factors need to be equated to electrical parameters prior to analyzing the system.

When given application requirements are only in terms of output current and load impedance, the first stop is usually the linear Power sheet, where these terms can be entered to easily find drive voltage requirements (output voltage will be correct no matter what supply voltage or amplifier is specified).

The next design step is usually the PWM Filters sheet where the matching network and filter are designed and then sent to the PWM Power sheet for check and modification.

Current Control Includes the Filter & Load

Modeling the PWM Filter & Load

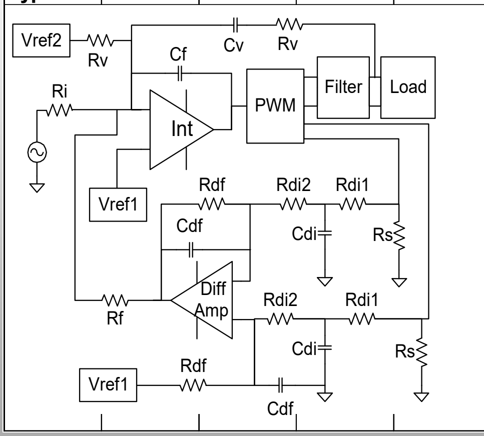


Pole 1				Matching Network				Load				CC	0	uF
L1	0.1	mH		CM	3.3	uF		LA	0	mH		RC	0	ohms
Rl1	0.032	ohms		RM	18	ohms		RA	0	ohms		LC	0	mH
				LM	0	mH		CA	1E+15	uF				
												CD	0	uF
Pole 2								LB	0	mH		RD	0	ohms
C1	1	uF						RB	0	ohms		LD	0	mH
Rc1	0.05	ohms						CB	1E+15	uF				
												CE	1E+15	uF
												RE	9	ohms
												LE	0.3	mH

Here we see the filter/matching network/load definition area of the Power Design PWM Stability sheet. This is “must have” data for current control. You have the option of entering the data one element at a time, but the “Extract” command button grabs values from the PWM Power sheet- - If you used that for checking voltage mode peaking. If you started in the PWM Filters sheet, the load inductance will be in the lower right cell.

Setup for Sense Pin Control

Type I1	Readme	SA12	

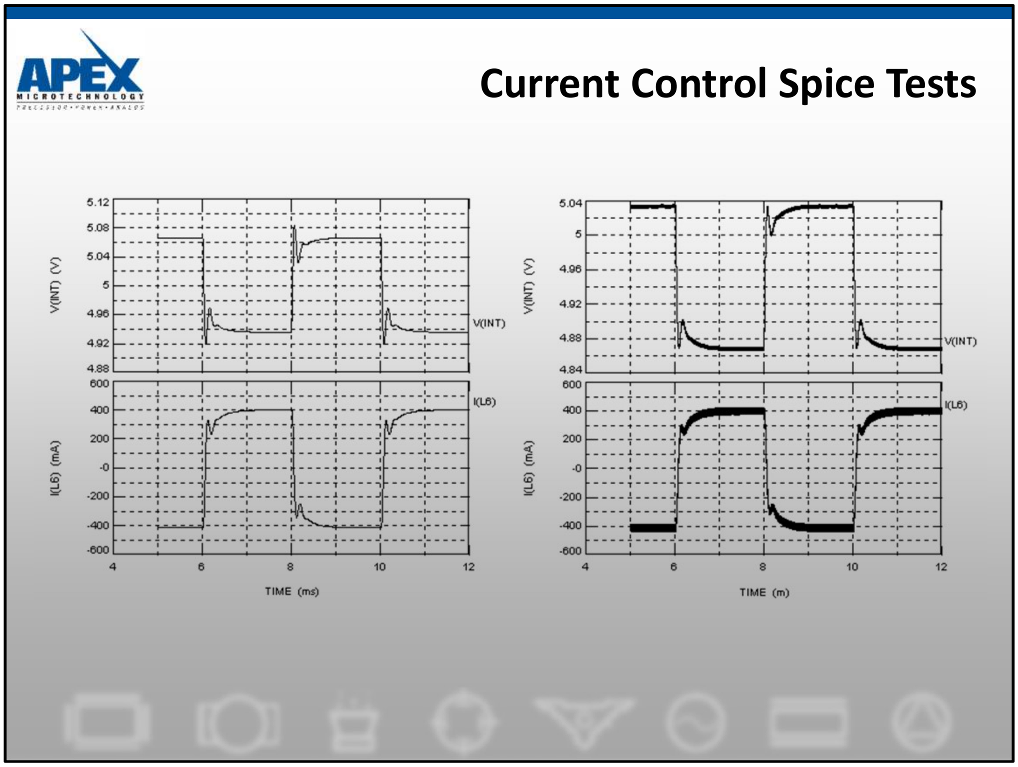


Desired Values:		Operating points:	
Iout high, A	10.2	Vramp p-p	4
Iout low, A	-10.2	PWM gain	60
Vin high, V	7.5		
Vin low, V	2.5	Vref1, V	7.5
Vs	120	Vref2, V	0
Ri KΩ	1	diff V high, V	12
Rs Ω	0.1	diff V low, V	3
Rdf KΩ	10		
Diff poles KHz	20	Suggestions	
Int pole KHz	5	8	
	Actual		
Rbias KΩ	9.3	-3	
Rf KΩ	1	1.8	
Rdi2 KΩ	3.3	3.709090909	
Rdi1 KΩ	0.33	0.78	
Cdi nF	100	24.11438532	
Cdf nF	3.3	0.795774715	

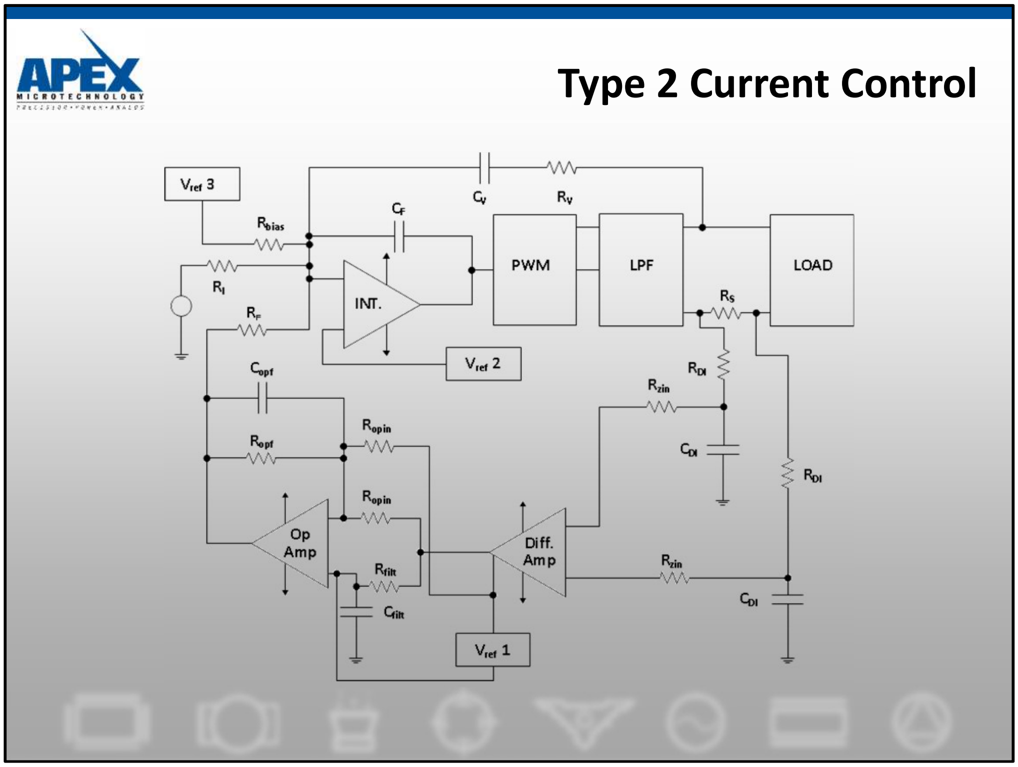
By now we know the outputs, inputs and the supply. Choose the input resistor high enough for the signal source to drive, and low enough to avoid parasitic problems- -1K to 10K is common. There are two lines of logic on selecting sense resistor values: a) develop 100mV on the Ilimit pin at maximum output current (the typical value used to activate current limit, or 2) develop 1V on the Isense pin at maximum output current (above 1V may affect control of the output switch). Option 2 results in better accuracy and wider bandwidth.

The acceptable range of values for the difference amplifier feedback resistor is wide. Lower values will require larger roll off capacitors, higher values call for smaller capacitors and can allow too much influence by parasitics. You be the judge how large to go with the capacitors, but let me suggest they never go below 100pF.

The ideal place for Vref1 is usually the center of the difference amplifier input and output limitations. If required, Vref2 should be several volts away from Vref1. If a negative value in red appears as a suggestion, switch Vref2 polarity with respect to Vref1.



Here are the state average and pulse-by-pulse spice runs on our example. If we were to lower impedances of Rv and Cv, the leading edges of the square wave will become more rounded. Increasing those impedances will sharpen up the leading edges, at the expense of phase margin.



If the PWM amplifier has only one sense pin or if current in the filter or match network are adversely affecting output accuracy, the Type 2 current control circuit may be best. Notice that phase shift introduced by the filter is now INSIDE the feedback loop. Filters in this configuration are usually of low order and often have a cutoff frequency at or even above the switching frequency (the load is doing most of the filtering).

The difference amplifier is often a gain of one, giving rise to the need of an op amp gain stage. This stage is not usually included if the difference amplifier can provide enough gain. When used, it may be inverting or non-inverting (diff amp inputs can easily be switched to provide correct phase feedback).

The rest of the circuit is similar to Type 1 and spreadsheet comments will guide you through the design process. Note that the input voltage to the difference amplifier will be as high as the supply voltage.

Current Out Stabilizing Steps

- Filter: no more than 10dB Vmode peaking
- Enter Filter/Load-except NO inductance
- Stabilize with up to 10dB peaking
  - Need high values for Cv & Rv
- Re-enter load inductance
- Selected Rv and Cv
- Check with Spice and the bench

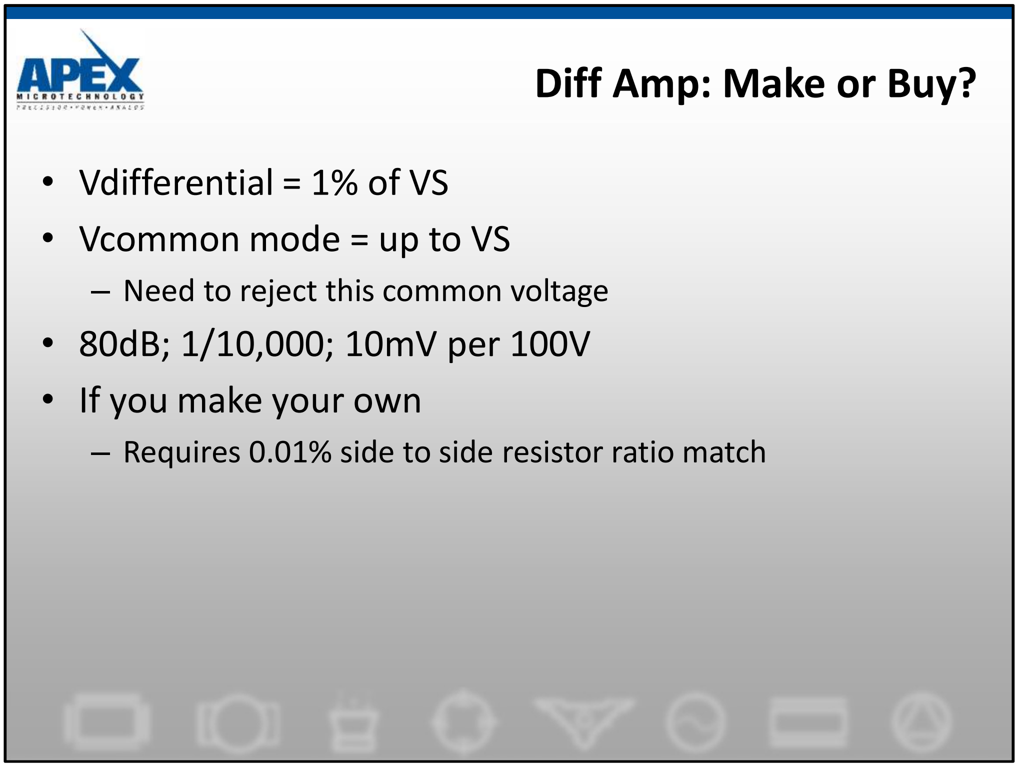
Vmode peaking is in the PWM Power sheet.

Move to the PWM Stability sheet.

Stabilize with no inductance & no voltage feedback network.

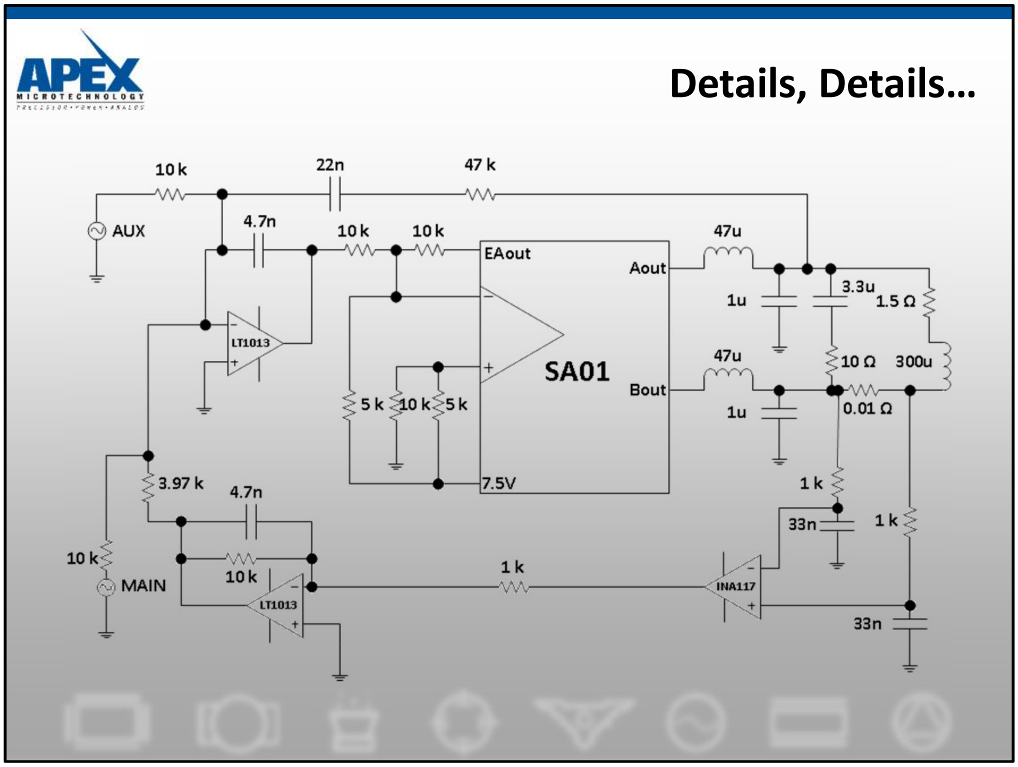
Re-enter inductance & stabilize with the voltage feedback network.

Check and revise as needed.

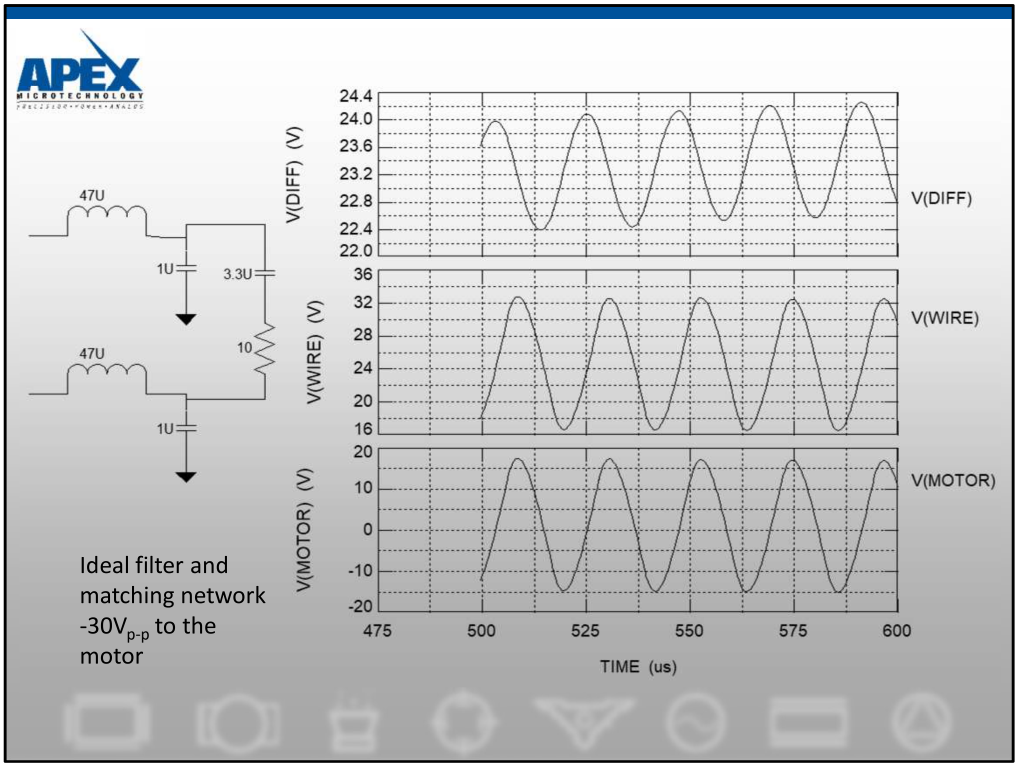


The required accuracy levels and circuit efficiency both play a role in this decision. Efficiency concerns ask for a sense resistor as small as possible- -meaning a small differential voltage. However, difference amplifier input errors (voltage offset and common mode rejection) must be small compared to the sense voltage to achieve high accuracy.

Here are a few numbers to illustrate the importance of common mode rejection. Assume Vs=100V, sense voltage=1V and CMRR=80dB. The actual common mode error at 100V swing is 10mV. This is a 1% error compared to the sense voltage. Resistor match required to achieve 80dB is 0.01%. These match requirements speak positively for the buy option for the diff amp.



This is an example from Application Note 41, where biasing and stability are covered. Four filter/match network options are covered, which all produce similar results with the square wave stability test. The next four slides are concerned with system RFI.



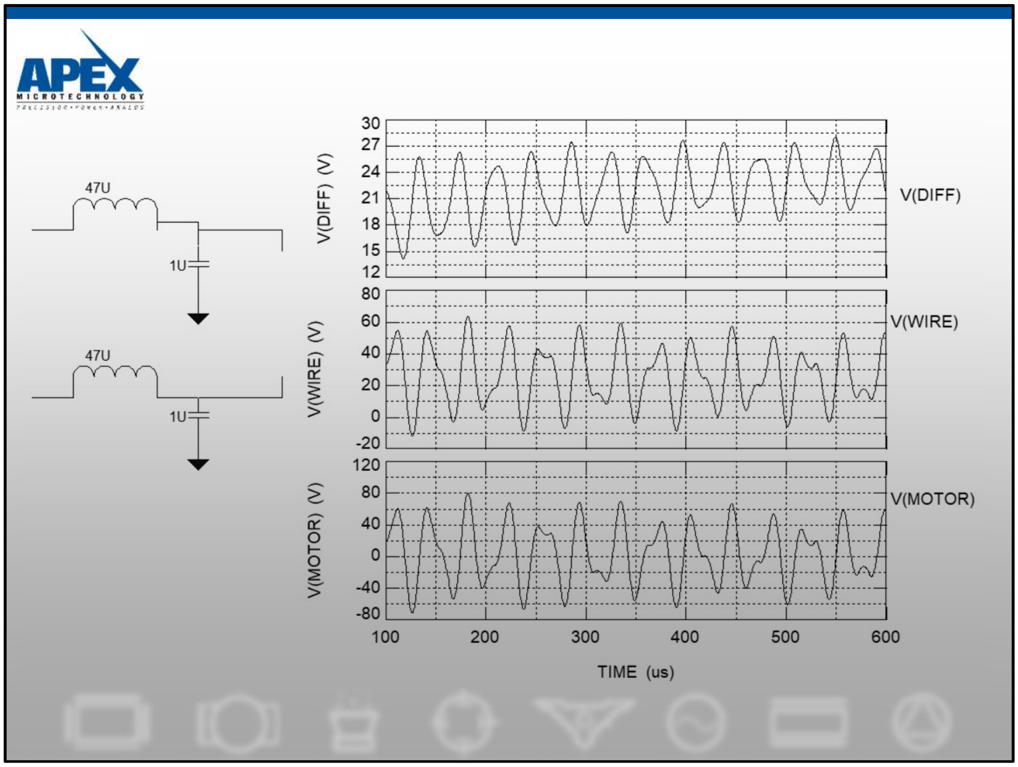
All the simulations are at zero drive current (50/50 modulation).

In this "best" design, all waveforms are basically a sine at the switching frequency of 42kHz.

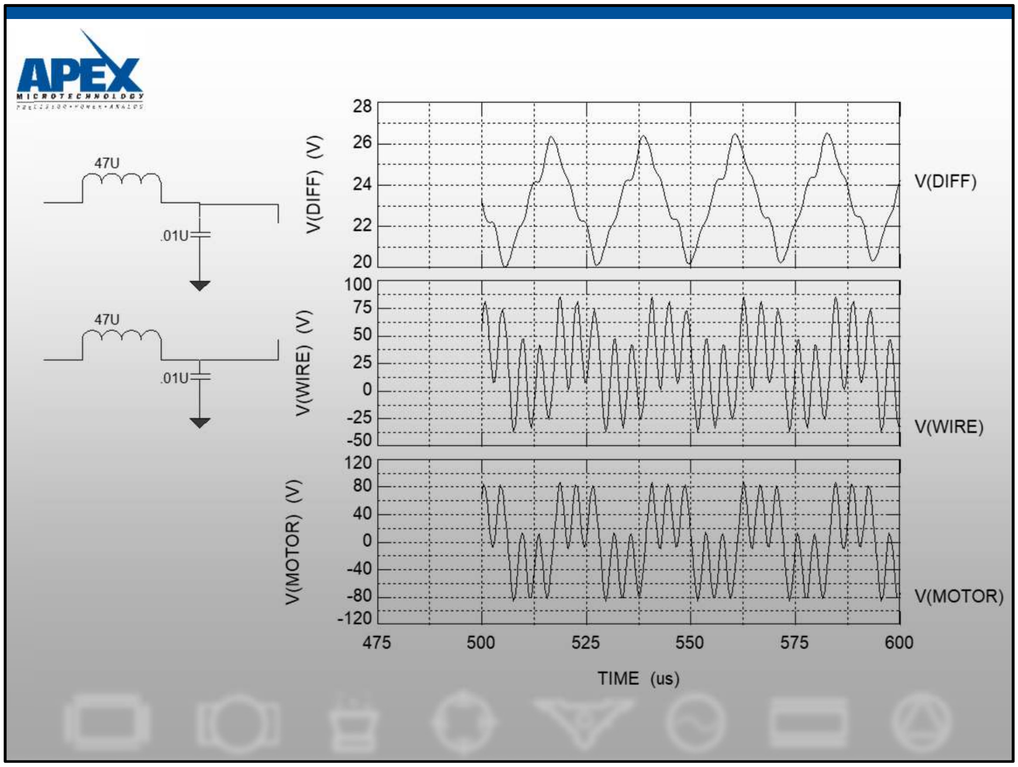
At the top is the common mode voltage applied to the diff amp input pins.

In the middle we see voltage with respect to ground on the wires connecting the amplifier to the motor; read this as transmission antenna.

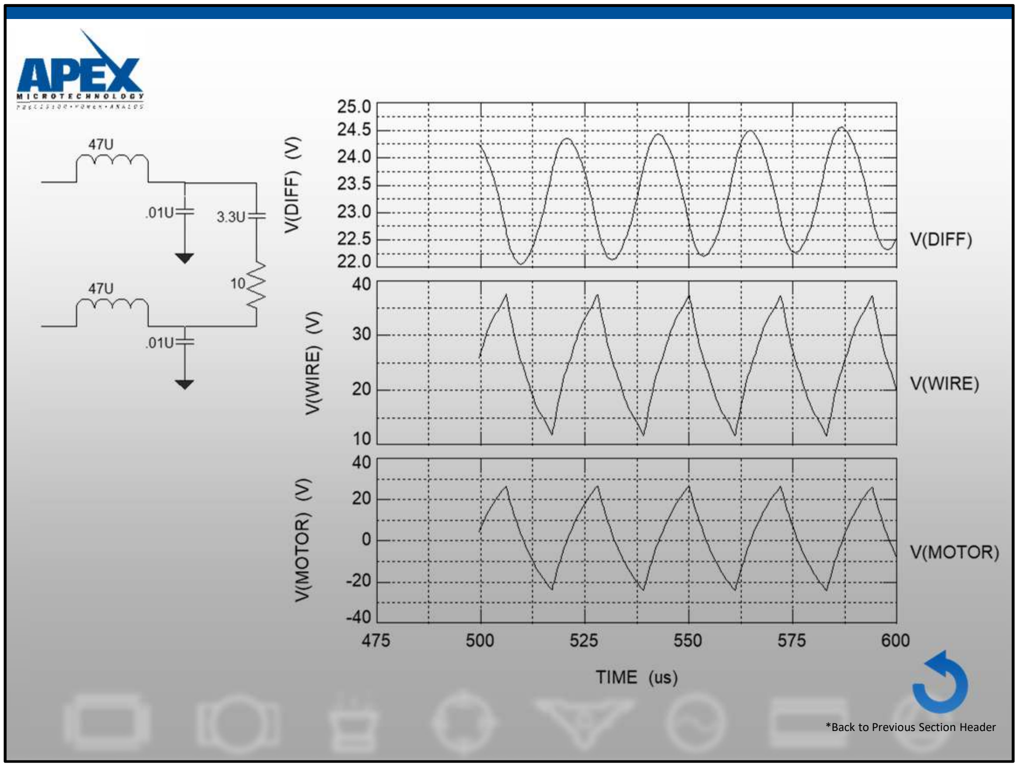
On the bottom is the voltage applied to the motor



In this option, the matching network was removed. Note the time scale has changed 4x. There is now major signal content at about 25kHz. While it is difficult to say what the RMS values are, a good guess is that they all increased a factor of 2.5. This might be a good time to check motor temperature.

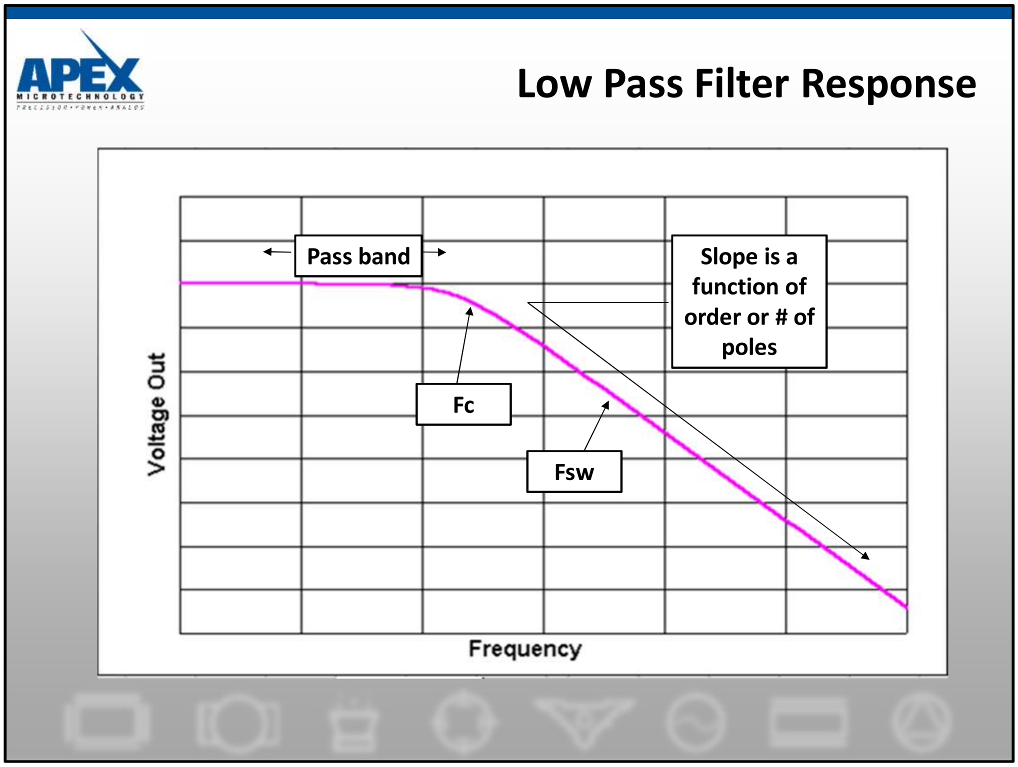


The matching network is still gone, and the filter capacitors have been reduced significantly. Common mode voltage seen by the diff amp is mostly a triangle and peak amplitude is up by a factor of about four. Voltage on the transmission line and across the motor has gone up and now has a significant content at about 220kHz!



Using an undersized filter capacitor with the matching network results in wire and motor waveforms with higher than optimum amplitude and worse yet, they contain considerable high frequency energy (read this as a radiation problem).

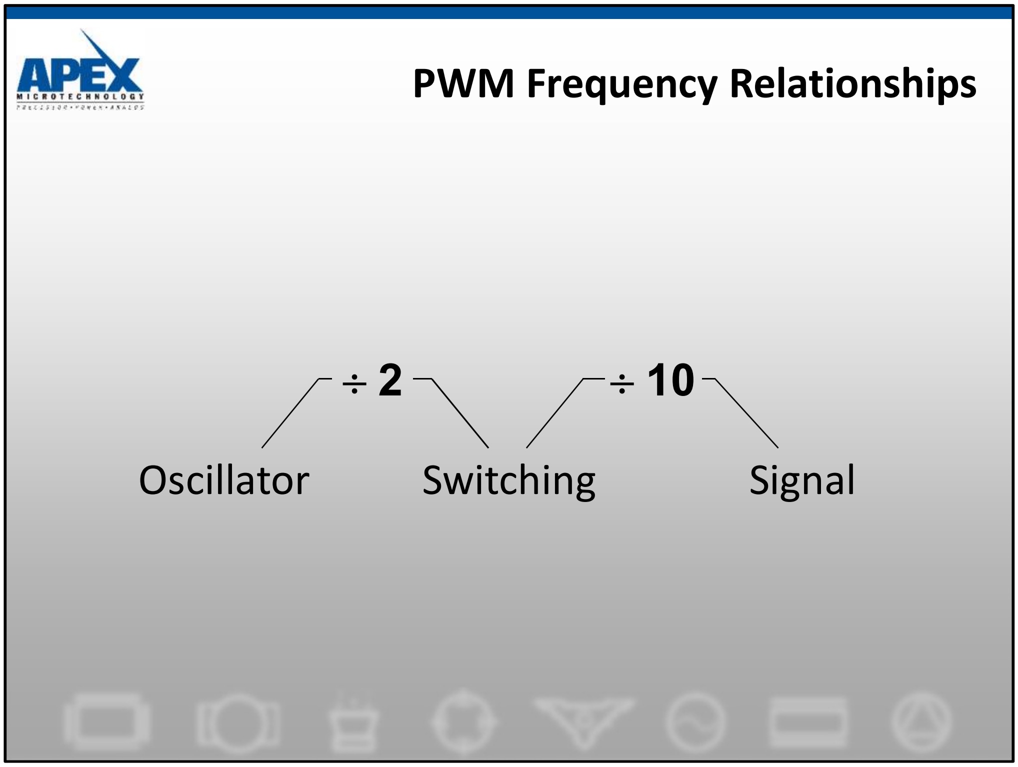
LOW PASS FILTER RESPONSE



PWM filters are normally low pass configuration. These exhibit low attenuation to the frequency spectrum from 0 Hertz to the frequency of cutoff (Fc). This low attenuation region is called the pass band. Beyond the Fc, attenuation increases at a rate determined by the filter type and the numbers of poles (order).

As we speak of the “frequency” of a PWM signal it is very important to realize what area of this response curve is being referred to. In the pass band area, signals are slow and can be thought of as analog. The switching frequency will be well beyond Fc, can be thought of as the carrier frequency containing time modulated digital information. A reasonable analogy for the filter function might be the audio CD technology where high speed DACs translate digital data to analog output, where the D-to-A conversion rate corresponds to switching frequency. Going even further out in frequency, where the high speed transitions of the PWM amplifiers generate spikes, it is best to think of RF energy.

Ref. AN32,AN39



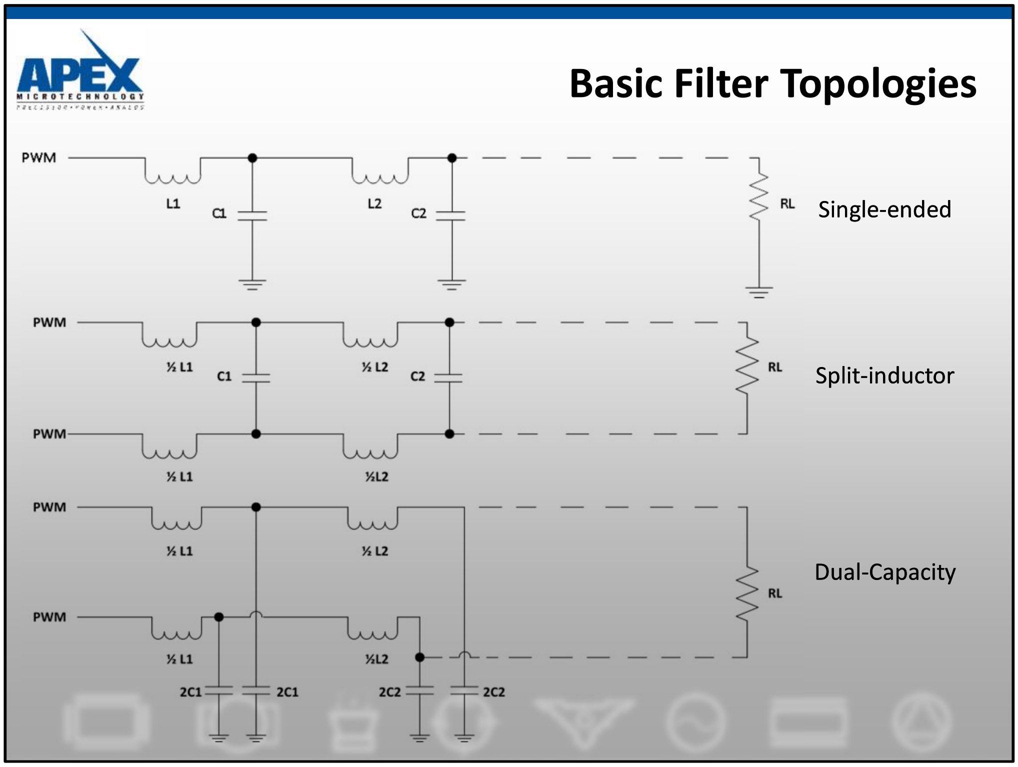
The common ramp generator illustrated the relationship between oscillator and switching frequencies. Some PWM data sheets (such as the SA01) do not mention oscillator frequency because there is no divide by two circuit.

Signal frequency is that of the power drive to the load, power bandwidth. Between the load and the PWM amplifier is the low pass filter (or at least the model of one if the load is also the filter). On the input side of the filter we have the switching frequency. We then go down the slope to a point where the attenuation is adequate. The frequency band we cover while going down the slope is required spacing between the switching and signal frequencies.

Pure theory says filter slope can be increased simply by adding more poles. This is true to a point. We would probably question an eight pole filter in the small signal world. Do you really need that? Can you find high enough quality components to make it work? Can you afford it in terms of size and cost?

In the PWM world these questions are not only valid but are many orders of magnitude more important because power levels have gone from mW to KW! Rule of thumb: Allow a decade between switching and signal frequencies.

Ref. AN32,AN39



No matter what topology is used, a first order filter would use only L1, a second order adds C1, a third order adds L2, and so on. Each pole of the filter adds 20dB/decade to the slope or roll-off of the filter.

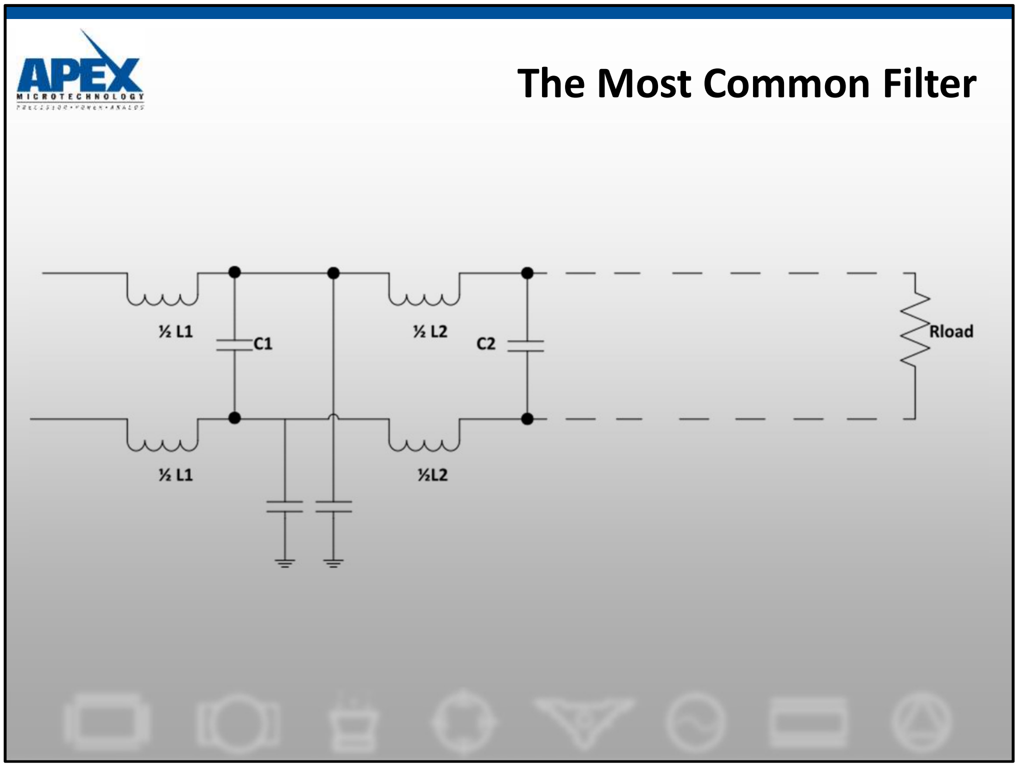
The single-ended filter configuration is the simplest; must be used with half bridge circuits; and can be used with full bridge circuits by substituting the second PWM output for all the ground connections. This substitution is very rarely done because it places the high speed square waves of the PWM output on both load terminals and all the cabling between the amplifier and load. With rise and fall times usually in the tens of nanoseconds, and amplitude nearly equal to supply voltage, this is an extreme RFI problem.

With full bridge circuits, an additional filter requirement is introduced in that common mode voltage applied to both load terminals usually needs to be minimized. The technique to achieve low common mode voltage is to simply split the inductor values in half, applying half to each PWM output as shown in the split-inductor topology.

Capacitors of the split-inductor topology must be capable of bipolar operation and will be very large when the filter is designed for both high current and low signal frequency. While the bipolar capacitors exhibit very low ESL and ESR to provide good roll off in the high frequency spectrum, this leads to very large and expensive banks of capacitors. The dual-capacitor topology can provide a cost savings, at the expense of high frequency performance, by substituting a pair of electrolytic (or possibly tantalum) capacitors of twice the size. To convince yourself this a valid substitution, forget the ground connection and think of two series connected capacitors in place of one. This substitution usually allows the use of unipolar capacitors.

If one could acquire a perfect PWM amplifier (equal rise and fall times, no dead time plus an exact out of phase condition) and perfectly matched inductors, current through each of the dual capacitors would be equal and phased such that no current would flow into the ground node. Even with these imperfections, the ground node current will be a small percentage of the capacitor

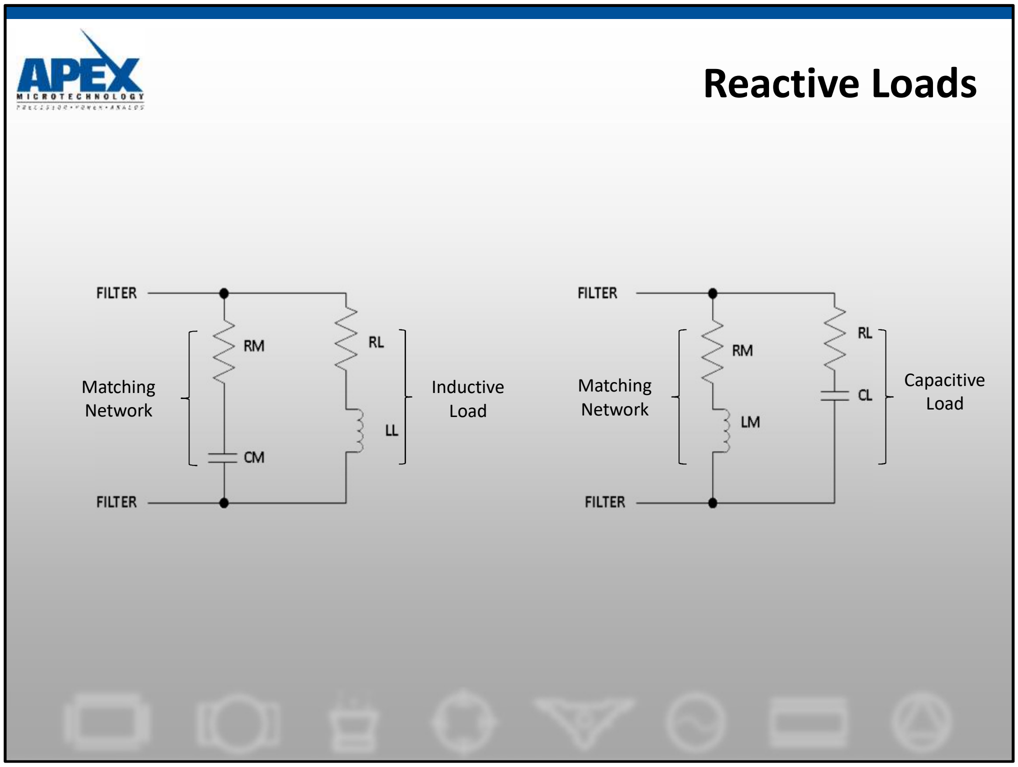
current.
Ref. AN32



If we apply our previously mentioned fantasy of perfect components to the split inductor filter topology, common mode voltage on the load terminals will be zero. With real PWM amplifiers, the output will contain large amounts of high frequency harmonics. Each application is different, but peak-to-peak noise amplitude may approach the supply voltage. The spectral content of this noise extends well above the switching frequency. A pair of small capacitors added from the output side of each half of L1 to ground will remedy this problem. It is not necessary (and sometimes it is counterproductive) to use more than this one pair of leg capacitors. Placing these small capacitors on the load side of L2 or L3 is not as effective as the placement shown.

Value selection for these ground leg capacitors is less critical than for the main filter capacitors. It has been determined empirically that setting the impedance value of these capacitors at the cutoff frequency, to between 10 to 30 times the value of the load resistance will provide reasonable common mode filtering. The addition of these capacitors will typically produce no more than 0.05dB peaking, nor more than 0.2db change at the cutoff frequency in any order filter. From the technical point of view, the two Clegs are in series, and this is in parallel with C1. This means that on all but first order filters, C1 could be reduced by half the value of Cleg to eliminate even these small errors.

Ref. AN32



To achieve even close to these ideal filter responses a constant and purely resistive load termination is required. If a reactive load can be modeled as resistance in series with either capacitance or inductance, a simple conjugate match network can be used to achieve proper termination. The resistor in the network will equal the resistor of the load model. As the network is in parallel with the load, all signals in the pass band will be applied to the network and power dissipation must be checked. Realize that combined impedance of the network plus load is constant and that changing frequency shifts the power between the network and the load. This means a 100W capacitive load drive will require a 100W matching network if DC signals are allowed.

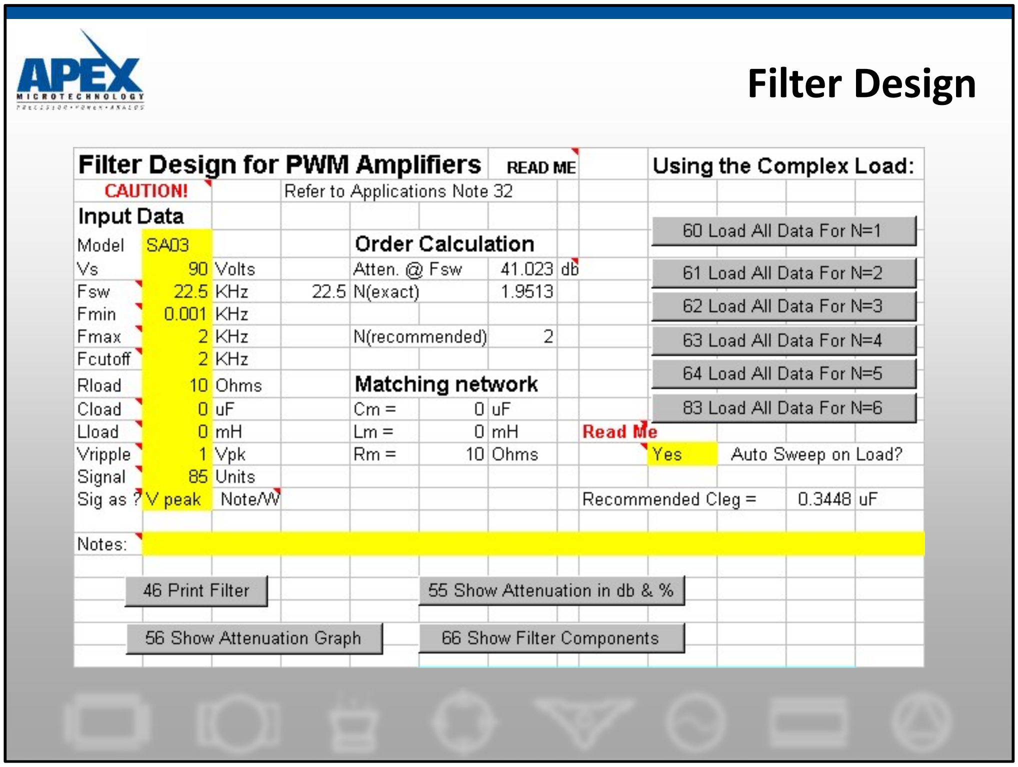
Ref. AN32

The Toolkit

- State average Spice models
  - Fast, any topology, AC sweeps
- Pulse-by-pulse macro models
  - Slow, no AC sweep, switching data
- The bench
  - Parasitics included
  - Light loads are a danger
  - Low supply voltage is OK, but…

PWM Spice models require Berkeley3 based or PSpice4 based platforms. Linear models usually run on older platforms also. State average PWM models run much faster than pulse-by-pulse models, can run an AC sweep, but provide no switching data.

With frequency components well into the RF range and power into the KW range, capacitive, inductive and resistive parasitics all mandate bench confirmation of a design. If years of linear power design taught you to start with light loads and a low supply voltage, beware: Improperly terminated filters can generate voltages greater than the supply. Frequency response and stability change as supply voltage changes.



So maybe filter design is not at the top of your list of most cherished jobs. Application Notes 32, 39 and the Power Design spreadsheet can help. Enter data describing the amplifier circuit, the load and desired attenuation. Placing the cursor in cells with red triangles will display notes of explanation. The order Calculation section converts your maximum ripple spec into dB attenuation and by examining the switching and signal frequencies, it calculates the order, or number of poles needed. The matching networks calculated will cause reactive loads to appear resistive to the output of the filter. Finally, a capacitor value is recommended for the leg capacitors for a filter topology.

power_design.zip is a free download from www.apexmicrotech.com. When unzipped, Power Design.xls will be extracted, ready to be run with Excel97.

Ref. AN39

Ideal Components

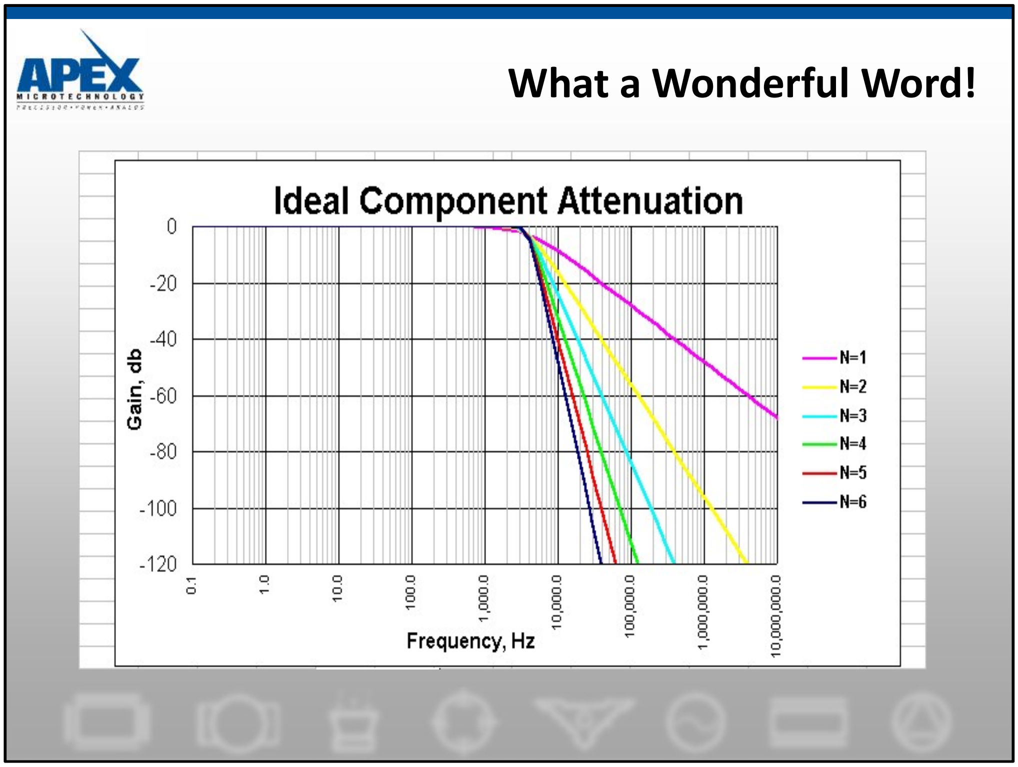
Component Calculations		Shading indicates values for Split Inductor topology									
	Dual Cap Filter			Single-ended Filter			Dual Cap Filter			Single-ended Filter	
N = 1	L =	0.3979	mH	0.7958	mH	N = 2	L =	0.5627	mH	1.1254	mH
	P-P Iripple =	2.5133	Amps out of the amplifier				C =	11.254	uF	5.6269	uF
	Avg. Iout for thermal calculations =			0.6283			P-P Iripple =	1.7772	Amps out of the amplifier		
							Avg. Iout for thermal calculations =			0.4443	
N = 3	L1 =	0.5968	mH	1.1937	mH						
	C =	21.22	uF	10.61	uF	N = 4	L1 =	0.609	mH	1.2181	mH
	L2 =	0.1989	mH	0.3979	mH		C1 =	25.102	uF	12.551	uF
	P-P Iripple =	1.6755	Amps out of the amplifier				L2 =	0.4307	mH	0.8613	mH
	Avg. Iout for thermal calculations =			0.4189			C2 =	6.0909	uF	3.0454	uF
							P-P Iripple =	1.6419	Amps out of the amplifier		
N = 5	L1 =	0.6148	mH	1.2296	mH		Avg. Iout for thermal calculations =			0.4105	
	C1 =	26.967	uF	13.484	uF						
	L2 =	0.5499	mH	1.0998	mH	N = 6	L1 =	0.6179	mH	1.2358	mH
	C2 =	14.235	uF	7.1174	uF		C1 =	28	uF	14	uF
	L3 =	0.1229	mH	0.2459	mH		L2 =	0.6179	mH	1.2358	mH
	P-P Iripple =	1.6266	Amps out of the amplifier				C2 =	19.124	uF	9.562	uF
	Avg. Iout for thermal calculations =			0.4067			L3 =	0.3016	mH	0.6031	mH
							C3 =	4.1189	uF	2.0595	uF
	56 Show Attenuation Graph			38 Data Input			P-P Iripple =	1.6184	Amps out of the amplifier		
							Avg. Iout for thermal calculations =			0.4046	

Application Note 32 will provide filter coefficient tables and formulas if you insist on calculating component values the hard way.

Values for dual-capacitor and single-ended filters are found under the appropriate columns, for orders up to six. Six is generally higher than is practical because of cost and diminishing returns due to component parasitics and stray coupling. To build a split-inductor filter, use values in the shaded areas from both columns.

P-P ripple calculations refer to current in L1 at the switching frequency when a 50% duty cycle is present. *The Avg. Iout for thermal calculations*=, is the average current through one PWM switch and can be used for determining junction temperature.

Ref. AN32,AN39

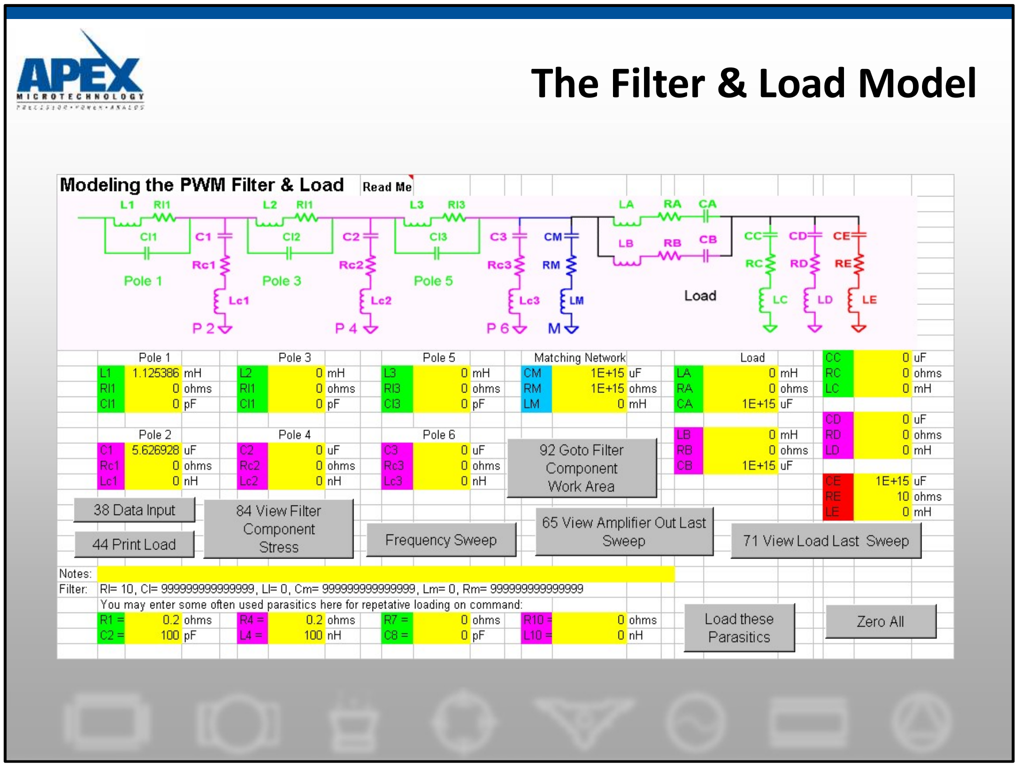


“Ideal” is a great word. In this case it means most of the work still lies ahead in finding components which work acceptably in the MHz range and whose losses won’t kill you at high current levels.

For capacitors, this often means parallel bipolar devices to obtain high value and high frequency performance. You will probably want ceramic for the smallest values and plastic for the higher values. For the largest capacitance values tantalum, or electrolytic types, can often be used in the dual-capacitor topology with some loss of high frequency attenuation.

Finding suitable inductors is also challenging. Air core inductors get away from the magnetic saturation problem and they have less tendency to become dummy loads at high frequency. The down side will be more turns of wire and more copper losses. When adding a magnetic core make sure the material can handle the high frequency components of the square wave at the switching frequency and can accommodate the flux density of the peak currents to be delivered to the load. Ferrite and powdered iron cores hold the most promise; avoid laminated steel cores.

Ref. AN32,AN39

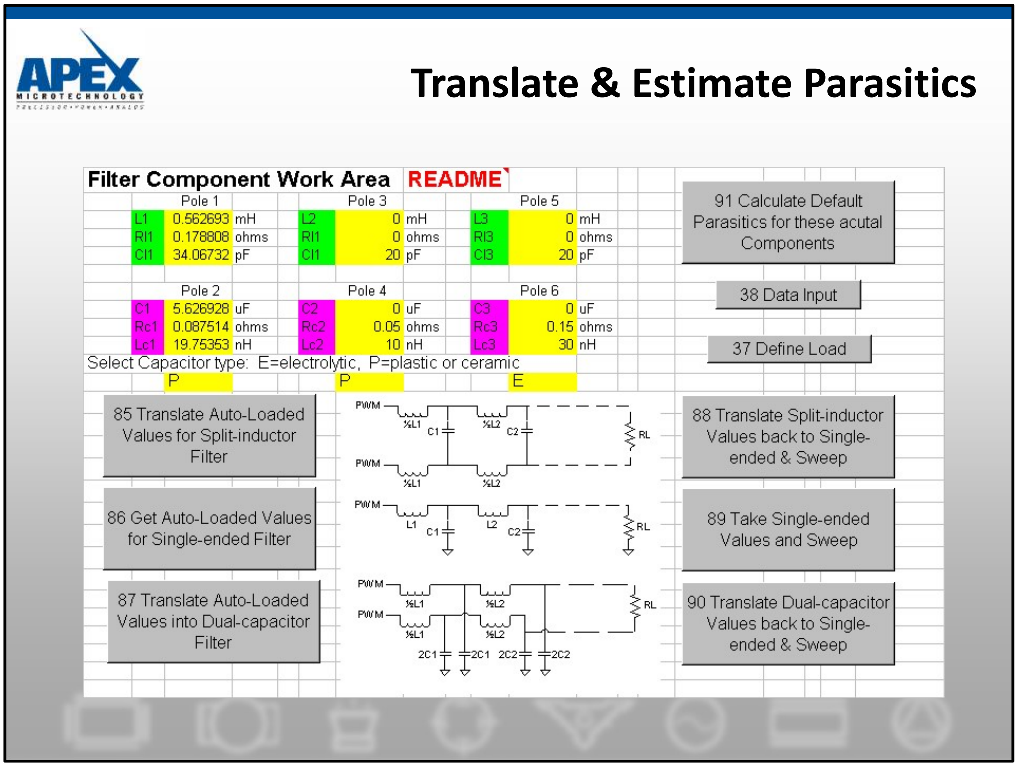


Pressing one of the "Load All Data" buttons on the PWM Filter sheet transfers your application to the PWM Power sheet. Ideal component values are loaded automatically for all six pole elements, the matching network and on the far right, the load we specified earlier. Extra components in the load modeling area provide more flexibility. As the math (and execution time) would be a significantly larger burden for any other topology, Power Design only analyzes single-ended filters. Note that the horizontal load model components are "zeroed" with no resistance, no inductance, but an extremely large capacitance. Unused components in the vertical orientation require zero capacitance or extremely large values of resistance or inductance.

The Frequency Sweep button will calculate critical voltages, currents and powers over the frequency range we specified. 100 frequency points will be examined. If this takes less than 10 seconds, you should be proud of your computer. If it takes more than a minute ………………

The Goto Filter Component Work Area button will be used to translate component values between the three topologies and for first pass design work, to estimate parasitic values.

Ref. AN32,AN39



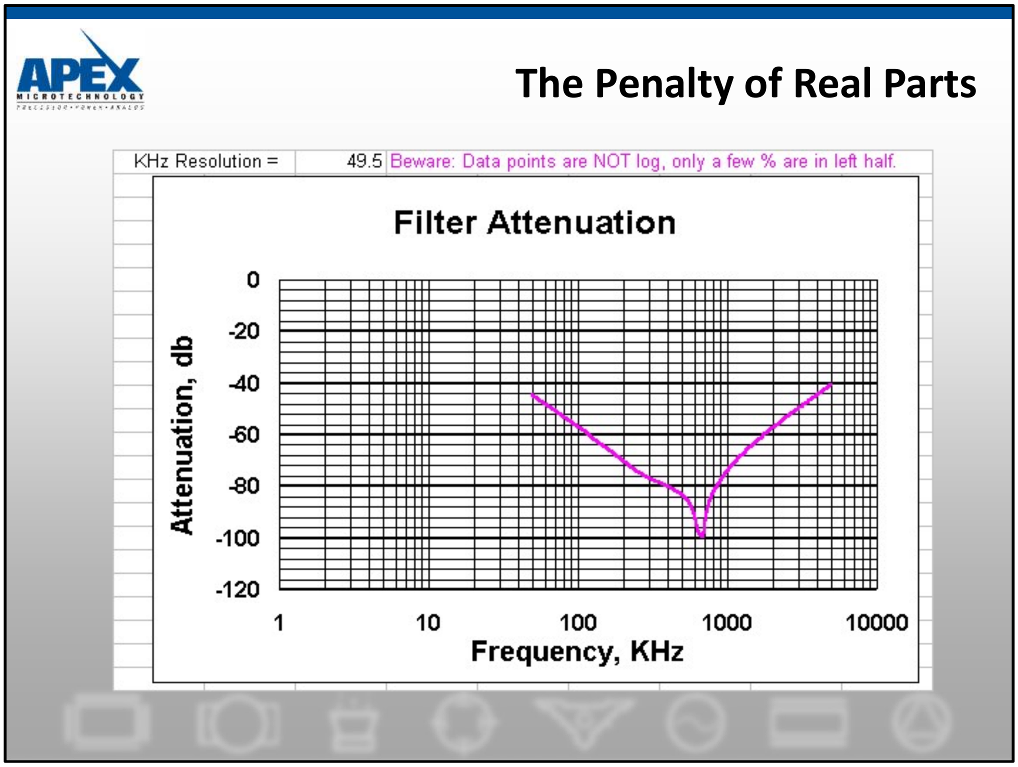
Buttons 85-87 will get or translate the Auto-loaded single-ended component values to values for the topology of your choice.

While there is absolutely no substitute for finding real parasitic values for filter components, button 91 provides a default parasitic calculator for first pass design efforts. Notice the cells where capacitor type can be selected individually for all three capacitors. Parasitics vary WILDLY from part to part. The default calculator is ONLY intended to get somewhere in the ballpark. These defaults are reasonable for parts suitable for switching applications. Your real parts could be better, but could easily be much worse. Consult manufacturer's data sheets or measure the parts to get accurate data for subsequent analysis. Values of purchased components and their real parasitics should be entered directly into the yellow cells and then be translated with button 88, 89, or 90.

During the translation back to single-ended values, if dual inductors are being used, the inductance and resistance will be doubled ,and the capacitance will be divided by two. If dual capacitors are being used, capacitance will be divided by 2, plus the resistance and inductance will be doubled.

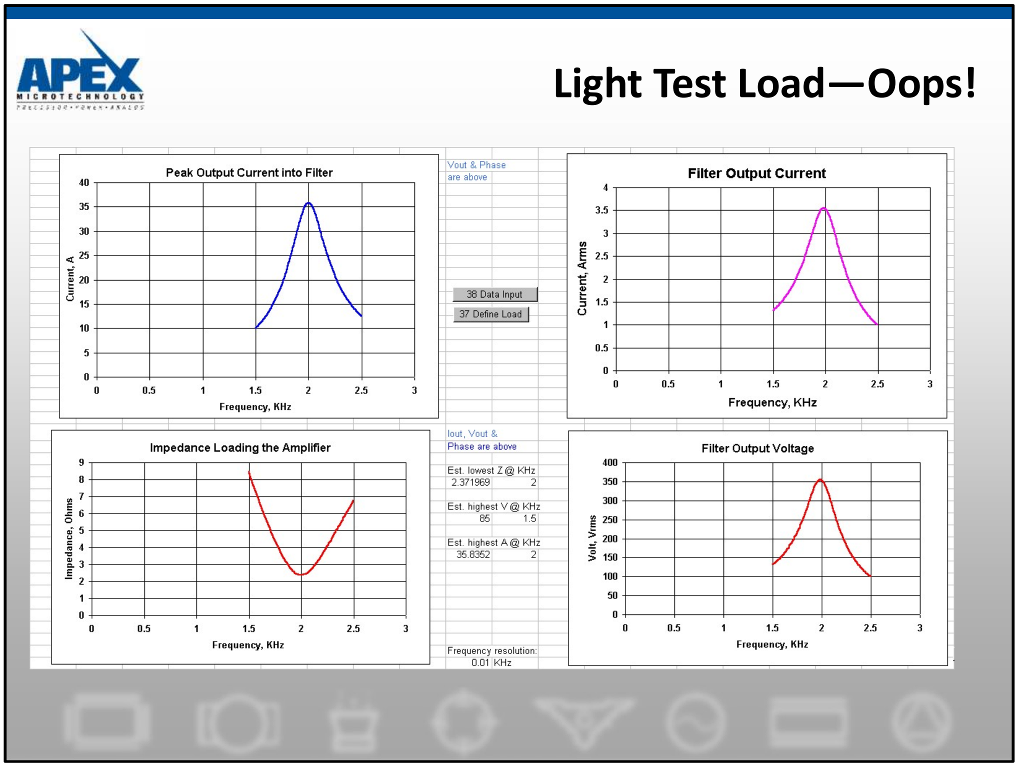
Frequency sweep will run automatically upon translation, and requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then do the sweep.

Ref. AN32,AN39



Attenuation is about as expected up to 200kHz, but then the parasitics come into play. We learned earlier that the extremely fast transition times of the PWM amplifiers means high frequency content is powerful well into the megahertz range. This graph is telling us spike content at the filter output is far from ideal. Is this OK? Or should we spend more on better filter components?

Ref. AN32,AN39



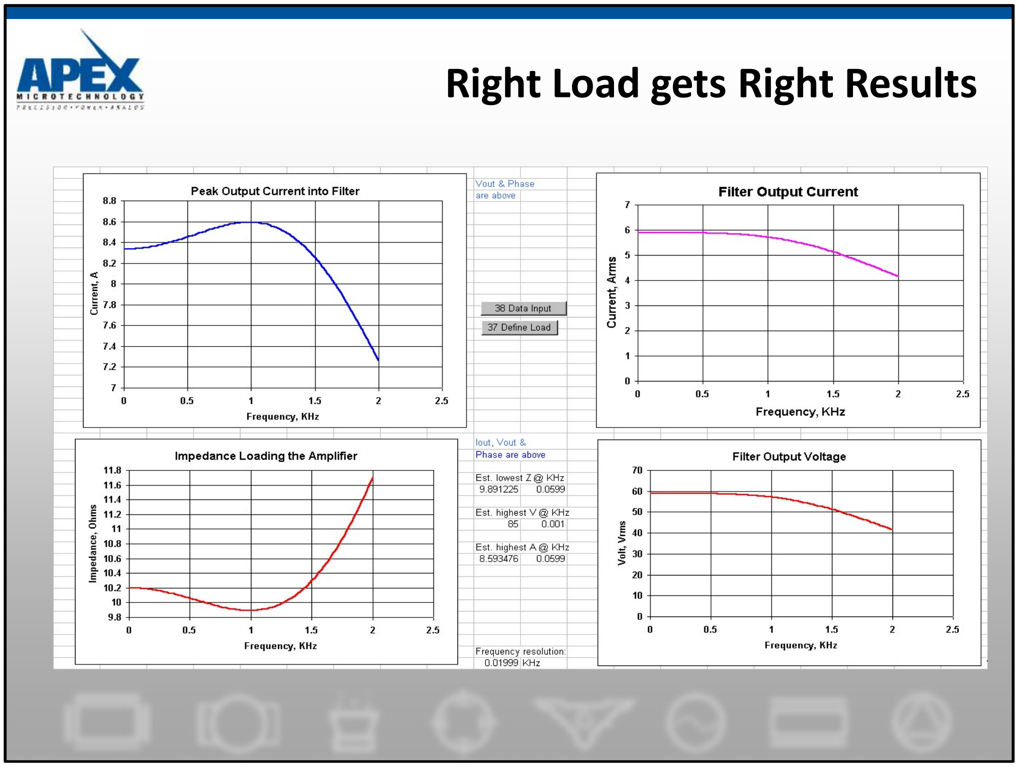
So, you're an old hand with linear power circuits; you fire up the prototype with a light load to make sure everything is working before connecting the real load.

While this procedure is commendable for linear drives and may work fine for a PWM drive, watch out for tuned circuits in the filter/match network/load. Replacing the designed 10 ohm load with 100 ohms produces the graphs above. At 2KHz impedance drops to ~2.5 ohms, peak current tops 35A, load voltage is ~355V and load current is 3.5A. 1200W delivered to the light 100 ohm load!

Be careful- -deadly voltages easily generated.

The second order filter driven at the designed cutoff frequency, with no load, is a series resonant circuit which presents a theoretical zero impedance to the amplifier and develops a theoretical infinite voltage at its center.

Ref. AN39

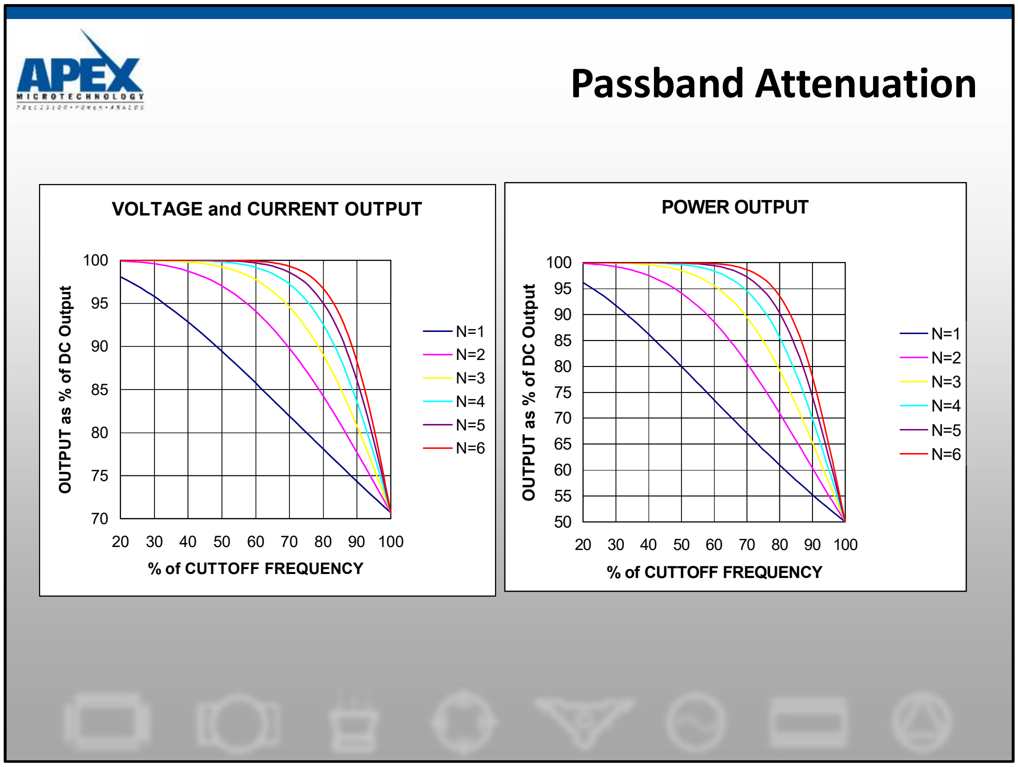


With proper termination of the filter we get a little mid-band peaking amplifier output current but the catastrophic potential of bad filter termination has gone away.

This filter design technique assumes amplifier output impedance is low compared to the load impedance and that the combined impedance of the load plus matching network is constant over frequency. The demand for circuit efficiency will insure the impedance relationship requirement is met. Beware that changing load element values, without corresponding matching network value changes, will alter the filter response curve. With some loads, such as solenoids or valves that tend to change inductance with position, the textbook response curve is nearly impossible to achieve. In these cases, try designing for the highest impedance, and then check performance driving the lower impedance.

While this operation is proper, is it what you wanted? The cutoff frequency of the filter is where the load voltage is down 3db. Does -3db equal .707 or .5? Both, .707 is the voltage or current ratio and .5 is the power ratio. Many times the half power at maximum frequency is not acceptable.

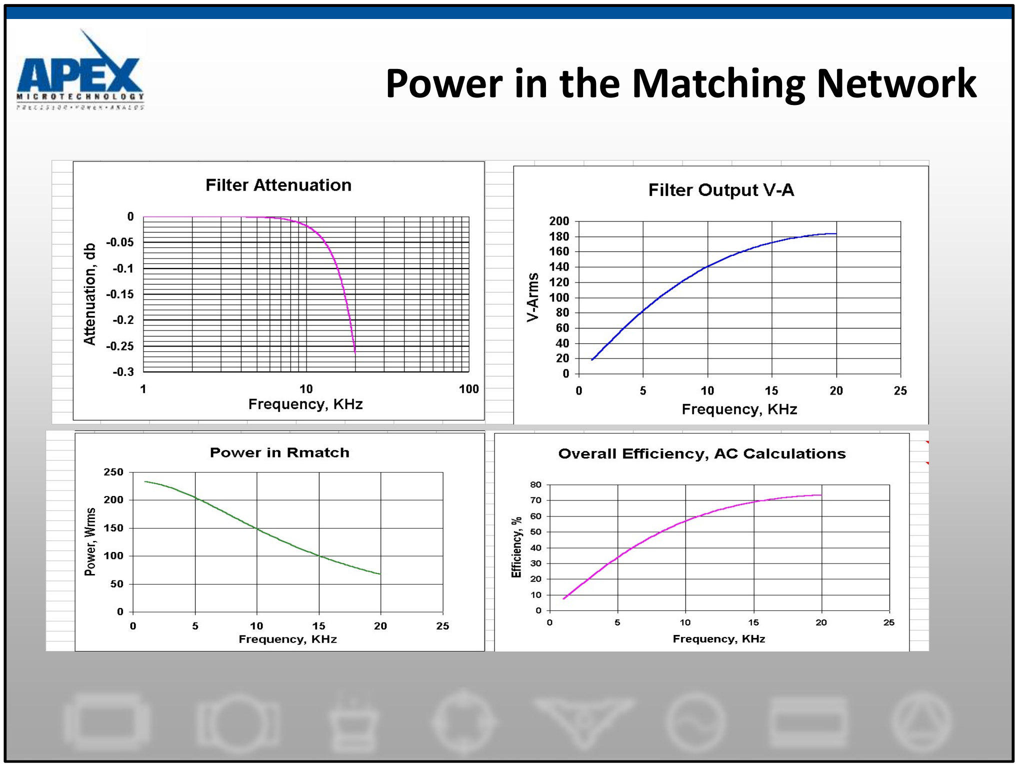
Ref. AN32,AN39



Designing the cutoff frequency at twice the actual maximum signal frequency is a very common technique to obtain a flatter response in the portion of the pass band actually used. You can see that in cases where amplitude flatness is critical, higher order filters and a wider ratio between actual signal frequency and Fc both help.

Yes, you could double again to achieve an even flatter pass band. No, there is no free lunch. Every time you move cutoff frequency up, you allow more switching frequency power in the load. Yes, you can add more poles to the filter. The question becomes one of cost in terms of money, extra loss in the filter, size and weight.

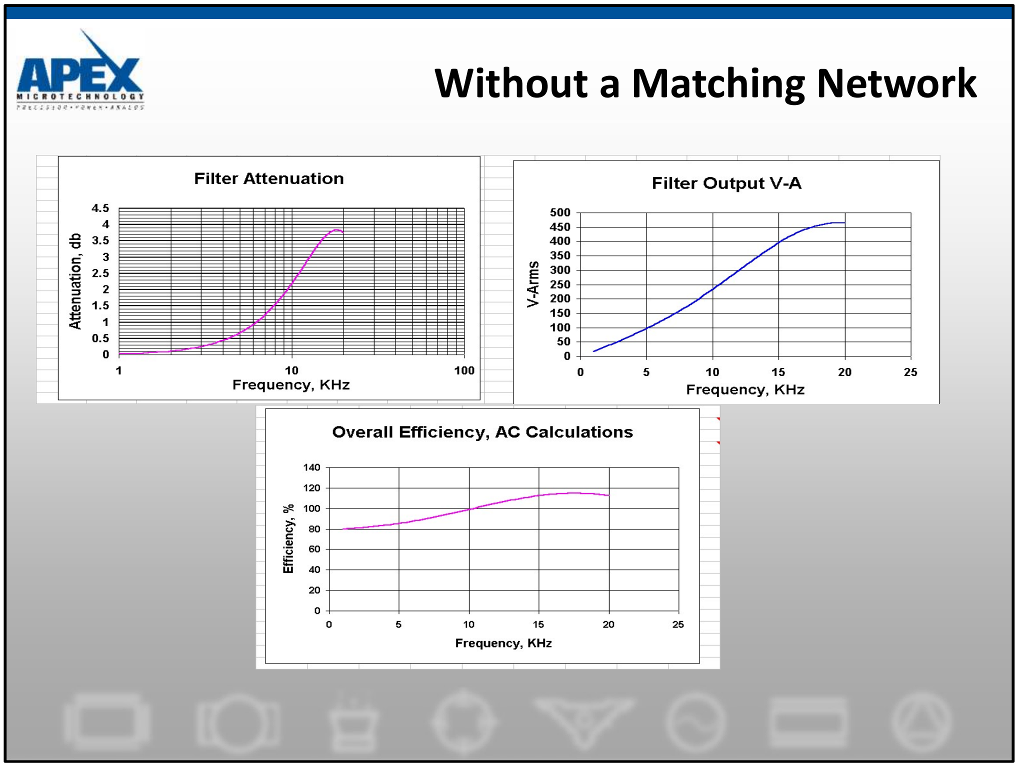
Ref. AN32



While the conjugate matching network performs almost like magic in terms of forcing the attenuation graph to near text book shape, there is a cost involved. This cost is slight when the load is mostly resistive but power dissipated in this network approaches power delivered to the load as the load approaches pure reactance.

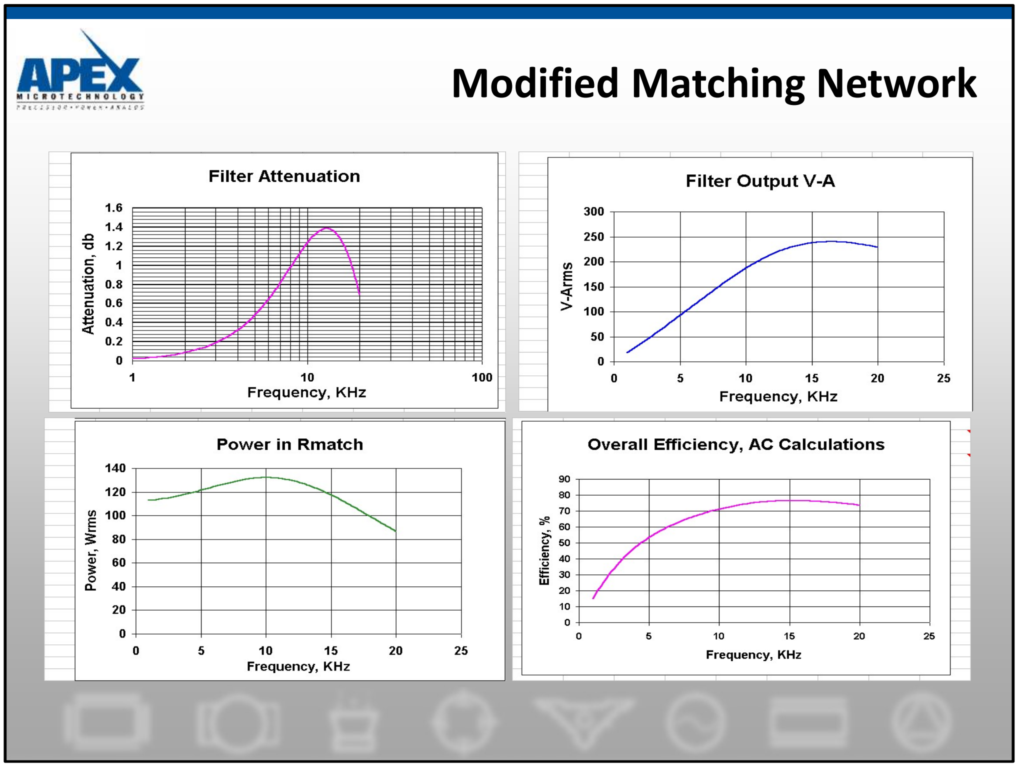
These graphs are for an application driving a 1uF piezo stack with 12 ohms series resistance, to 75V peak from 1KHz to 20KHz. The filter cutoff frequency was designed for 40kHz providing quite flat response. The V-A output falls at low frequency because the load impedance is increasing. To keep filter termination impedance flat, the matching network impedance moves in the opposite direction giving rise to large power levels in the matching network resistor. As this power is not delivered to the load, efficiency is far from the desired level.

Ref. AN32,AN39



With no matching network we cannot lose any power there, but this leaves the filter with an improper termination. The result is a resonant circuit causing almost 4db peaking. In terms of V-A in the load near the upper end of the band, power goes from ~180 to over 450V-A. The efficiency graph looks like a patent should be applied for. The reason for this is recirculating currents in our newly formed resonant circuit.

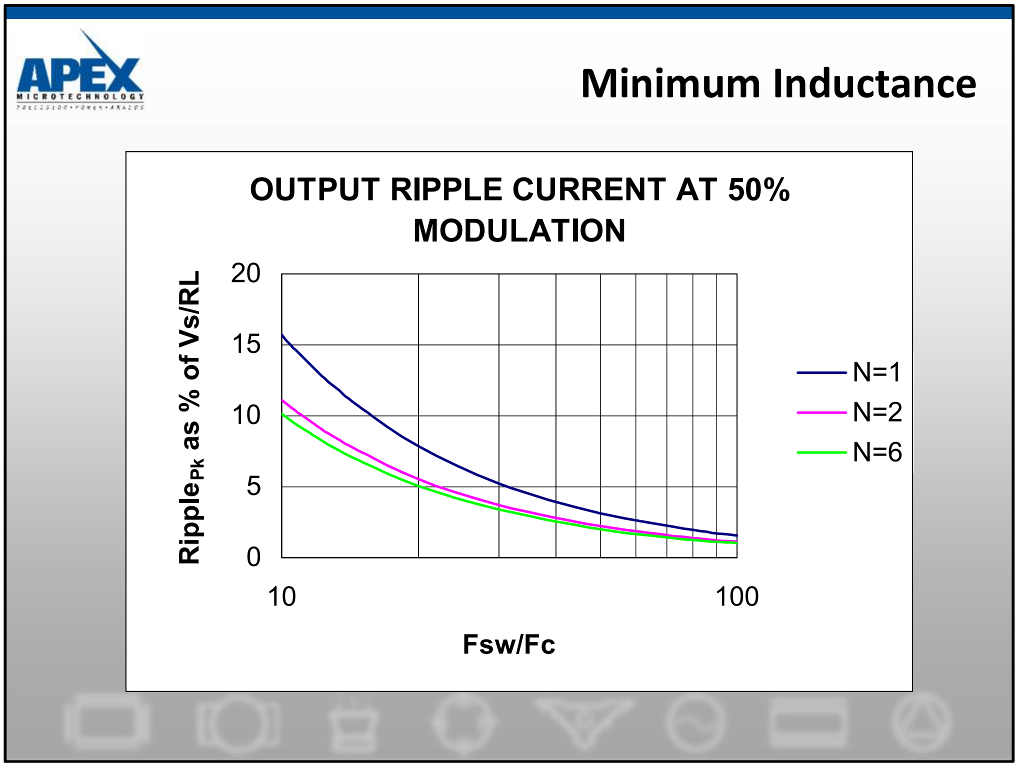
Ref. AN32,AN39



Here lies part of the beauty of the Power Design spreadsheet; it took more time to prepare this slide than it did to discover that doubling the resistor value in the matching network may provide a workable compromise.

Peaking at the load is down substantially from not using any network and wasted power is down substantially from using the ideal network.

Ref. AN32,AN39

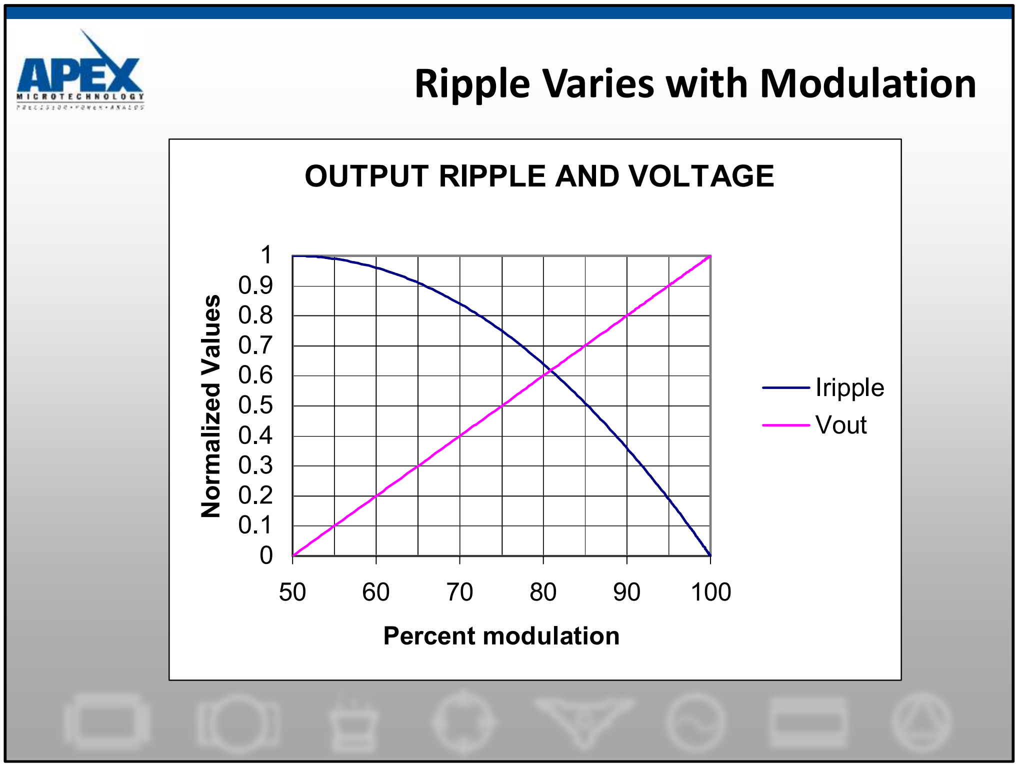


Application Note 30 admonishes us to make sure the PWM amplifier is driving enough inductance to keep ripple current at the switching frequency to a reasonable level. When designing filters according to Application Note 32, this concern becomes part of the filter design.

A full bridge PWM amplifier driving a first order (single pole) filter with Fc set at 1/10, the switching frequency will be required to deliver approximately 15% of the peak output current as peak ripple current. The ripple is at the switching frequency; measured when the modulation level is 50%; and assumes peak output current equals Vs/Rl. Changing to a second or higher order filter will drop this to almost 10%. A second and even more effective way to reduce this ripple current is to widen the ratio between signal and switching frequencies. As switching frequencies of Apex PWM amplifiers range from 22.5kHz to 500kHz, this technique has obvious limits.

This ripple current flows through the first inductor of the filter, meaning high frequency core loss is of concern. With first order filters driving resistive loads, it also flows through the load. With higher order filters, most of the ripple current flows in the first filter capacitor, affecting the ripple capacity rating of these components.

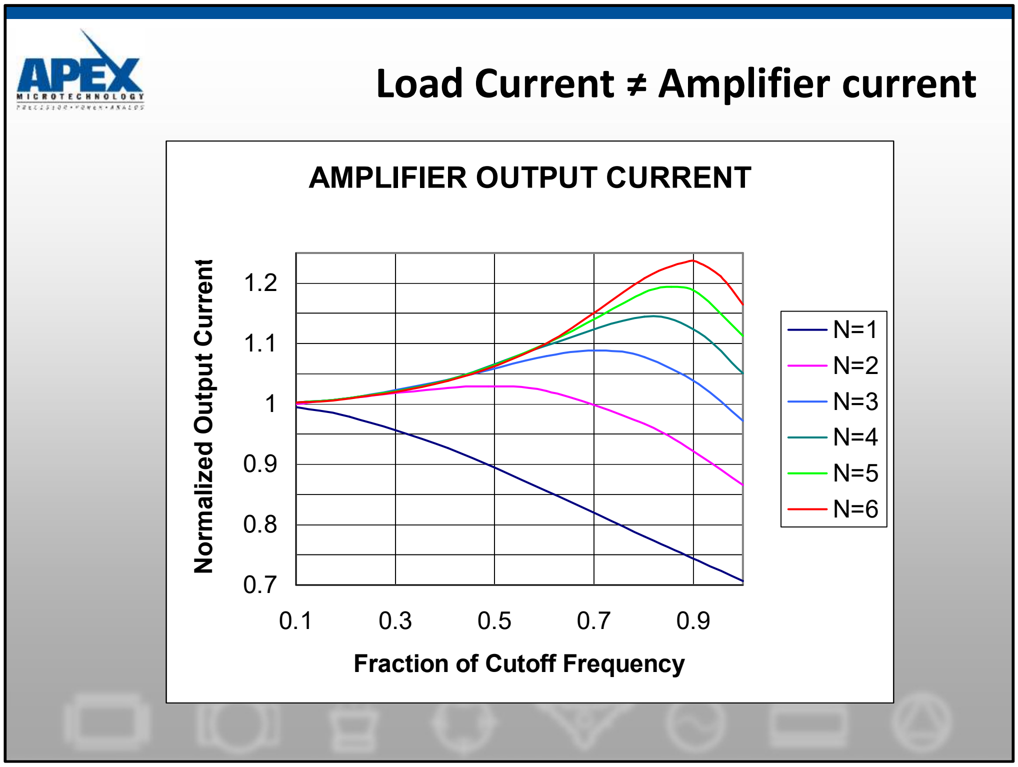
Ref. AN32



In applications where full modulation is expected (output current is expected to approach Vs/Rl), the workload imposed on the amplifier by delivering the ripple current is of minor concern. While 15% (or less as) of maximum output may seem more than minor, this ripple current decreases as modulation percentage moves away from 50% (a graph of zero to 50% would produce a mirror image curve). In other words, heatsink size is not increased 15% because maximum DC output and maximum ripple output never occur at the same time. The heatsink will be sized to handle the much larger output current. The ripple current curve is also valid for half bridge circuits, but the Vout curve would need to be re-scaled from 0.5 at 50% modulation to 1 at 100%.

For applications spending a major portion of the time near the 50% modulation level, the ripple current will be quite noticeable in terms of lowered efficiency (power supply loading and heatsink temperature). These circuits include full bridges spending most of their time delivering small signals compared to peak output capability; full bridges whose peak output voltage is considerably less than supply voltage; and half bridges spending most of their time delivering half the supply voltage.

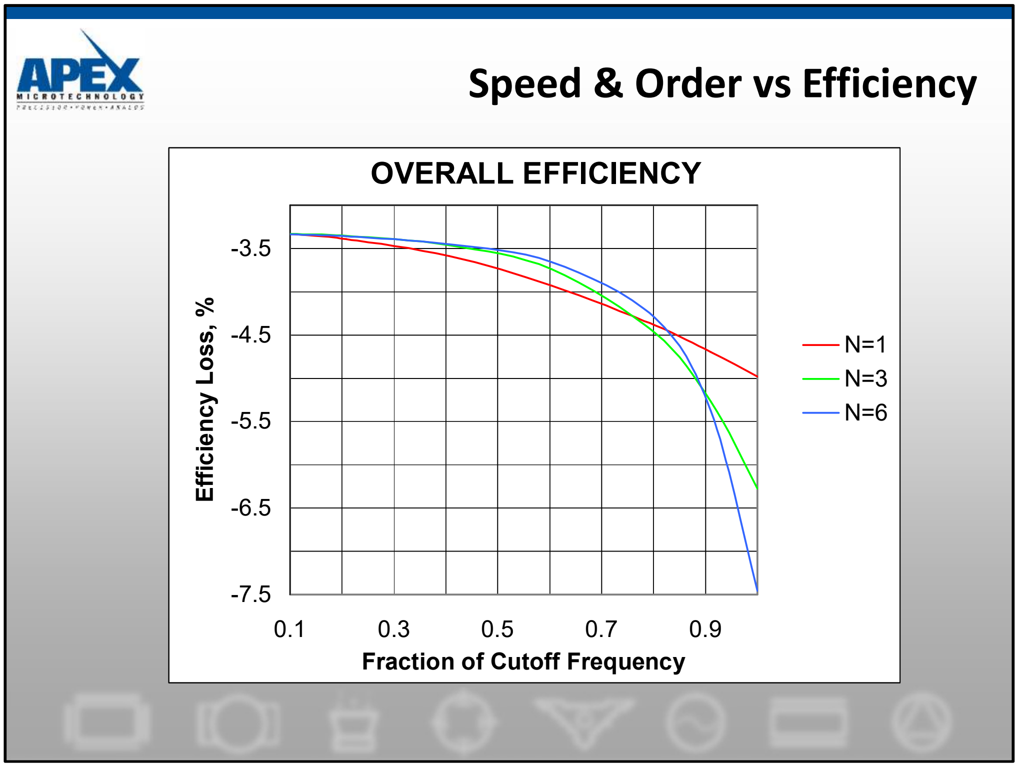
Ref. AN32



When using second and higher order filters, impedance presented to the PWM amplifier will dip below the load impedance as signal frequency approaches Fc. The graph above shows this in reciprocal form. Putting some numbers to go with the worst point: N=6, Fc=1kHz, Fsignal=900Hz, Iload=10A, amplifier output=12.3A. This "extra" current flows in the output devices of the PWM amplifier increasing internal power, increasing ON resistance, increasing junction temperatures and reducing efficiency. This effect should be considered also with regard to amplifier and power supply current ratings and design of current limit circuits. We will see what looks almost like a duplicate of this graph when discussing filter component stress levels.

Again, this graph shows the advantages of lower order filters and wider ratios between actual signal frequency and Fc.

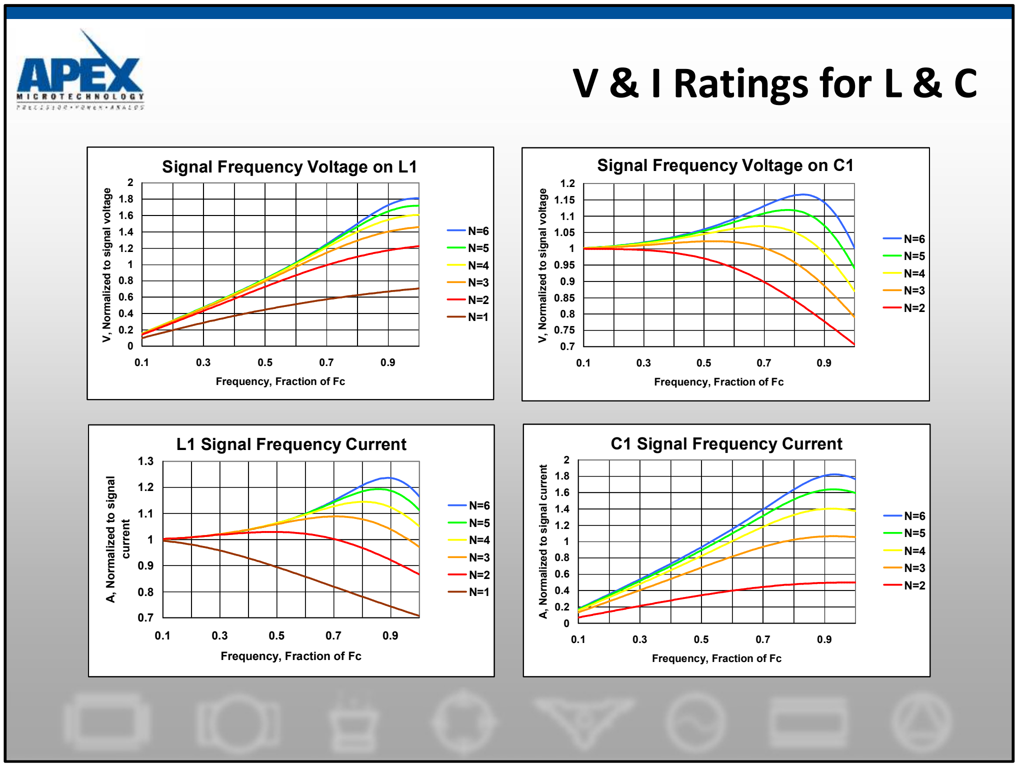
Ref. AN32,AN39



This is efficiency data for a perfect component filter (no parasitics) designed for an SA03 running maximum output voltage into a 10Ω load while mounted on a 0.1°C/W heatsink. At 10% of Fc, about 3.3% is lost in the amplifier and the filter is having very little affect on efficiency. As signal frequency increases, three effects combine to bring high frequency efficiency down further. First, quiescent power remains constant even though the output signal is rolled off. Secondly, the peaking output current demanded by second and higher order filters increases internal PWM losses. The last item is the positive non-linear temperature coefficient of the ON resistance of the PWM, which increased about 1% in this example.

The point here is that filter choices can double efficiency loss even before allowing for filter component loss. Importance of this data varies with the spectral content of the signal being amplified. Consider an audio application versus a fixed 400Hz inverter application.

Ref. AN32



Multi-pole filters are a combination of one or more series resonant circuits and they do develop currents and voltages above the input and output levels as the signal frequency approaches the cutoff frequency. The highest stress levels will be born by L1 and C1. Higher order filters produce higher amplification levels. The last two components of the filter do not see stress levels above the signal level. In these graphs, voltages and currents are normalized to the DC or very low frequency output signal amplitude and are based on ideal components.

Data on current can be used directly for any filter topology for both inductors and capacitors. If a split inductor topology is used, the inductor voltage data must be divided by two. Voltage data can be used directly for capacitors not connected to ground. Ground terminated capacitors have a DC bias equal to ½ the supply voltage which must be added to half the peak voltage calculated from the graphs. Do this calculation for BOTH the positive and negative peak output voltages. Note that if output voltage is nearly equal to supply voltage, and the filter order is three or more, the most negative going peak for C1 will be negative with respect to ground. The same is true for C2 with fifth and sixth order filters. This means even a ground-terminated capacitor can have BIPOLAR voltages applied. From a practical point of view, this situation implies the use of unipolar capacitors limits filter order to two.

As an example, consider filter options for an SA06 (which is no longer available, but the text was kept the same for example purposes) which is to deliver ±470V to a 332Ω resistive load at 1kHz. Current will be 1.414A peak or 1A RMS. Power will be 665W peak or 332Wrms. A supply of 480V will provide plenty of headroom for internal losses and maximum linear duty cycle limitations. The worst case for voltage and current extremes will be a sixth order filter.

L1 peak current = 1.414A * ~1.23 = 1.75A

L1 peak voltage = 470V * ~1.82 = 850V 425V each if dual

C1 RMS ripple current = 1A * ~1.82 = 1.82A

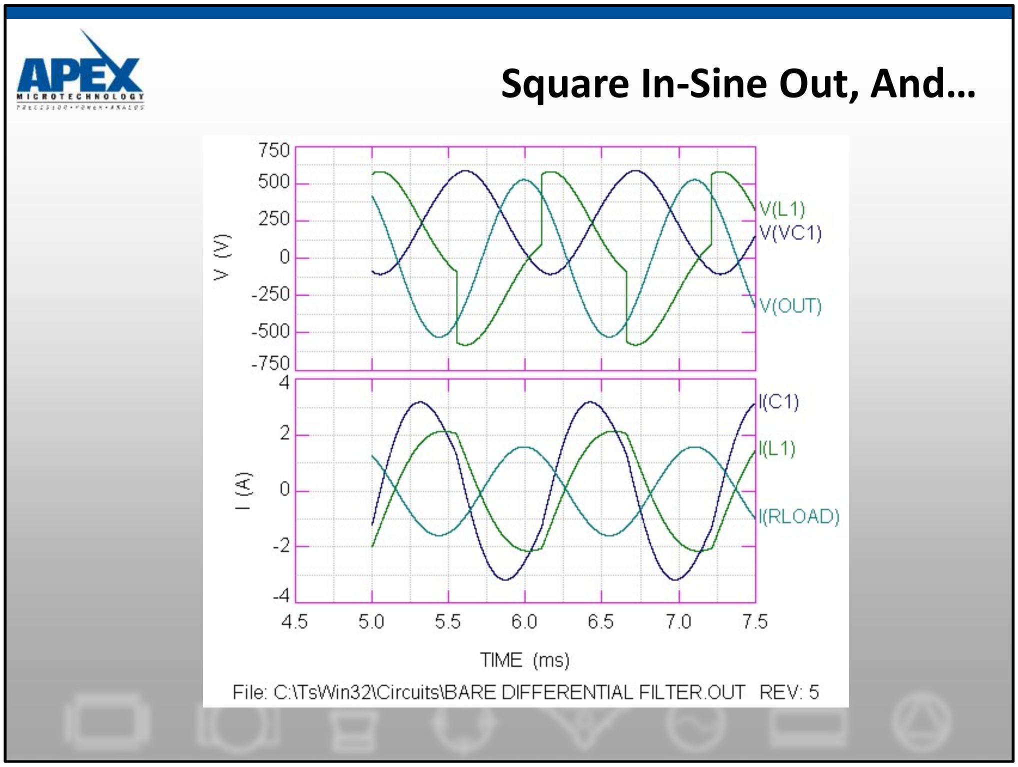
C1 peak voltage (differential) = 470V * ~1.17 = 548V

C1 + peak voltage (grounded) = 240V + 274V = 514V

C1 – peak voltage (grounded) = 240V – 274V = -34V Must be bipolar

These stress levels are normal, even though the output ratings of the circuit are only 470V peak and 1Arms and the filter is properly designed and terminated. Before we go to the next slide, note that the input signal for this circuit is a sine wave.

Ref. AN32



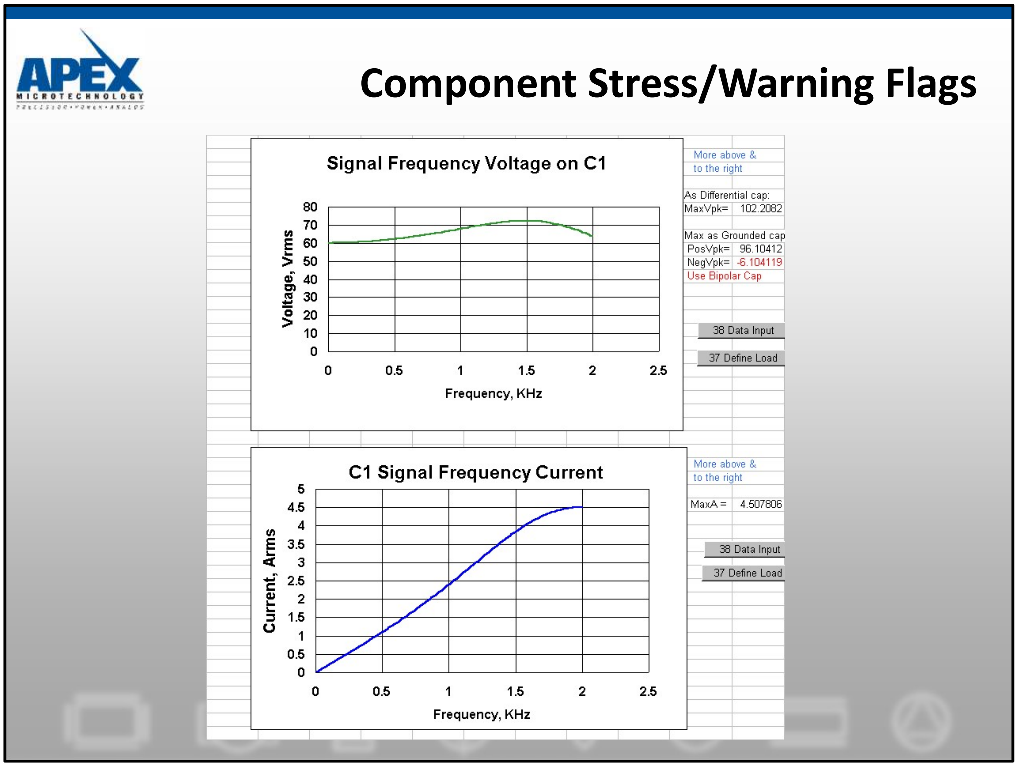
This is a Spice simulation of the previous example showing L1 and C1 stresses when the input signal is a 900Hz, 470V square wave instead of a sine. The modeled filter topology was a dual capacitor design.

L1 voltage = ±582V and is for ½ the total inductance (a single-ended design would place ±1164V across the inductor). L1 current peaks at ±2.14A. C1 current peaks at ±3.18A. C1 is grounded and has voltage peaks of 587V and – 107V. Watch out with that electrolytic capacitor! The output is a very good looking sine wave instead of a square, and peak output amplitudes have risen from 470V to 527V, from 1.414A to 1.59A and from 665W to 838W.

Points to consider:

1. Other than this slide, all input signals have been sine waves.
2. Input waveforms other than sine, can produce stress levels even higher than Power Design predicts.
3. As signals approach Fc, filters REALLY like to output sine waves.
4. If you really do need constant frequency sine waves with peak amplitude higher than the supply voltage, this is a possible circuit.

Ref. AN32

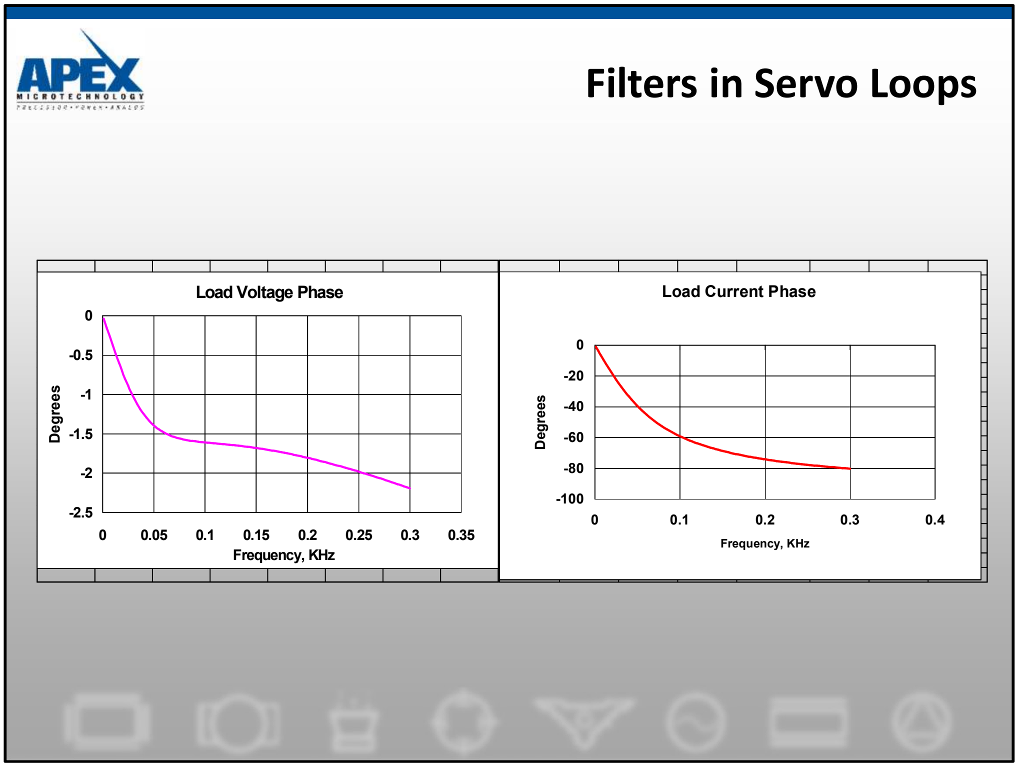


Power Design calculates voltage and current stress levels on L1 and L2, plus C1 and C2 for all designs. Resonance of these filters can produce voltages and currents larger than the load levels. Button 84 will place the first graph on the screen, then scroll up and to the right to view other graphs. The currents shown here can be used directly for all filter topologies. If L1 is actually two inductors, half the voltage shown will be across each individual inductor.

This circuit example only has a 90V supply; the drive signal is only 85Vpk; the load resistance has risen to 15Ω even though the filter design was for a 10Ω load. We might initially expect the 85Vpk signal and the 15Ω to limit inductor current to about 5.7A, but L1 has current peaks of 10.1A and voltage peaks of 108V. These peak values are pointed out on the right.

For capacitors, peak voltage is calculated for both differential and grounded capacitors. If a ground capacitor would experience a negative voltage, The red flag pops up.

Ref. AN32

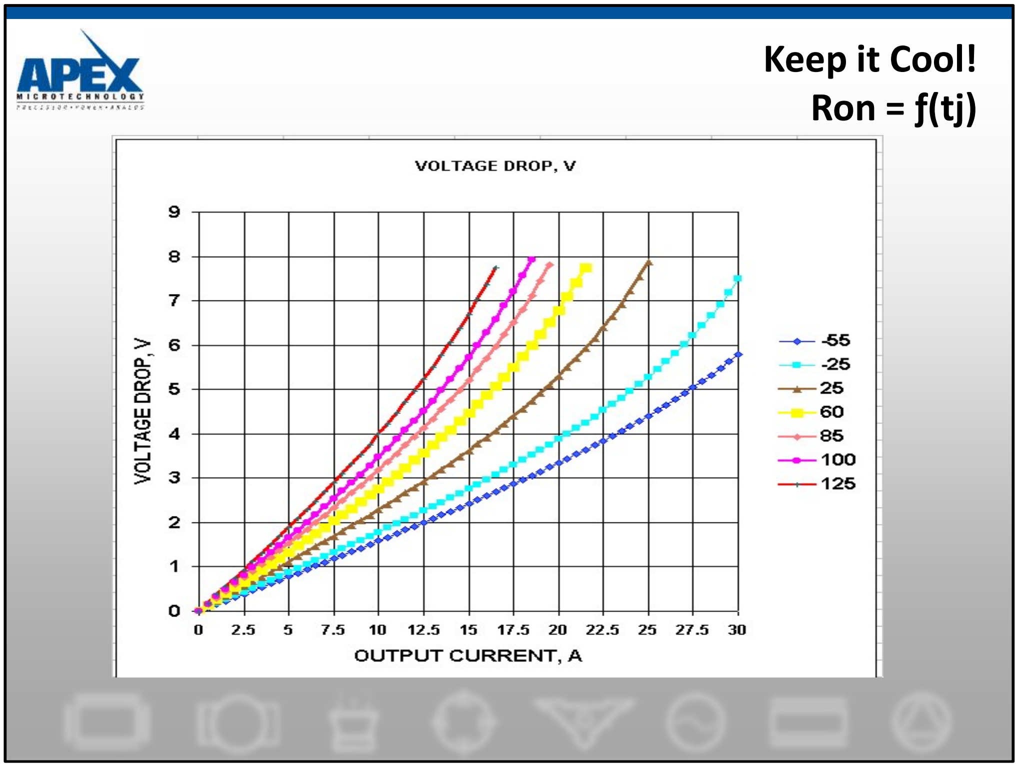


These filters are notorious for introducing large phase shifts. This is usually not a problem when feedback is taken directly at the output of the PWM amplifier. In applications such a servo loops, feedback is taken after the filter and any phase shift introduced here affects system phase margin. Power Design calculates both voltage and current phase in the load.

Voltage phase shift through a properly designed and terminated filter will be 45° per pole at Fc. This phase shift is reduced as the ratio between Fmax and Fcutoff frequencies widens.

These graphs are from a 5mH, 2Ω magnetic bearing application featuring current output, third order filter with a cutoff frequency of 3kHz, and a modified matching network.

Ref. AN32



The “on” resistance of a power MOSFET increases about two times as junction temperature rises from +25°C to +150°C. This means a larger heatsink increases both output capability and efficiency. If there’s good news to this story it’s the nonlinearity of the curve: The first few degrees we lower temperatures buys the most. Here’s a way to approach the problem.

First order power dissipation in the PWM is a function of the output current and the voltage drop at that current. This is the PWM advantage over linear power delivery; supply voltage is not part of the equation. Start with the 60°C curve (interpolate if required). Find your current (PEAK if below 60Hz, otherwise RMS) and read the voltage drop. The product is power dissipation. The voltage drop divided by supply voltage approximates efficiency (quiescent current of both Vcc and Vs will reduce this a little). The heatsink rating is 60°C minus ambient temperature, divided by power.

Are these numbers all affordable? Remember that a bigger heatsink actually reduces the watts to be dissipated (unlike linear systems).

Ref. AN32,AN39

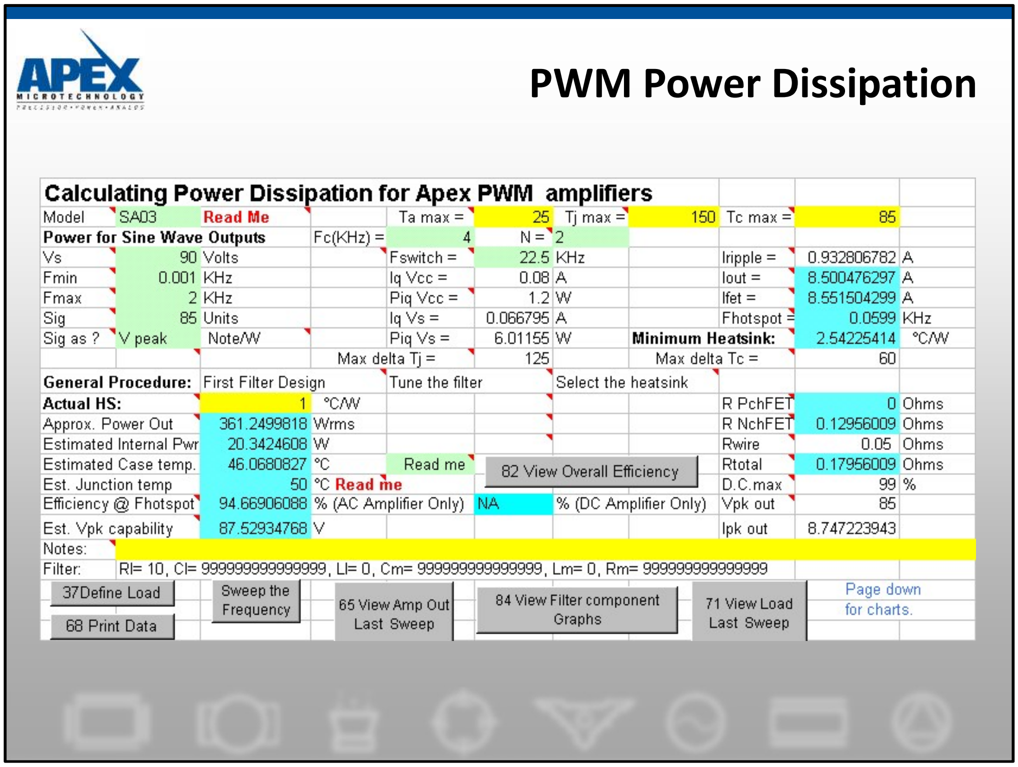
PWM Internal Power Dissipation

- P = I*I*R
  - I = switch current, R = switch on resistance
  - VS and VO are NOT in the equation!
- Both terms are moving targets
  - ΔR ≈ 2:1 from Tj 25 to 150°C
  - Reactive elements cause I to move vs. frequency
- Heatsink rating affects efficiency

First order approximation of internal power dissipation looks deceptively simple. The advantage of PWM power delivery is that supply and output voltages are NOT part of the equation. This means that the power supply can be substantially higher the output voltage without a significant penalty in efficiency.

The fact that both terms of the prime equation move around makes the calculation task more complex than with linear amplifiers. Again, this becomes a good job for a spreadsheet.

as with linear amplifiers, the heatsink must keep the semiconductors cool enough to provide a reliable circuit. In addition, larger heatsinks on PWM amplifiers actually increase efficiency.



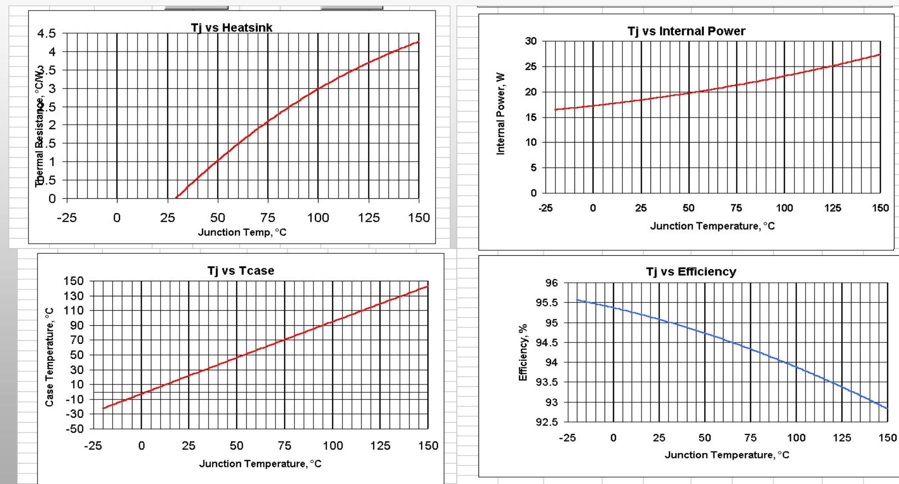
Did someone complain about lack of details on the previous page? Here they are, and the inputs were transferred from the PWM Filter sheet. If you change a green cell value, blue cell answers will not be valid until you run a frequency sweep.

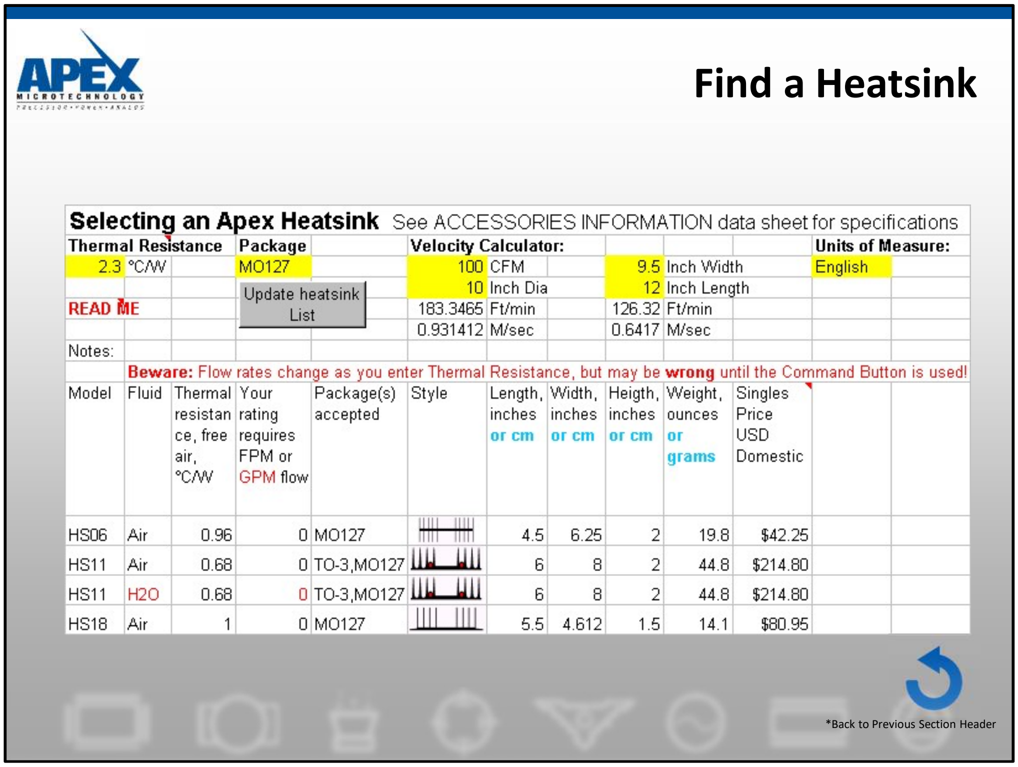
If you get errors when you do this at home, check the READ MEs. You need the Analysis Toolpak add-in. Now you can see in the upper half, quiescent powers calculated, plus output current, FET current, hotspot frequency and best of all, minimum heatsink.

A little lower, notice I have already input an acceptable heatsink value and operating points have been calculated. Please read the comments. The Power Output assumes a properly terminated, zero loss filter, and a power factor of 1 in the load. Use button 82 to see efficiency including filter losses. If you enter too small a heatsink, most of these answers will be forced to ridiculously large numbers and a red TOO HOT warning will appear.

Ref. AN39

Find a Heatsink Rating





Model	Fluid	Thermal resistance, free air, °C/W	Your rating requires FPM or GPM flow	Package(s) accepted	Style	Length, inches or cm	Width, inches or cm	Heigth, inches or cm	Weight, ounces or grams	Singles Price USD Domestic
HS06	Air	0.96	0	MO127		4.5	6.25	2	19.8	$42.25
HS11	Air	0.68	0	TO-3,MO127		6	8	2	44.8	$214.80
HS11	H2O	0.68	0	TO-3,MO127		6	8	2	44.8	$214.80
HS18	Air	1	0	MO127		5.5	4.612	1.5	14.1	$80.95

Believe me, heatsinking is NOT the easiest science in our universe.

Let's start with "the" heatsink rating. The HS03 is rated at 1.7°C/W in free air. True, when power dissipation is about 45W, but check the actual curve at 10W and you'll find a rating more like 2.3°C/W. On top of that, "free air" means no obstructions to air flow and the flat mounting surface must be in the vertical plane. Demands for higher performance in smaller packages can be at odds with optimum heatsinking. Poor installation choices can easily reduce effectiveness 50%.

Moving on to this selector software. Air velocity curves from the heatsink data sheet (when available) have been approximated with polynomial expressions. While these errors are minor compared to the previous paragraph, it would be good to allow 10% for velocity ratings over 150 feet per minute and 20% below that.

Adding a fan to your design enables you to use smaller heatsinks. Please remember: Most fans are rated in cubic delivery and this rating varies with working pressure. A 5 inch diameter fan delivering 100 CFM produces over 700 FPM right at the fan. If this air is flowing through a 19 x 24 inch rack, theoretical velocity is down to 32 FPM, will vary with location and goes lower as the rack is sealed tighter.

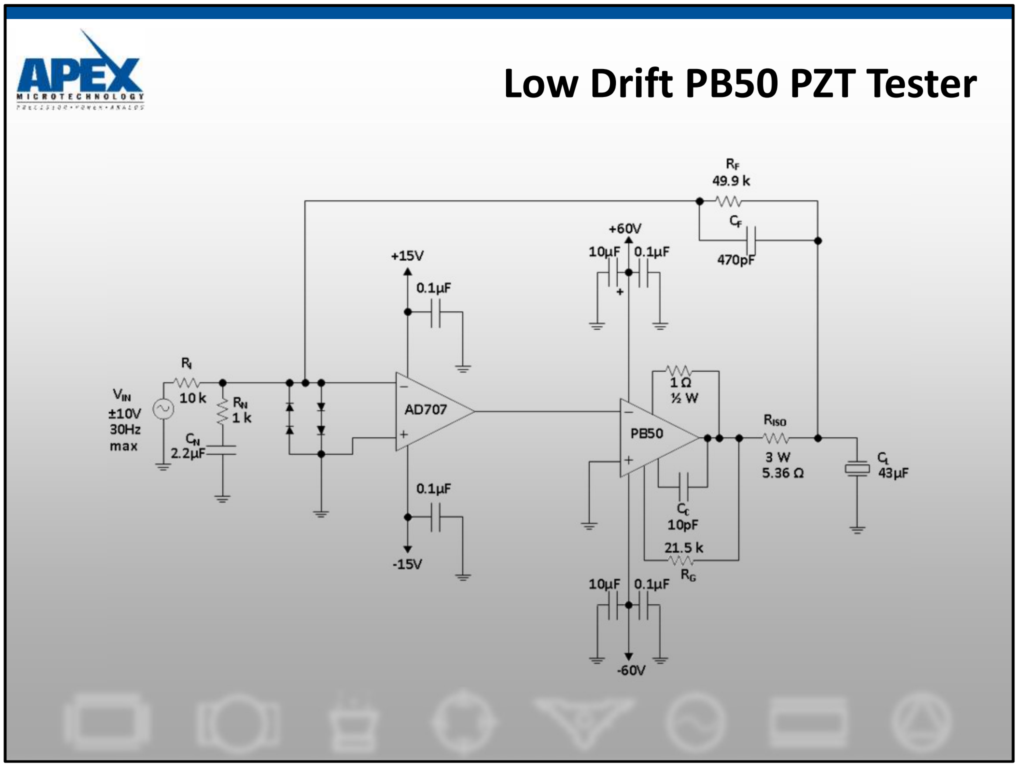
The bottom line: Without case temperature measurements, your design effort is NOT complete!
Ref. AN39

ATE - AUDIO

ATE Applications

- High Voltage PPS
- High Current PPS
- AC Power Supplies
- Pin Drivers
- Waveform Generators
- Active Loads

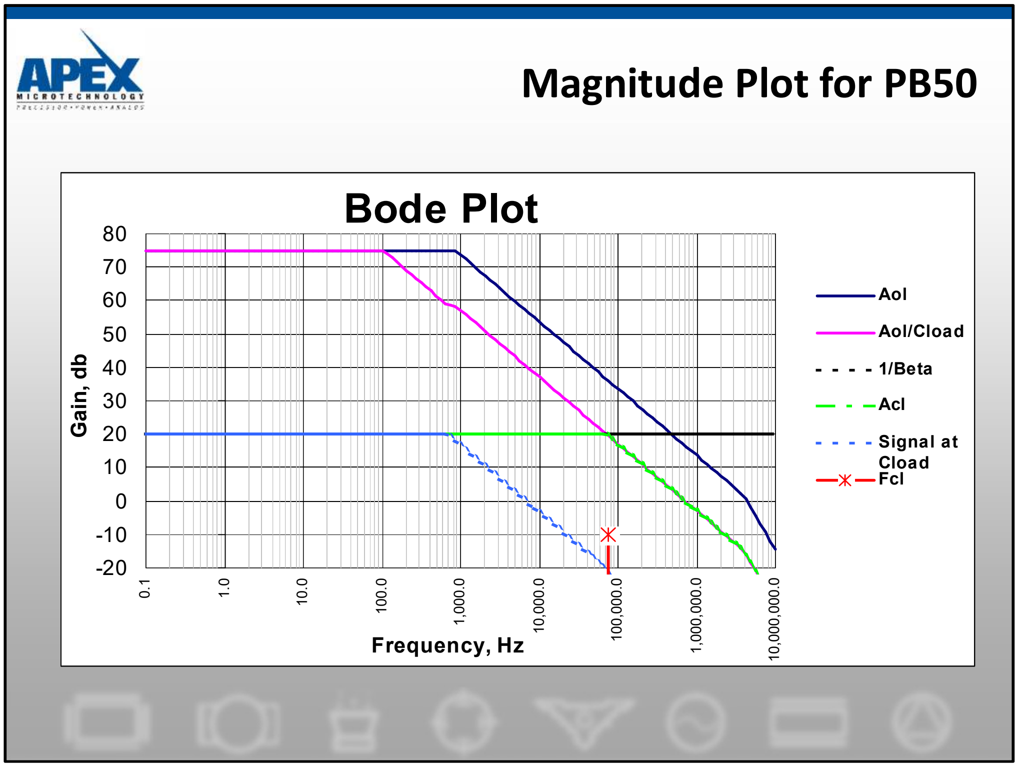
There are an extensive array of application for high power, high voltage, and/or high speed linear amplifiers in almost any type of automatic test equipment. Some of the most popular application include different types of programmable power supplies. There are also ample opportunities for them to be used for waveform generation for DUT excitation



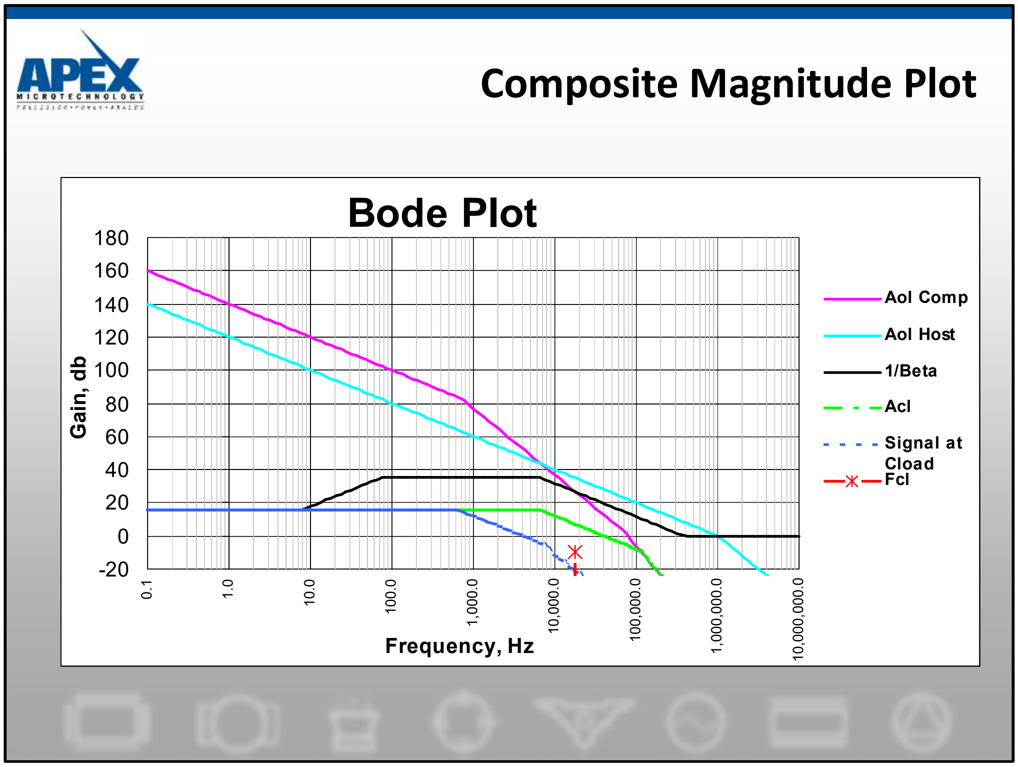
This Low Drift PB50 PZT Tester utilizes the flexibility of the PB58 power booster to provide low drift, high accuracy voltages to the PZT (Piezo Transducer) under test. The AD707 provides a composite amplifier input offset voltage of 90µV, and a drift of 1µV/°C. Higher accuracy can be obtained with a different host amplifier or a better grade of AD707.

The PB50 is a versatile building block for ATE design that provides a low cost option for providing high voltages to devices under test. With supply voltages from ±30V to ±100V, with a slew rate of 100V/µS, and output current drive capability of 2A, The PB50 can provide up to 100KHz power bandwidth for high voltage test equipment. The composite amplifier approach for using this power booster allows the user to program the accuracy of the overall amplifier through selection of the front end host amplifier.

This particular implementation of the PB50 will present some stability challenges since we are driving a capacitive load with a composite amplifier. The approach to stabilizing this circuit will be to stabilize the power booster with its capacitive load and then stabilize the total composite amplifier. We don't stand a chance of stabilizing the composite amplifier if the output power booster is not stable first.



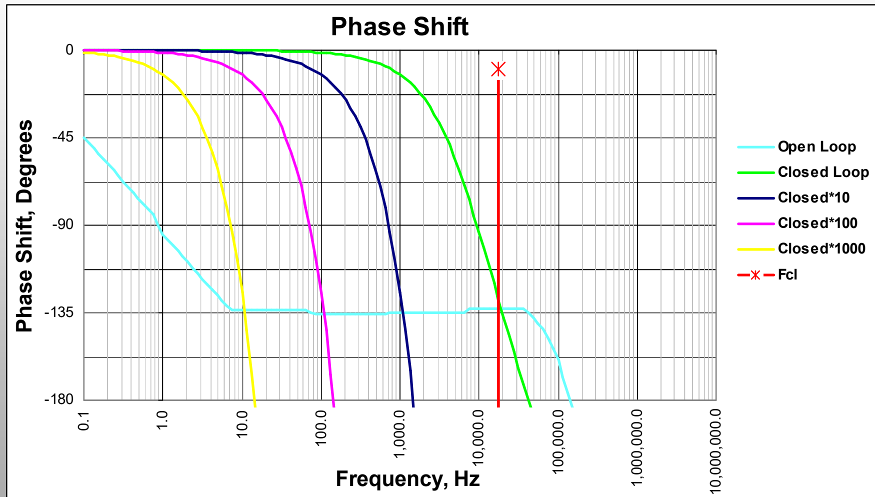
Without the isolation resistor, the modified Aol curve would have changed to -40db per decade just under 1KHz giving an unacceptable intersection rate and about 2.5° phase margin rather than 90°.

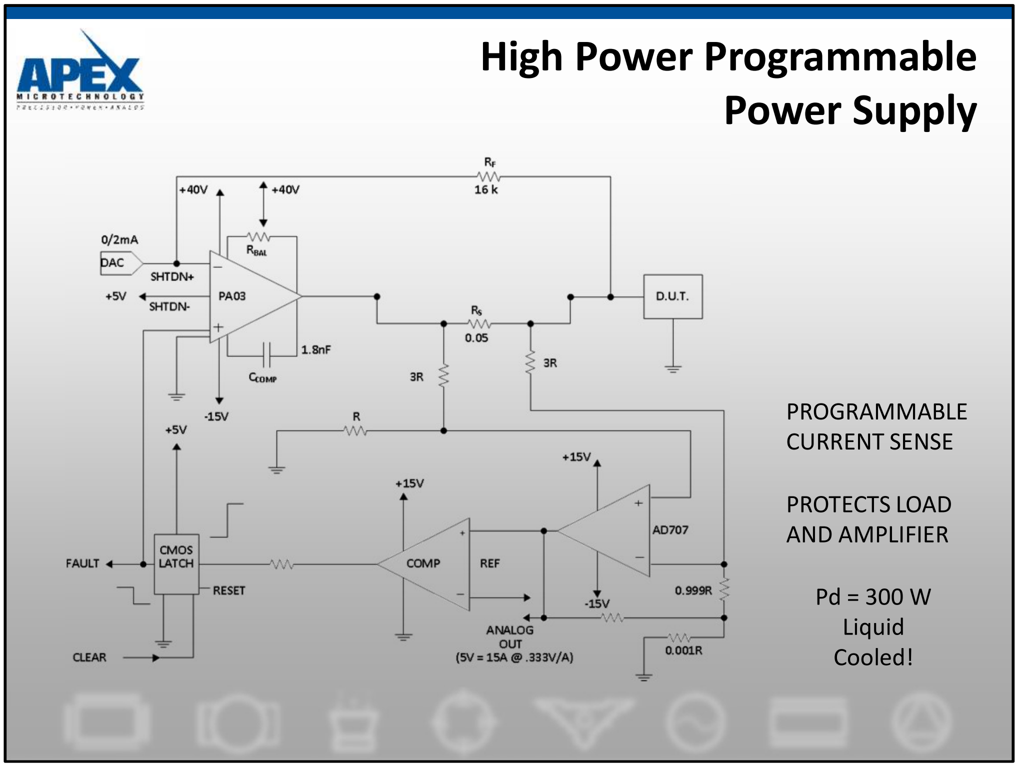


Now that the power stage is stable we add its closed loop gain to the open loop gain of the host amplifier. Note that it is the poles of the power stage rather than the host producing the -40db per decade slope in the area of interest. A roll off capacitor gives us required slope for good intersection rate and noise gain allows good placement of the actual intersection.

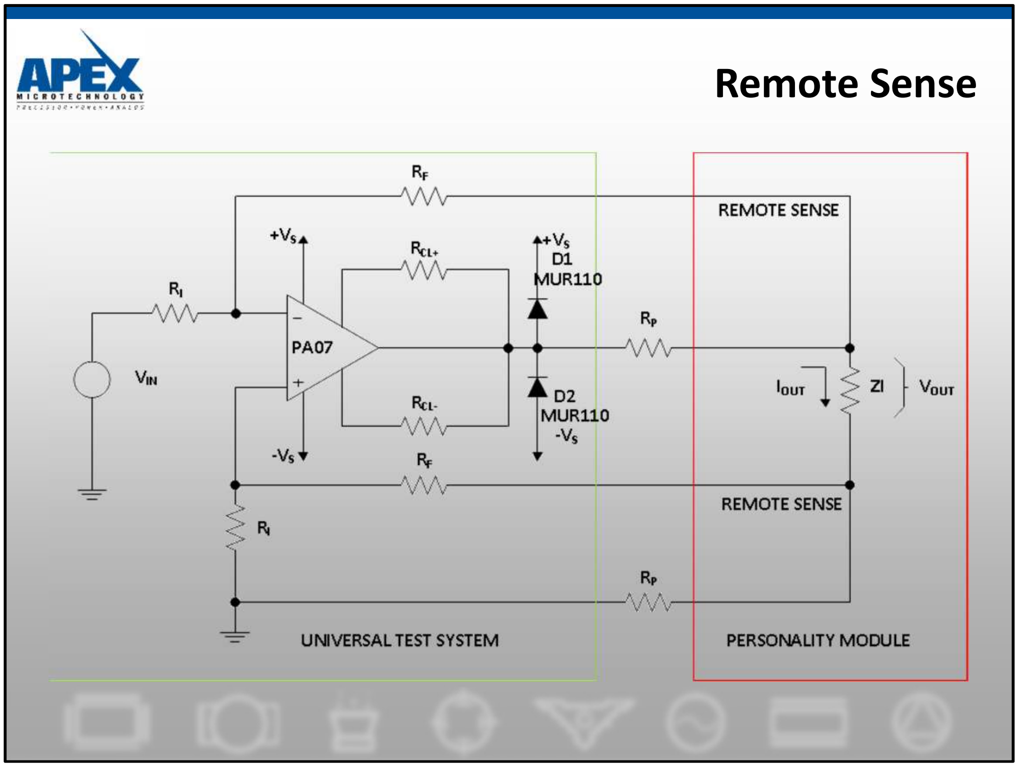
In this circuit final value selection was a result of playing “what-if”, and the phase component graph was very useful. The first pole of the host amplifier is at 0.1Hz giving a 90°open loop phase shift by 1Hz. The first pole of the power stage at just under 1KHz produced 180°at less than 10KHz. Visualizing the phase components moving on the graphs and using the R-C calculator make fairly short work of the design.

Composite Open Loop Phase Plot



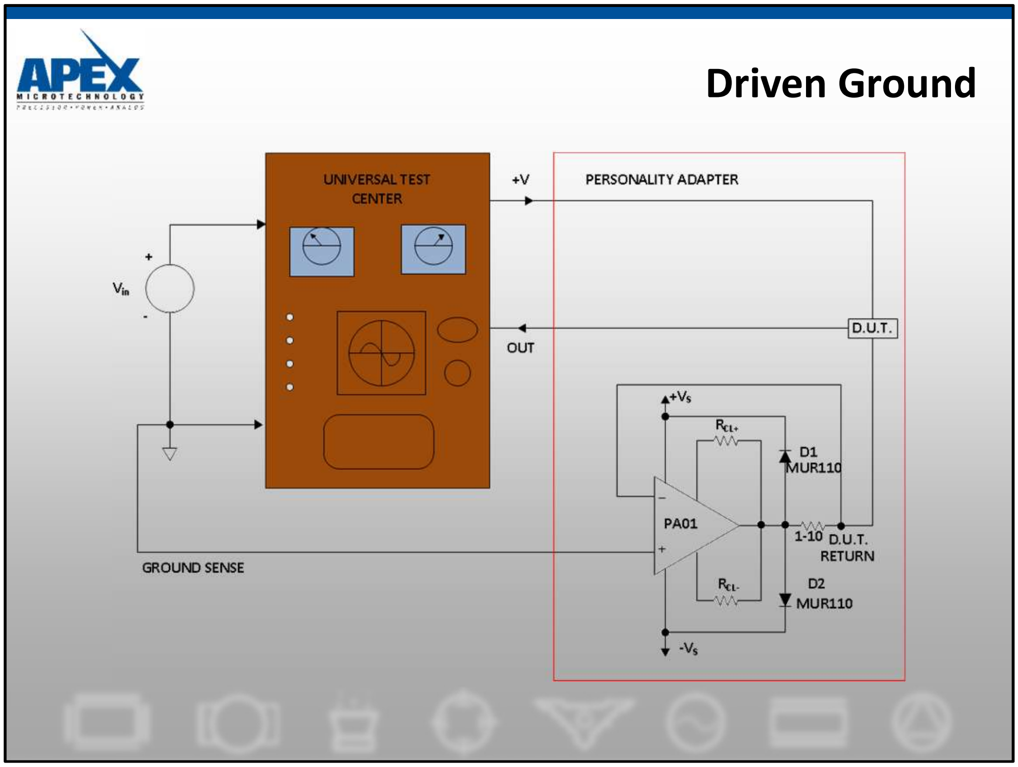


In this circuit the PA03 is being used in a simple, reliable programmable power supply which utilizes the PA03 shutdown features. It requires little calibration because the current to voltage conversion of the DA converter output is done by the power op amp itself while a 12 bit DAC (i.e. DAC80) provided accuracy levels high enough to eliminate the need for adjustment. Rs senses current to the DUT. The AD707 is configured as a difference amplifier which senses the voltage across Rs and develops an analog output signal proportional to DUT current through Rs. It is then compared to a reference voltage which determines the current level desired. The comparator will trip high once this current limit is exceeded thus tripping a CMOS latch low and resutling in a 5V differential signal between the two shutdown pins on the PA03. This circuit is explained in detail in Application Note 6 in the Apex Data Book.

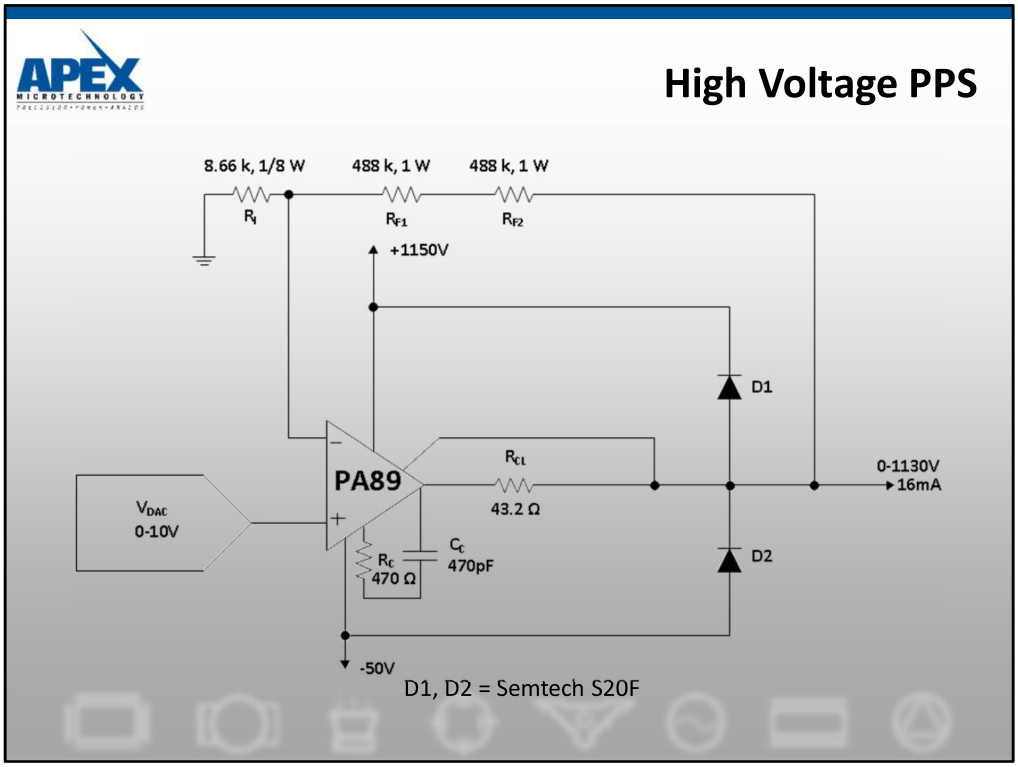


Universal test stations often contain a power op amp that is used to provide power to some remote load. If significant amounts of current are being delivered to this remote load, the parasitic resistance of the wiring can contribute significant errors to the measurements. For instance, 50 milliohms of wire resistance in the output and return line would result in an error voltage of 500mV with a 5A load current. When the power amplifier is configured as a differential amplifier, with the differential plus remote sense and minus remote sense lines being run directly to the load and connected across the load at the remote site, drops from the parasitic resistances become common mode signals to the difference amplifier and are rejected due to the high CMRR of the amplifier.

Ref. AN7



Often a test rack is located quite a distance away from the actual test head where the DUT is being excited, or where measurements are being made. When the equipment at the personality adapter or the test head dumps a significant amount of current into a ground return line, enough voltage may be developed between the personality adapter and the universal test station to contribute significant errors to whatever measurements are being made. One way to solve this problem is to eliminate current flow in the ground line. This circuit accomplishes that feat by taking the reference ground from the universal test station and running a "gound sense" line over the personality adapter. This line is now used as a reference voltage input to a unity gain follower — in this case the PA01. The PA01 is used to generate a "remote ground." Now the ground current from the DUT or remote test equipment is dumped into the output of the PA01 where it is returned to one of the remote supply lines. The 1-10 ohm series resistor is used to keep power dissipation outside of the amplifier and have it dissipated in the resistor instead. Its value should be chosen such that the Imax (ground current) x Rs = Vo max of the PA01.



This high voltage programmable power supply utilizes the full voltage capacity of the PA89. It uses asymmetrical power supplies to eliminate the necessity for biasing up the front end input DAC voltage to comply with common mode voltage requirements of the PA89, as well as providing adequate voltage headroom at the output so it can swing down to zero.

Although the PA89 can be used single supply, it ends up requiring large value resistors and high wattage resistors to bias the front end to comply with the input common mode voltage specification of +/-Vs-/+50. Tthe output would only be guaranteed to swing within 20 volts of ground. Asymmetrical power supplies, as discussed earlier, eliminate both of these problems.

With the current limit set at 16mA the PA89 can withstand a fault condition of a short to ground on the output by using an Apex HS06 heatsink, a TW05 thermal washer, and in a 25°C ambient environment, free air convection cooling.

Although the PA89 generally works at low currents (<60mA), power dissipation is still a major design consideration due to the high voltage (remember P = V x I)

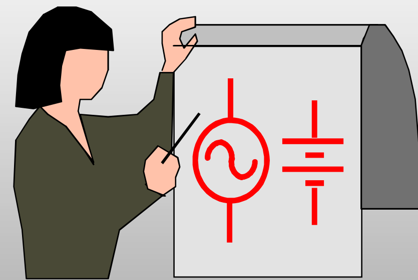
As a high voltage amplifier the PA89 does present some unusual design considerations. The following is a quick check list of support components requiring special attention:

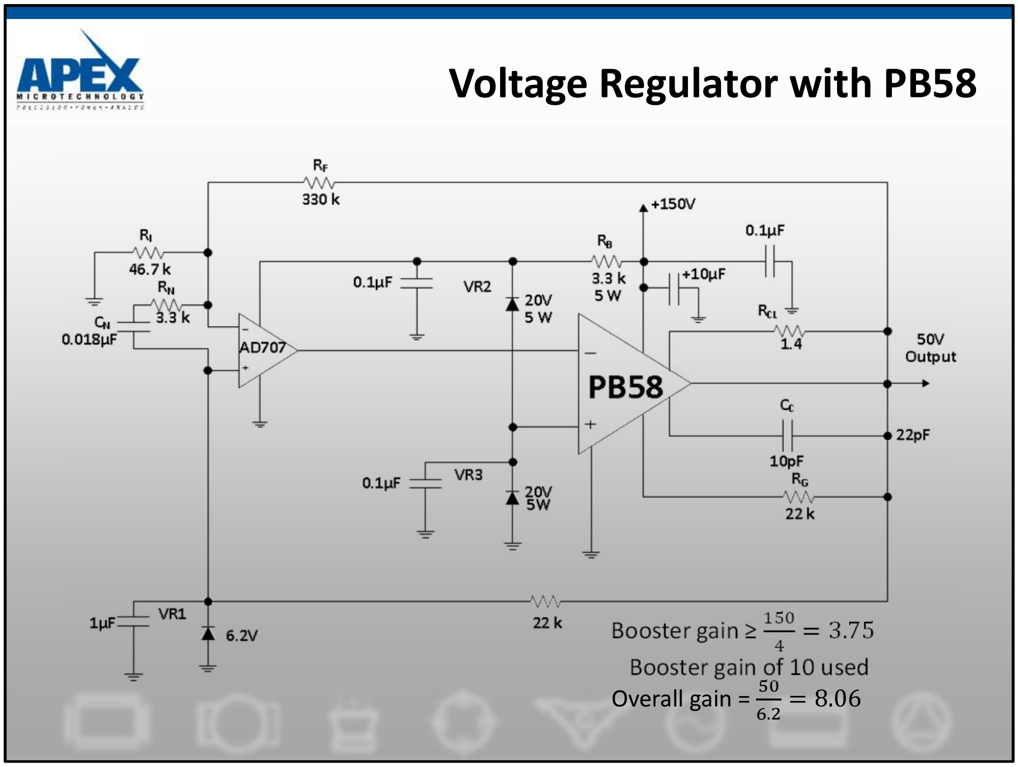
1) Cc—Compensation capacitor will see nearly the full supply voltage. In this case 1200V. Because of corona effects and partial discharge, this capacitor must be rated at twice the total supply voltage. Lower ratings can cause amplifier destruction.

2) RF1 and RF2—Feedback resistors must be selected for power dissipation, voltage coefficient of resistance, and voltage breakdown rating.

3) D1 and D2—Flyback diodes must have a peak inverse voltage rating of the total supply voltage. Here we need a 1200V PIV rating minimum.

Sources

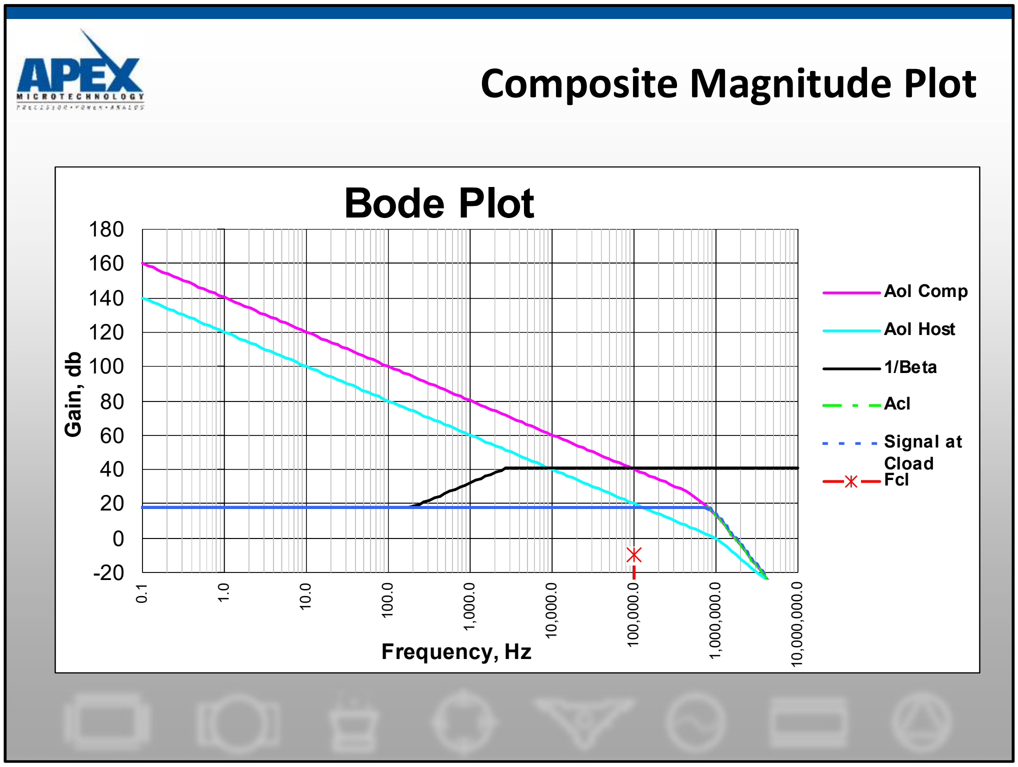




At first this may not seem to be the least costly approach to voltage regulator design. However, there is no packaged solution to regulating 150 volts down to 50 volts while being able to provide up to 500 mA (PB58 is rated up to 2A, but SOA limits us to 500 mA in this application). This regulator has both good source and good sink regulation characteristics.

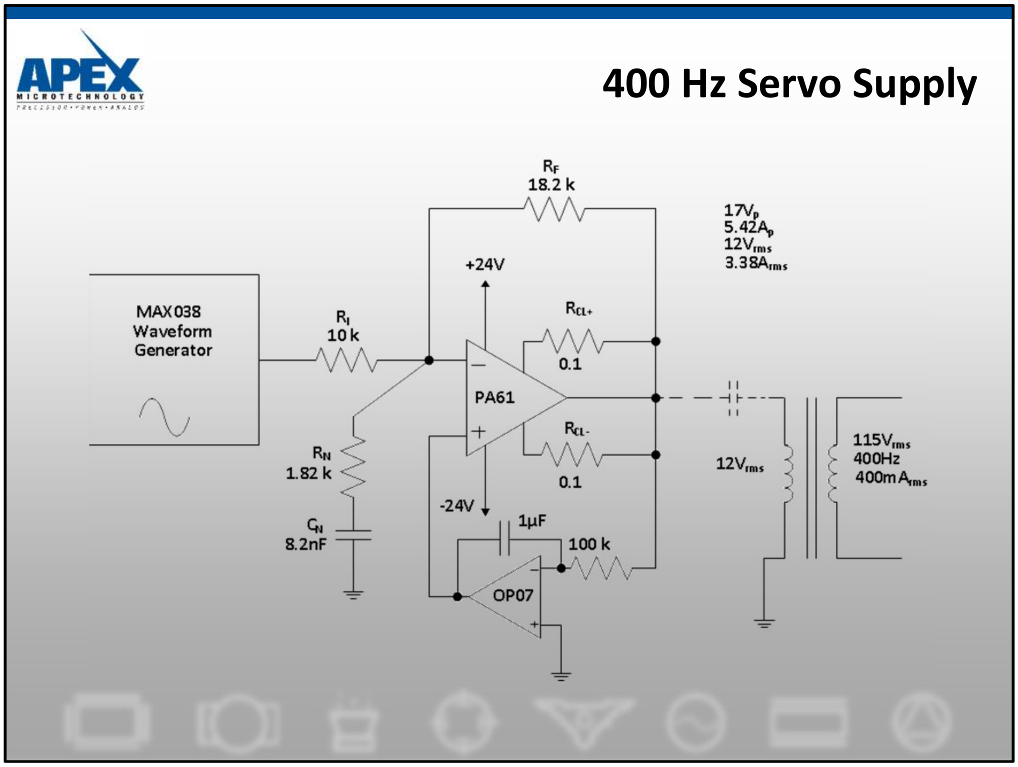
This application does serve well to illustrate PB58 design techniques, and some of the limitations tobe aware of. For instance, in normal applications the negative supply of PB58 must be 15 volts more negative than ground. In this application we have created a quasi-ground at the junction of VR2 and VR3 which meets this requirement. VR2 and VR3 also provide regulated supply voltage for the driver op amp.

The reference zener source is derived from the output of the regulator to improve supply rejection. The overall gain is whatever is necessary to multiply the 6.2 volt reference VR1, up to the required output voltage. In this case a gain of 8.06 for a 50 volt output. In the next few slides, we’ll discuss stability considerations in the booster application.



This circuit is not battling capacitive loading or inductance in the feedback path and each part of the composite would be stable on its own but the composite open loop gain reaches a slope of -60db per decade before crossing 0db.

While a DC gain of 100 (A short in place of Cn) would have made the circuit stable, the DC errors due to offset and drift would have been objectionable. Including Cn keeps DC gain at the desired level and produces a stable circuit.



This 400Hz servo supply uses a separate oscillator to maintain oscillator stability under varying load conditions. The PA61 provides a gain of 1.8 to match the output of the industry standard 8038 waveform generator IC to the primary of a 12V to 115V step-up transformer.

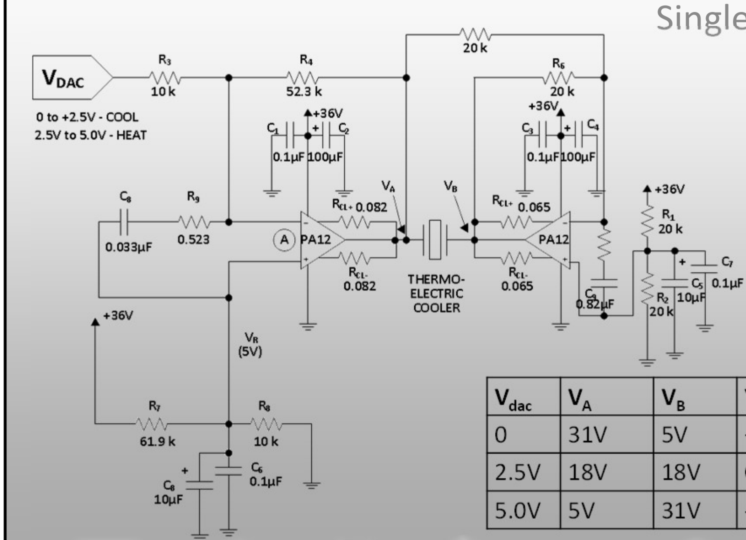
The input R-C network is selected to provide unconditional stability on the PA61 with a phase margin of 45°in the 100Hz to 3kHz region. Phase margin increases to 90°at the 100kHz small signal bandwidth of this circuit. This extra phase margin allows for parasitic cable capacitance and/or capacitive loading on the output of the PA61 with guaranteed stability. The capacitor is selected for a corner frequency of 10KHz since this is well away from the 400Hz signal yet low enough to control any stability problems.

Note that the power supply is set to a value just large enough to accommodate the signal amplitude plus the amplifier's worst case output voltage swing specification. The use of minimum power supply voltage minimizes dissipation and improves efficiency.

If AC coupling should lead to unmanageable size bipolar capacitors, use an integrating amplifier (OP07 in this example) to compensate for offset voltage.

Thermo-Electric Cooler

Single Supply Bridge



V_{dac}	V_A	V_B	V_A-V_B
0	31V	5V	+26V
2.5V	18V	18V	0V
5.0V	5V	31V	-26V

1. Vout = VA-VB
   Max Vout +Vs – VsatA – VsatB
   = 36V -5V -5V = 26Vp

2. Gain = Voutpp/Vinpp = (VA-VB)pp/Vinpp
   52Vpp/5Vpp = 10.4

Gain = 2 R4/R3 since we have a bridge configuration.

The voltage gain across the load is twice that of the primary amplifier, A, since +1V out of the amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +18V

Therefore R4/R3 –=5.2

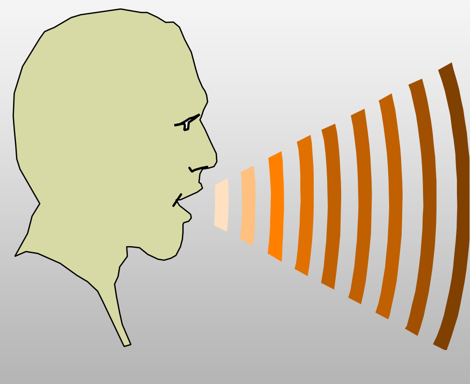
3. Offset

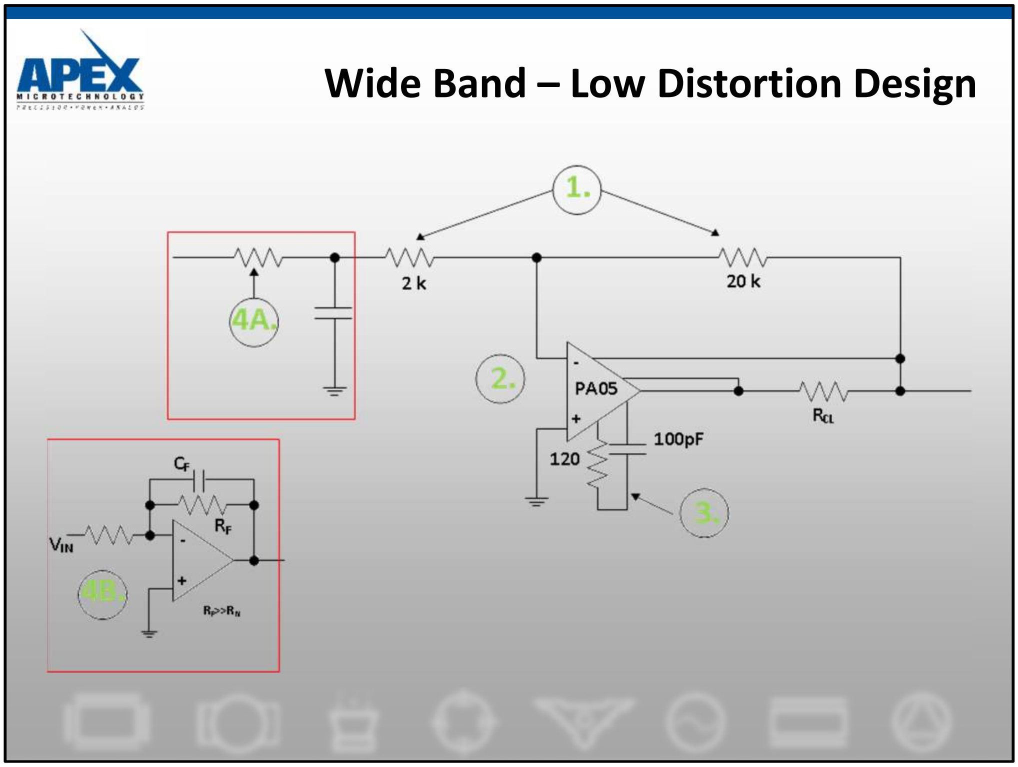
VA-VB + Vs(2(1+R4/R3) $\frac{R8}{R7+R8} - 1)$ – 2(R4/R3)Vdac

But when Vdac = 0 then VA-VB = +26V
Using R4/R3 = 5.2 and solving above yields R7 = 6.2 R8
Choosing R8 = 10K implies R7 = 61.9K

4. Check for common mode voltage compliance:
   5V meets the minimum common mode voltage spec.

Audio





When audio or ATE applications demand the best in distortion and bandwidth, there are four basic rules to follow:

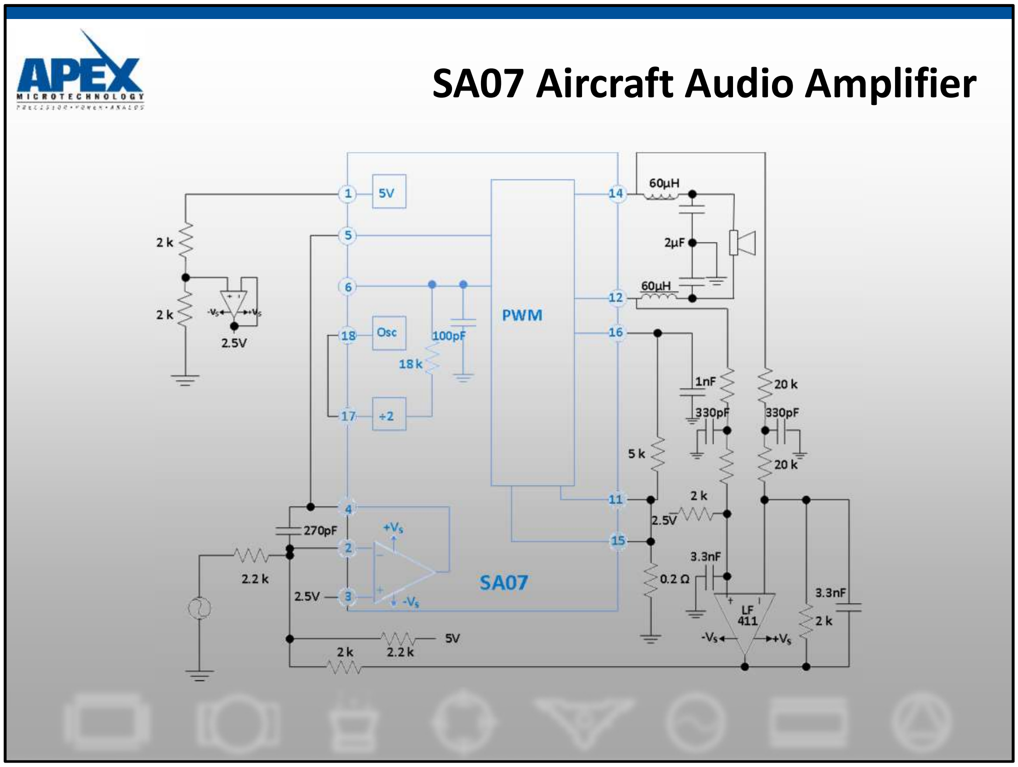
1. Low closed loop gain insures maximum reduction of distortion because of increased loop gain. However, the heavy negative feedback can cause transient response problems during rapid transitions (slew rate overload). Rule #4 will show how to solve the transient response problem.

2. The inverting configuration, by forcing both inputs to 0 (remember your basic op amp theory), eliminates common mode signals and the errors (read: nonlinearities) that they cause.

3. External phase compensation allows the designer to tailor the circuit to the minimum acceptable compensation. This increases high frequency loop gain to further reduce distortion, especially at high frequencies. Consider noise gain compensation to improve stability for low gain and small compensation capacitors.

4. Input slew rate limiting (4A) designed to keep input signal transitions within the slew rate limit of the amplifier will eliminate transient overload problems. 4B) You may use an integrator to accomplish this function, while RF /RI pre-amplifies the input signal to accommodate a low power stage gain. Then Cf = Vin/Rin • Acl /SR.

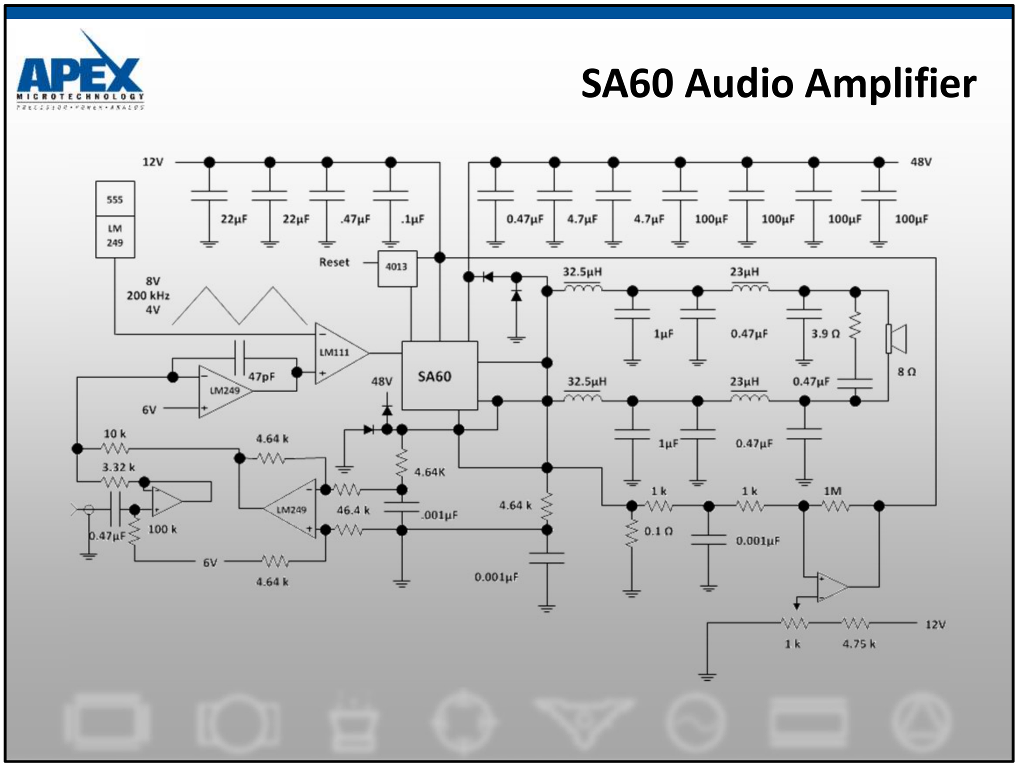
Ref. AN17



Weight is right at the top of the list of things airliners don't want. This is where the SA07 becomes the best choice for cabin audio. Heatsink concerns make PWM a natural choice and 500KHz switching cuts down the size of capacitors and even more important, the inductors. Not only is size and weight for a specific inductance reduced compared to a lower switching frequency, but having a wider band between switching and signal frequencies yields a filter with fewer components (a lower order filter). The filter is based on Power Design recommendations given 28V supply, 15KHz signal bandwidth and maximum ripple of 25mVpk.

The differential voltage amplifier has two poles at about 23.5KHz, a gain of 1/20 and the output is referenced to 2.5V. The integrator amplifier is also referenced to 2.5V and scaled to 1Vrms inputs which are ground referenced.

While not shown here, make no mistake about it, selection of bypass capacitors and careful layout make or break this application. In addition to 10µF per ampere low frequency bypass, use lower value ceramic chip capacitors to achieve low ESR well into the MHz region.

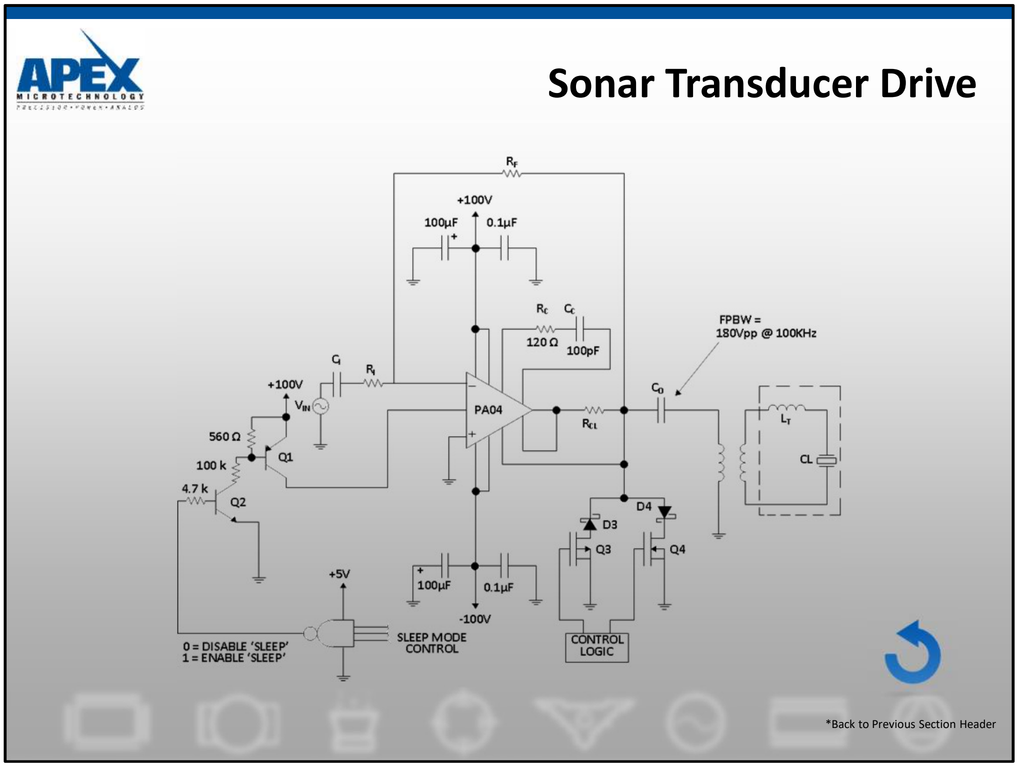


This class “D” audio amplifier is cost effective, cool running, good sounding and delivers up to 100W. Does any one know what this number would be if you bought the equipment as consumer audio gear?

Tested efficiency of this circuit was 80.6% at 60W output, meaning 14.4W wasted. A theoretical linear power stage would dissipate 72W delivering the same output from ±48V supplies. Again, roughly that 5:1 heatsink savings of PWM over linear.

Operation of the overall circuit is similar to previous voltage output designs except there are more functions external to the PWM amplifier. The LM111 generates the PWM duty cycle based on the 6V referenced ramp and input signals. The SA51 converts this to power pulses. The filter removes most of the 200KHz switching frequency for the speaker. The differential amplifier also converts power pulses to an analog feedback signal. Over current is detected and latched to disable the power stage. Response time in the area of 5µs is required.

Capacitor arrays seen decoupling the supplies are not overkill. Larger values do a good job at lower frequency, lower values keep ESR low at the high end. Select capacitors specified for high current switching applications.



High current drive capability and wide power bandwidth make the PA04 ideally suited for sonar drive applications.

Often the amplifier is required to drive the primary of a transformer to step-up its output voltage to a desired high voltage for end drive to the sonar transducer. Because transformers do not work well when saturated it is essential to minimize DC current flow in them. AC coupling of the input signal and/or the output minimizes and/or eliminates the DC input offset voltage of the PA04 from becoming gained up by the gain of the amplifier, creating a large DC offset at the output.

Often times, either through the construction of the transformer or through an additional inductor, Lt, the sonar transducer, predominantly capacitive by nature, is tuned to look resistive for a narrow band of frequencies. This minimizes SOA stresses on the PA04. It is a good idea however to consider worst case capacitive loading reflected to the primary of the transformer onto the PA04 for AC stability considerations, should there be a possibility of non-resonant frequencies being applied to the sonar transducer drive circuit.

Another feature of the PA04 which is especially helpful in battery operations is its sleep mode function which can be used to turn the amplifier off during periods of non-use to minimize battery drain. Sleep mode quiescent current is only 5mA and the output is turned off into a high impedance state.

One caution when using sleep mode is to be aware of transients up to the supply rail that can occur during transitions into and out of sleep mode. There is no esoteric way to eliminate these internal to the op amp. If these transients would provide undesired transmissions, the problem can be cured through the use of two Schottky diodes (D3,D4) and two MOSFET switches (Q3,Q4). These components short the output of the PA04 to ground during the sleep mode transitions.

Timing logic going into sleep mode is to first command the input to zero, switch on Q3 and Q4 and then enable sleep mode. Coming out of sleep mode we would first ensure input signal is zero, ensure Q3 and Q4 are on, disable sleep mode, turn off Q3 and Q4, and finally begin transmitting with our input signal. Typical delay time to squelch the sleep mode transients is about 5-10 mS.

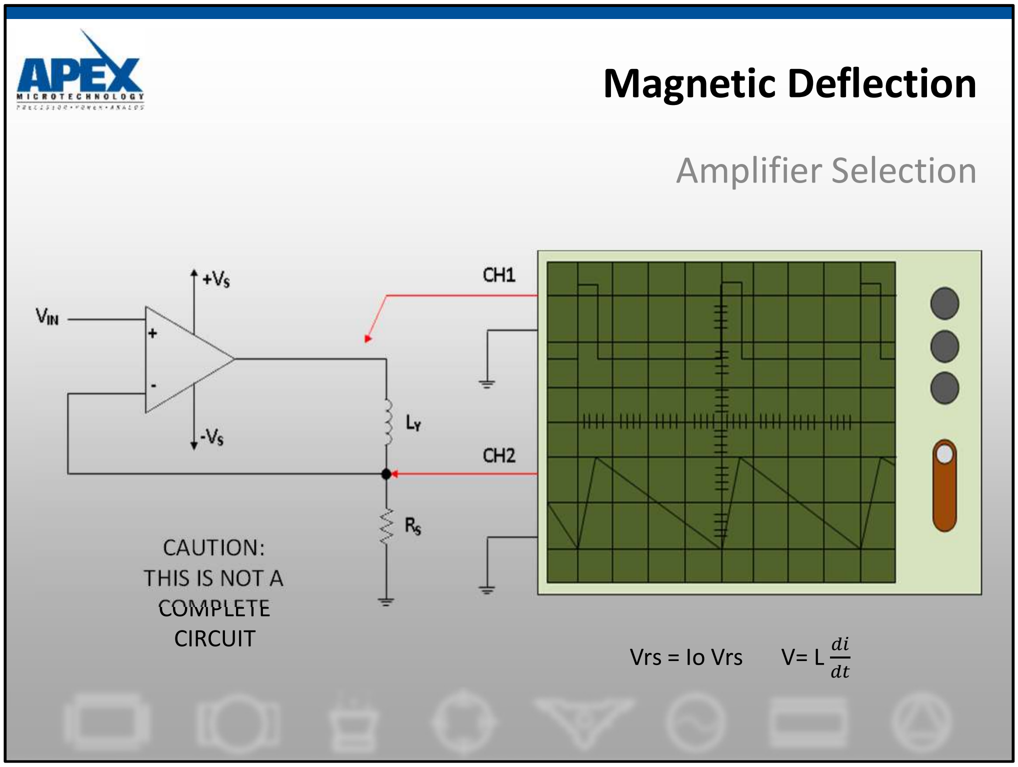
As a final note, to minimize SOA stresses it is advised to always start the input signal at zero crossing and exponentially ramp the amplitude if possible, since a transformer really doesn’t look like a transformer until we have passed a few cycles of AC through it.

DEFLECTION

Deflection

- Electromagnetic
- Electrostatic
- Dynamic Focus Control

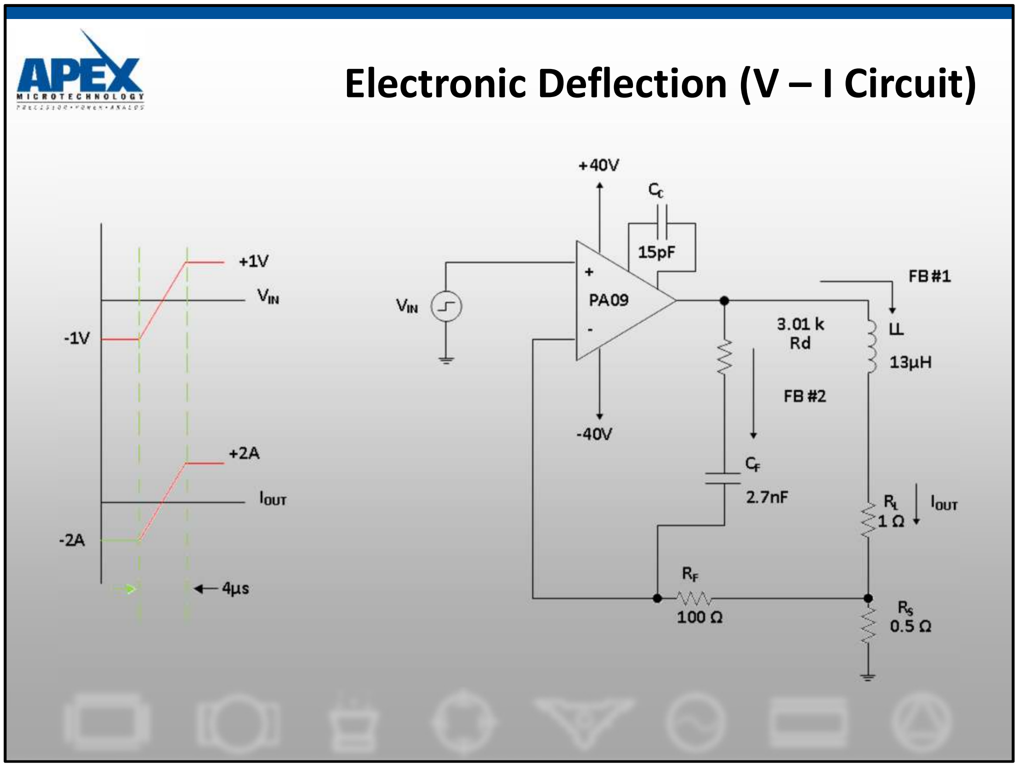
High speed power op amps are ideal candidates for all types of deflection uses. High current, high speed models are ideal for electromagnetic deflection. Models with rapid slew rates and extended supply ranges allow rapid dI/dt of the yoke being driven. High voltage models are especially useful for electrostatic deflection and/or focus.



An amplifier selected for magnetic deflection must have an adequate slew rate and voltage rating to slew the current in the yoke fast enough.

These two considerations go hand in hand since the rate-of-change of current in the yoke is proportional to applied voltage. And the amplifier must slew to this applied voltage at least 10 times faster than the rate of change of current to achieve truly fast and accurate magnetic deflection.

Ref. AN5



Amplifier Selection:

Step 1: Voltage

$V_{LL} = LL \frac{Dip-p}{dt}$ $\qquad$ $V_{LL} = 13\mu H \frac{4A}{4\mu s} = 13V$

$V_S = V_{LL} + V_{RL} + V_{RS} + V_{sat}$ $\qquad$ $V_{SMIN} = 13V + 2V + 1V + 8V$

Where: $V_{RL} = Ip\ RL$ $\qquad$ $V_{SMIN} = 24V$

$V_{RS} = Ip\ Rs$

Step 2: Current From desired I_{out}, current must be 2A

Step 3: Speed

A design rule of thumb for good performance is to select an amplifier with a minimum slew rate equal to 10 times faster than the desired current slew rate, faster will be better.

$S.R._{MIN} = \frac{V_{S\,NIN}}{(.1)dt}$ $\qquad$ $S.R.\ MIN = \frac{24V}{(.1)(4\mu s)} = 60V/\mu s$

Step 4: PA09 and PA19 meet or exceed these requirements. PA09 is less expesnive.

Ref. AN5

PA09 Deflection Setup

STABILITY FOR INDUCTIVE LOADS

MODEL	PA09-150	Note/PBs	Rin	99999999999	Kohms	Estimated Closure Frequency =	3162.278	KHz
Rs	0.5	Ohms	Rf	0.1	Kohms	Suggested maximum bandwidth	177827.9	Hz
Lload	0.013	mH	Cf	2.7	nF	Estimated Closure Rate =	20.0	db/decade
Rload	1	Ohms	Rd	3.01	Kohms	Estimated Phase Margin =	45.63	Degrees
		Is this a Composite?		No				
Notes:								

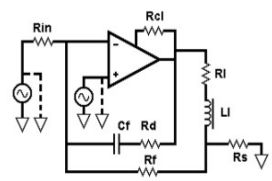
R-C Pole Calculator +:

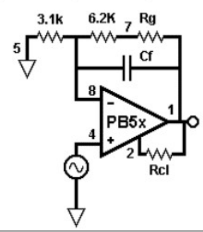
3.01	Kohms	Rd Kohms	1.16509	AC gain db	30
20000	Hz	Rd Kohms	2.9	Rd Kohms	3.062278
2.6438	nF	Cf nF	2.081381		

28 Print Data, Bode & Phase

29 Print Data, Bode, Phase & Parts

Ri/(Ri+Rf)	1	
Equiv Z @ Rs	0.5	Ohms
Requiv/(Rl+Requiv)	0.333333333	
DC Beta	0.333333333	
DC Gain	9.542425094	db
Zero R/L	18364.0319	Hz
Rin||Rf	0.1	Kohms
Zero Rd/Cf	19583.48013	Hz
AC Gain	29.85520778	db
Zero Cross	177827.941	Hz



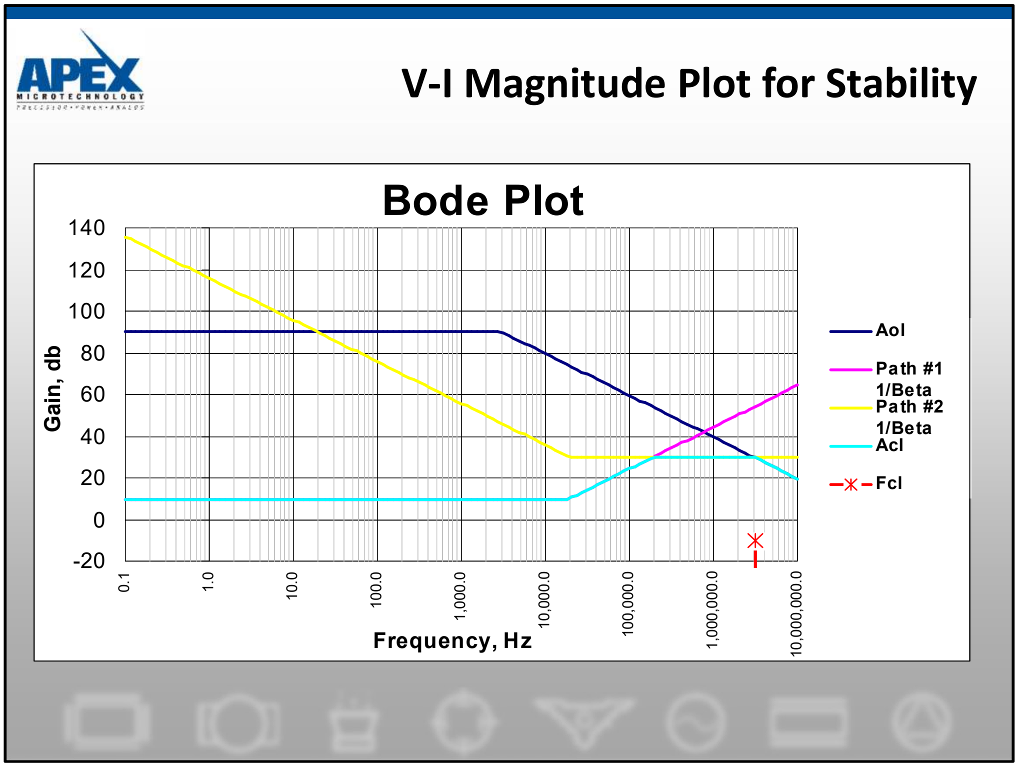


Set up the basic circuit in Power Design to see we have a 17 degree phase margin. Visualize the flat portion of feedback path #2 at about 30db. This is well below the intersection point and gives a nice round gain increase of 10x or 30 total. Estimate the line will cross the closed loop gain at about 200KHz.

Considering the inductor open and Cf shorted, AC gain will be roughly Rd/Rf. Put 3.01K and 20KHz (a decade below our estimated cross) in the R-C Pole Calculator. Enter 2.7nF for Cf.

We have good phase margin and an suggested maximum frequency of 178KHz. This suggestion is the lower of two criteria: The cross of the two feedback paths (the case here) or the frequency where loop gain is 20db (difference between open loop and closed loop gains).

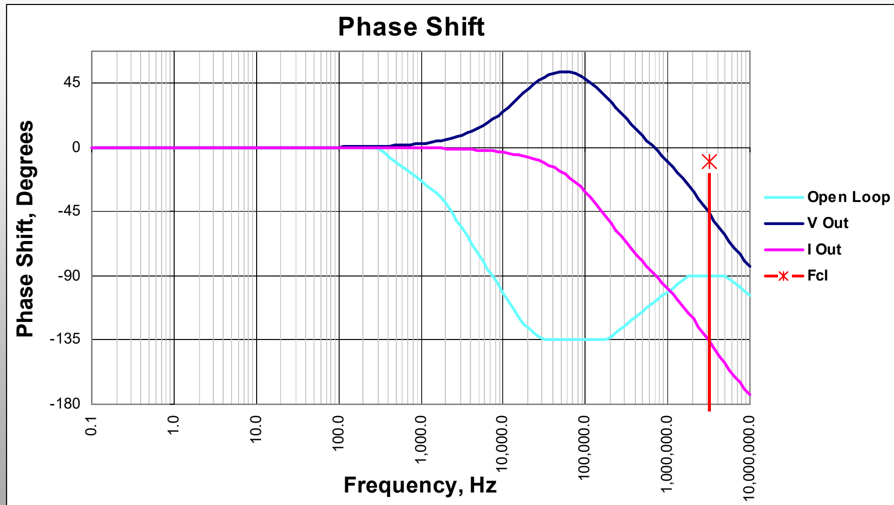
Ref. AN38



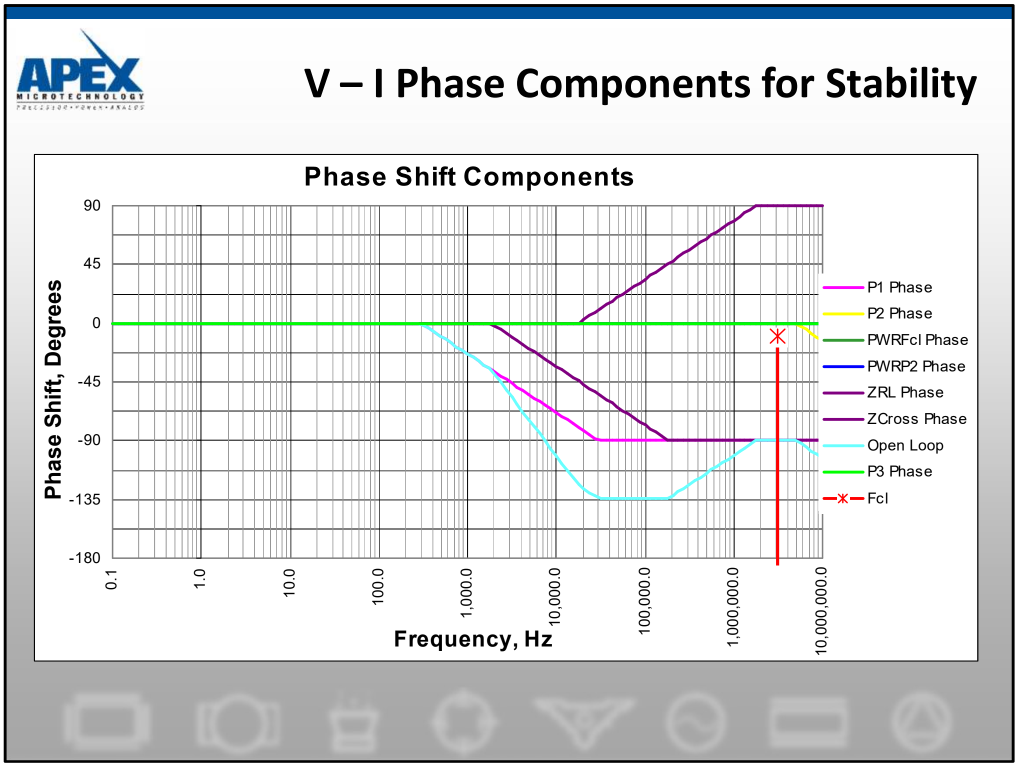
V-I Magnitude Plot for Stability
Bode Plot
140
120
100
80
60
40
20
0
-20
Gain, db
0.1
1.0
10.0
100.0
1,000.0
10,000.0
100,000.0
1,000,000.0
10,000,000.0
Frequency, Hz
Aol
Path #1 1/Beta
Path #2 1/Beta
Acl
Fcl

Ref. AN38

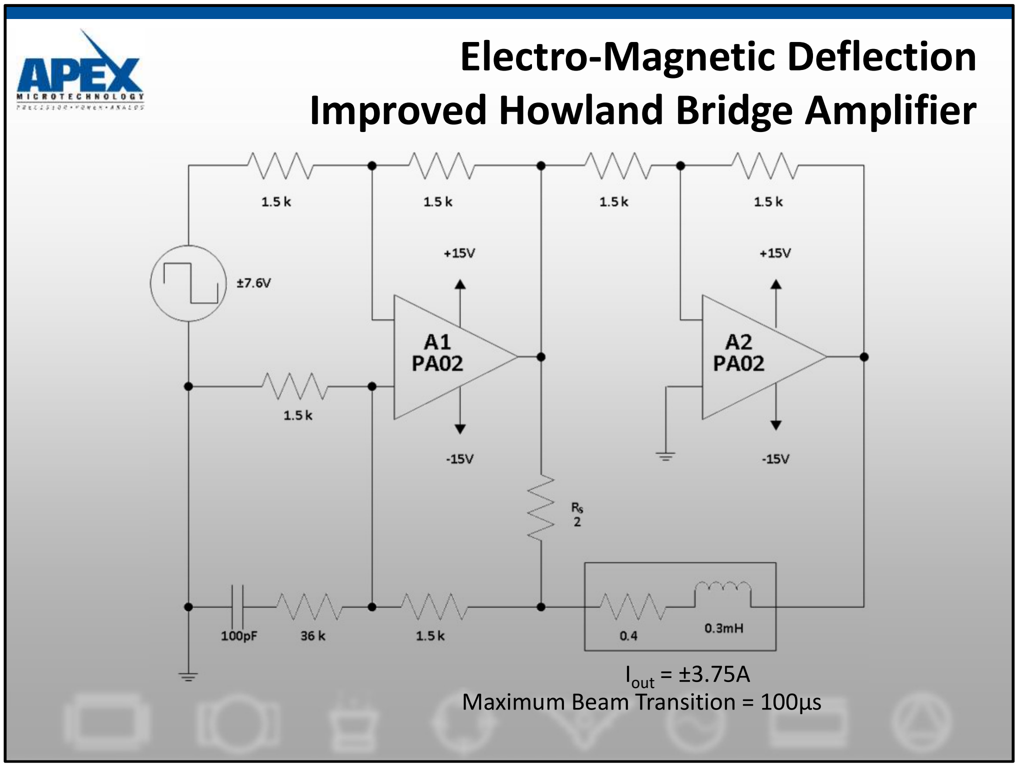
V – I Open Loop Phase Plot for Stability



Ref. AN38


V – I Phase Components for Stability
Phase Shift Components
Phase Shift, Degrees
90
45
0
-45
-90
-135
-180
0.1
1.0
10.0
100.0
1,000.0
10,000.0
100,000.0
1,000,000.0
10,000,000.0
Frequency, Hz
P1 Phase
P2 Phase
PWRFcl Phase
PWRP2 Phase
ZRL Phase
ZCross Phase
Open Loop
P3 Phase
Fcl

Ref. AN38

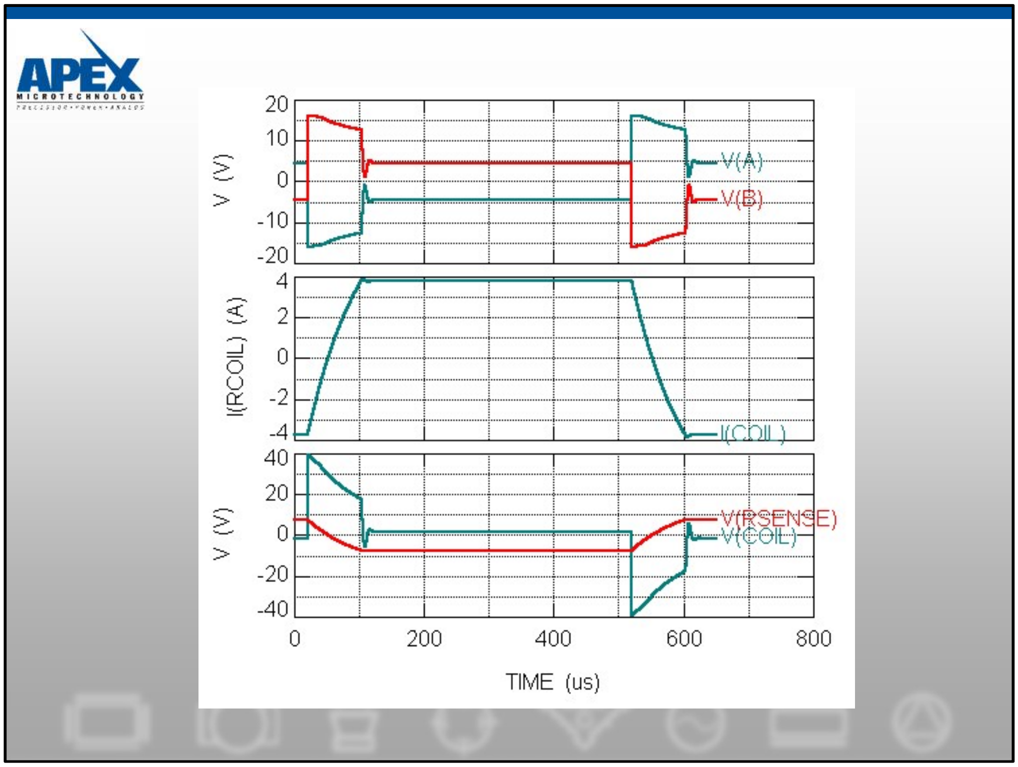


A1 is a Howland Current Pump, A2 provides a gain of –1 to drive the opposite terminal of the coil. A first glance, it might appear the choice of 2Ω for the sense resistor is quite large because the peak voltage drop across it is 7.5V, or half the supply voltage.
Voltage across the inductor required to move the beam is given by:
VL = L * Δ I / Δ t VL = 300µH * 7.5A / 100µs = 22.5V

If one were to add to this the peak voltage drop across the coil resistance (1.5V) and the sense resistor (7.5V), it would be easy to assume a total swing of 31.5V or greater than 15V at 3.75A would be required of each amplifier.

Salvation for this problem lies in analyzing current flow direction.

Ref. AN5



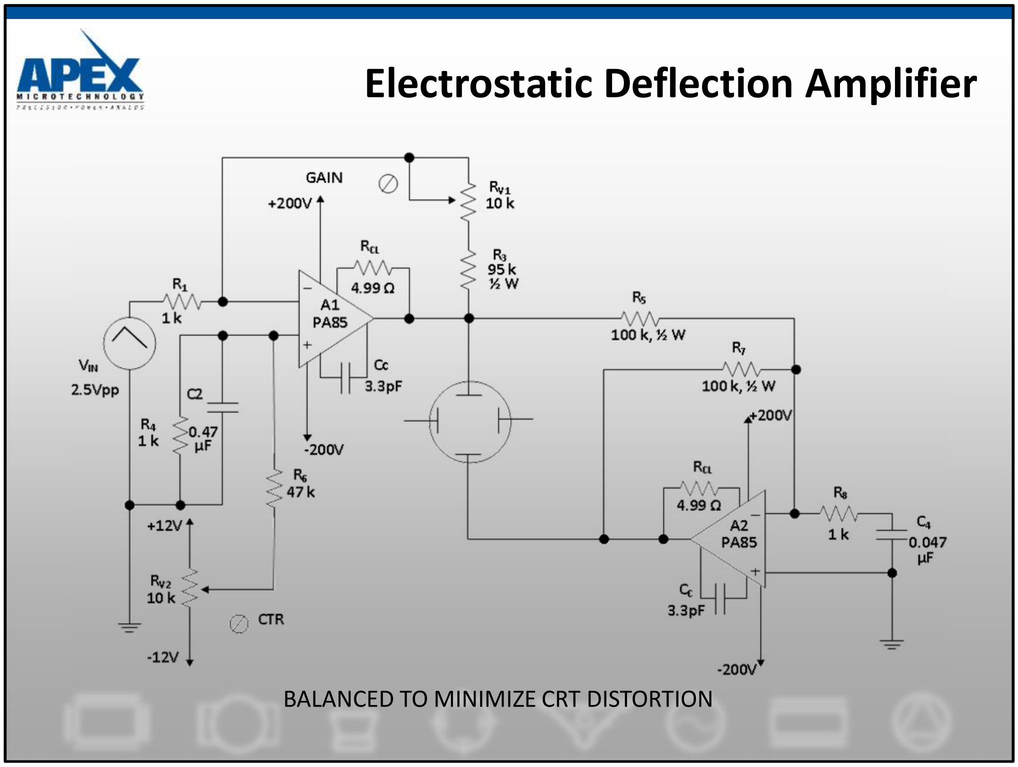
Check out the middle graph. Did you expect me to show you anything but a good current waveform? The main portion of the transition is complete in about 80µs and settles nicely.

In the top graph, we find surprise #1; both amplifiers are actually swinging OUTSIDE their supply rails. The “upside down” topology of the output transistors in the PA02 allows energy stored in the inductor to fly back, turning on the internal protection diodes. The result is peak voltages in the first portion of the transition greater than total supply.

In the bottom graph, we find surprise #2; stored energy in the inductor develops voltage across the sense resistor which ADDS to the op amp voltage until current crosses zero. In this manner, peak voltage across the coil is nearly 40V!

The seemingly large value of sense resistor did not kill us on voltage drive requirements and gives us two benefits: First, internal power dissipation is lower than with a smaller resistor. Secondly, with larger feedback signal levels, the amplifier closed loop gain is lower; loop gain is larger; fidelity of the current output is better; and voltage offset contributes a lower current offset error.

Ref. AN5

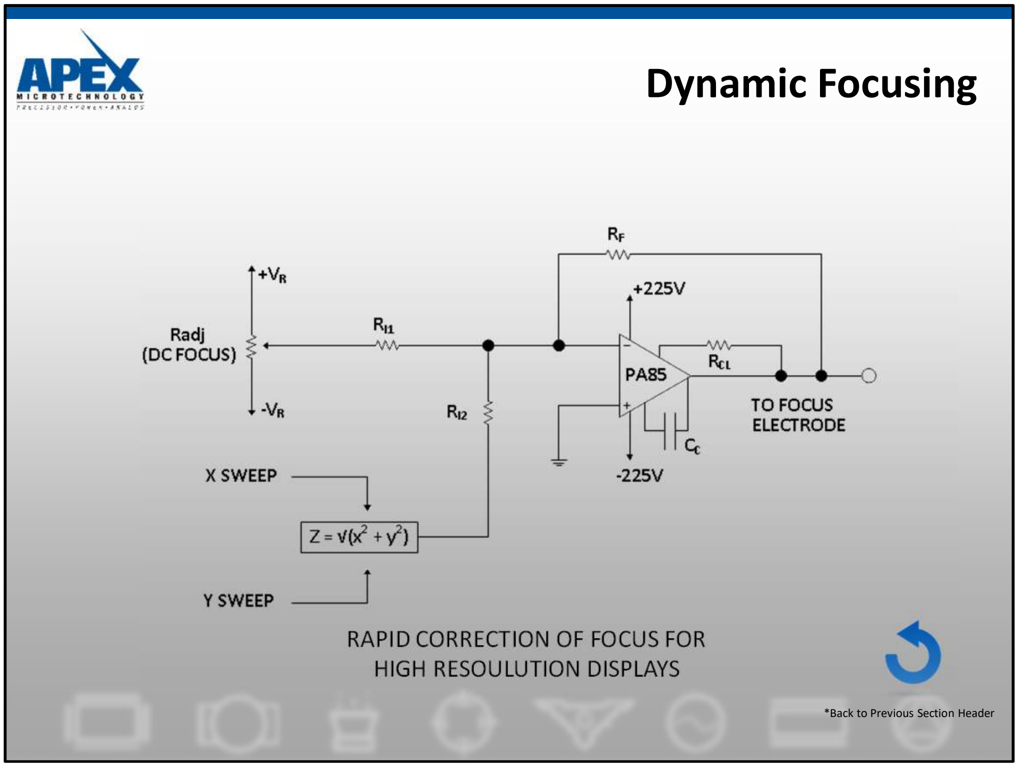


The PA85 was chosen for this application for its high voltage and high speed characteristics. Full bridge drive is utilized to provide a balanced drive to the CRT plate. Bridge drive is useful to reduce geometric distortion in electrostatic deflection applications.

A1 is the main amplifier operating at a gain of 100. This high gain permits minimal phase compensation for maximum speed performance.

follower amplifier A2 is operated at a feedback factor of 1/2, that is an inverting unity gain. To get the same benefit of high speed that A1 enjoys due to the minimum compensation requirements, A2 is fooled into thinking it has a gain of 100 with the use of R8 and C4. This results in A2 having the same small signal bandwidth and high frequency gain as A1, which allows symetrical bridge slew rates since A1 and A2 now use the same Cc compensation capacitor. This is the “Noise Gain Compensation” trick discussed earlier.

Ref. AN3



In a flat screen display system the distance from the source of the beam to the screen changes as it deflects on the screen, from left to right, and from top to bottom. As a result of this a dynamic focus is required to keep the beam in focus, no matter where it is located on the screen.

A normal CRT screen does not have to overcome these distance differences, since the distance from the source of the beam and the screen are the same no matter where you are on the screen, by virtue of the curvature of the screen.

To achieve electrostatic dynamic focus requires an amplifier with high voltage and high slew rate, as it is important to rapidly change the focus to keep the beam focused, regardless of screen position. The 450V, 1000V/µs slew rate PA85 is the ideal choice.

X and Y location sweep information is summed and scaled to provide the proper focus bias to the focus electrode. A DC offset sets the focus at the center of the screen.

Don't forget the heatsinking on the PA85 as the high slew rate requires a high quiescent current which in combination with the high power supply voltage will result in 11.25W of quiescent power dissipation. A PA85 can cook, from a slew rate standpoint, and will literally cook without proper heatsinking!

HIGH POWER TECHNIQUES

Dead Op Amps Don't Power Much

Who, me? Read the book?

- AN1 General Operating Considerations
- AN8 Optimizing Output Power
- AN9 Current Limiting
- AN19 Stability for Power Amplifiers
- AN25 Driving Capacitive Loads

- Subject Index

We've heard of the male stereotype character who reads directions only as a matter of last resort. This anonymous author isn't much of a reader but after a few explosions, I broke down and opened the book- -the Apex book of course.

Better than ¼ of the book is application notes, arranged mostly by type of application rather than amplifier model. This along with a comprehensive subject index make this book very valuable.

Here's my suggestion: Thumb through at least the Ap Notes above looking at pictures and paragraph titles. Then check out the index in the back.

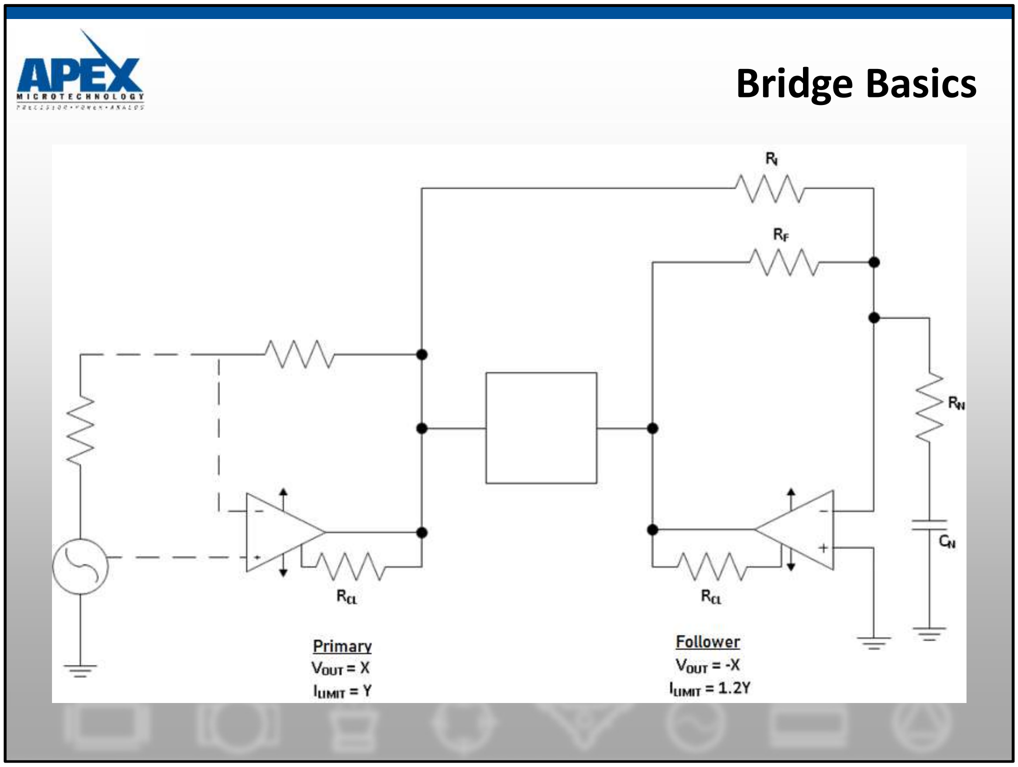
Quiz for today: What is the Apex Cage Code?

The Bridge Circuit

- Double the voltage swing
- Double the slew rate
- Double the power

- Bipolar drive on a single supply
- More efficient use of supplies

There are two basic categories of motivation to use the bridge circuit. The most common is doubling the voltage capability of the whole line of power op amps. The second category solves some limited supply availability situations.



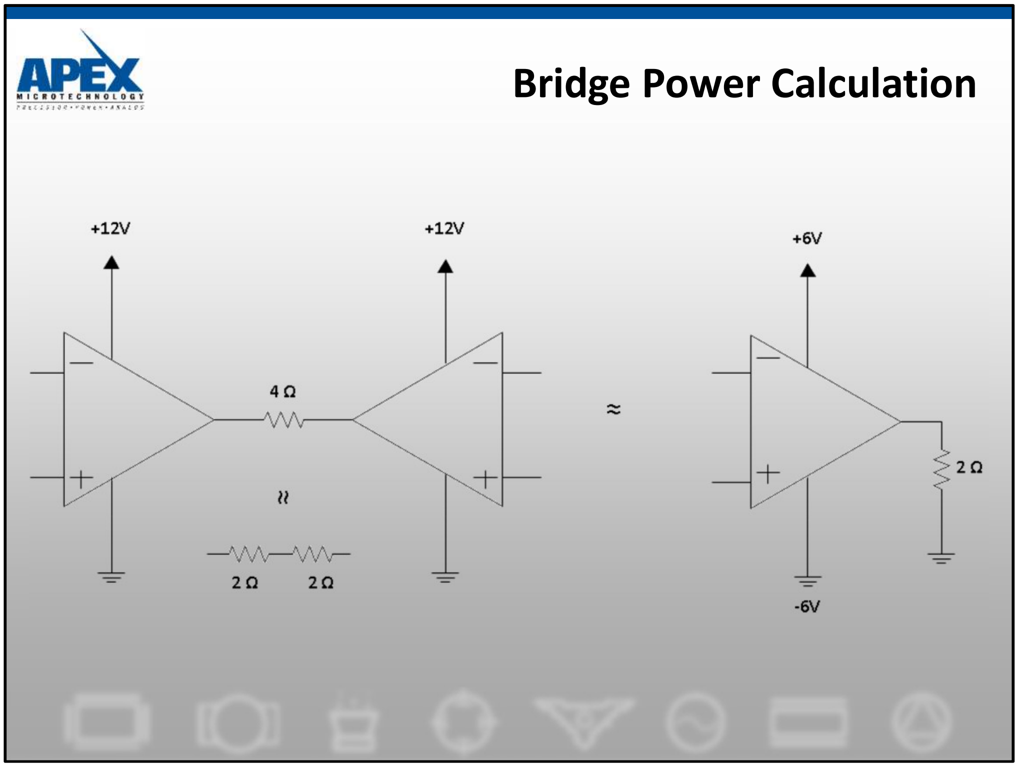
The primary amplifier in the bridge may be configured in any manner suitable for a single version of the particular model. Set gain of the primary for ½ the total required to drive the load. The follower provides the other half of the gain by inverting the output of the primary and driving the opposite terminal of the load. Dual supply operation is the easiest but asymmetric or single supply versions are also common.

The R-C network is often used to fool the follower amplifier into believing it is running at the same gain as the primary. This is important when using externally compensated amplifiers at other than their lowest bandwidth compensation. Set Rn for Rin||Rn = Rf/gain of the primary. Set Cn for a corner frequency with Rn at least 1½ decades below unity gain bandwidth.

Consider a shorted load. Tolerances make it impossible to set identical current limits on the primary and the follower; one will go into current limit, the other will never reach the limiting level. Assume the primary limits and the follower reduces its drive to the load also because it is still in a linear inverting mode. With both amplifier outputs going toward zero, power dissipations are equal and worst case is Ilimit * ½ total supply.

If the follower limits first, the primary remains linear and capable of driving to either rail leaving a power stress on the follower of Ilimit * total supply.

Ref. AN20



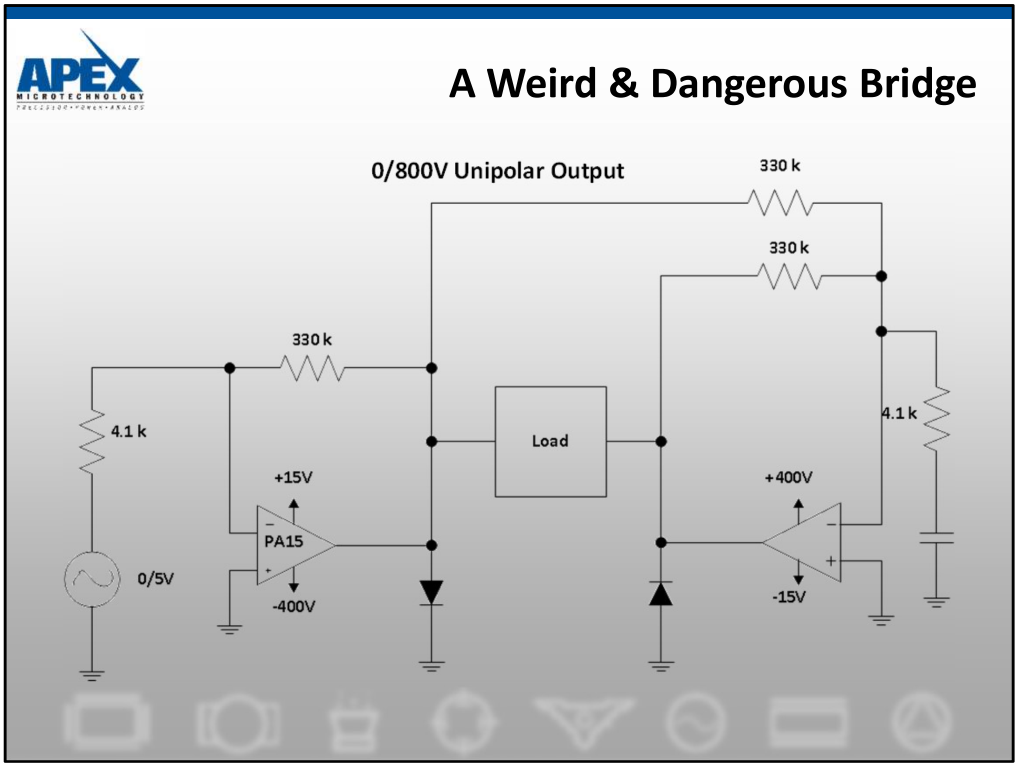
There are several formulae available for calculating worst case power dissipation in a power amplifier (refer to APEX catalog "General Operating Considerations" as well as previous seminar text). These formulae are based on a single power op amp using bipolar, symmetrical supplies. But what about this single supply bridge?

Instead of attempting algebraic manipulation of the formulas, try using circuit algebra. Knowing the primary and follower drive equally but in opposite directions tells us the ohmic center of the load does not move. This leads to an equivalent two resistor load where the center voltage can be calculated. When using dual symmetric supplies the center is almost always ground and we have an equivalent circuit right away.

For the single supply the center of the equivalent load is almost always the mid-point of the supply. Simply lowering all voltages by the load center voltage yields the same equivalent circuit. Simply calculate power dissipation of the equivalent and don't forget to double this figure.

If you are using Power Design you will need the voltage translation portion of this exercise, but not the equivalent load. Enter the total load, total signal level and "Yes" in the bridge question yellow cell.

Ref. AN37



No, this is not the most common bridge circuit. But consider that the only other choice above 450V total supply is the PA89 which is quite slow and costs about $200 more than two PA15 amplifiers (both @ 100 quantity).

Dangerous? Any 800V circuit qualifies for this description but from the op amp point of view this one is a little more so because there are voltages in the area greater than his supply rails.

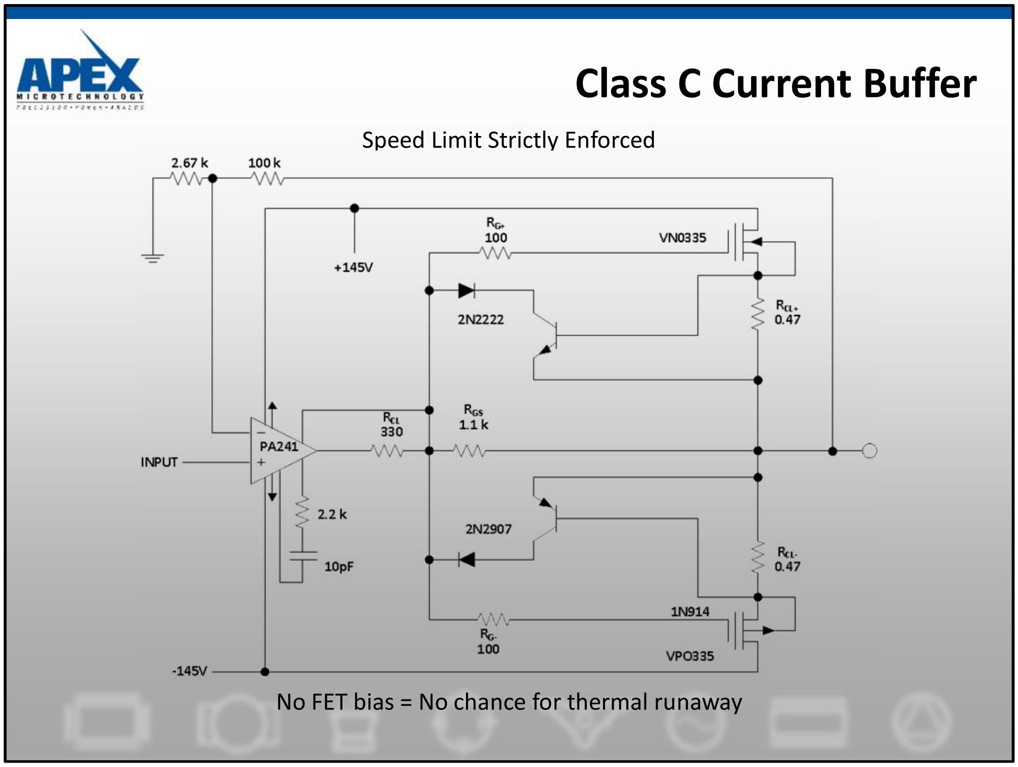
The left hand op amp swings 0 to -400V; the right hand from 0 to +400V. With the load looking at these two voltages differentially it sees 0/800V.

Consider a shorted load causing the right hand amplifier to current limit. If the left amplifier ever goes below -15V, he can destroy his partner. The diodes prevent this.

Ref. AN20 UNIPOLAR OUTPUT

Output Current Buffers

- Multiplies power & current capabilities
- Small loss of swing capability
- More prone to oscillate

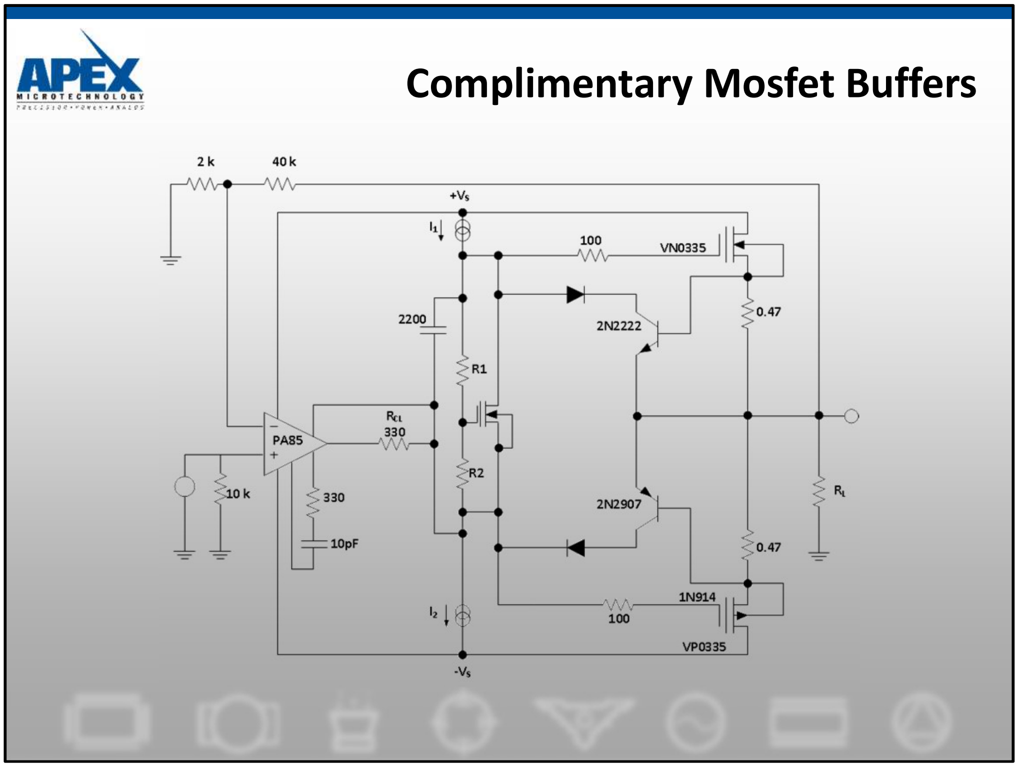


The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages of transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300V in this case.

Current limits work like the circuits we covered earlier. Power dissipation requirements for the MOSFETs can also be found with methods we learned earlier, just remember the power is split between the two packages if the signal is AC only. Power Design will calculate the watts, plug in the driver amplifier, the real load and ignore the red flags.

The 330 Ω current limit resistor sets the PA241 current limit to approximately 9mA. This current flowing across RGS limits drive voltage on the MOSFETs to 10V. This current also lowers crossover distortion. Worst case (during output stage current limit) power dissipation in the PA44 will then be 1.3W due to output current plus 0.6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing Rgs will a 10 to 12V bi-directional zener will allow a cooler running op amp at the cost of increased distortion.

If more power is required than a single pair of MOSFETs can handle, additional MOSFETs may be added in parallel. Each device needs its own source resistor and gate resistor but the small signal current limit transistor and diode need not be duplicated.
Ref. Use High-Voltage Op Amps to Drive Power MOSFETs, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.

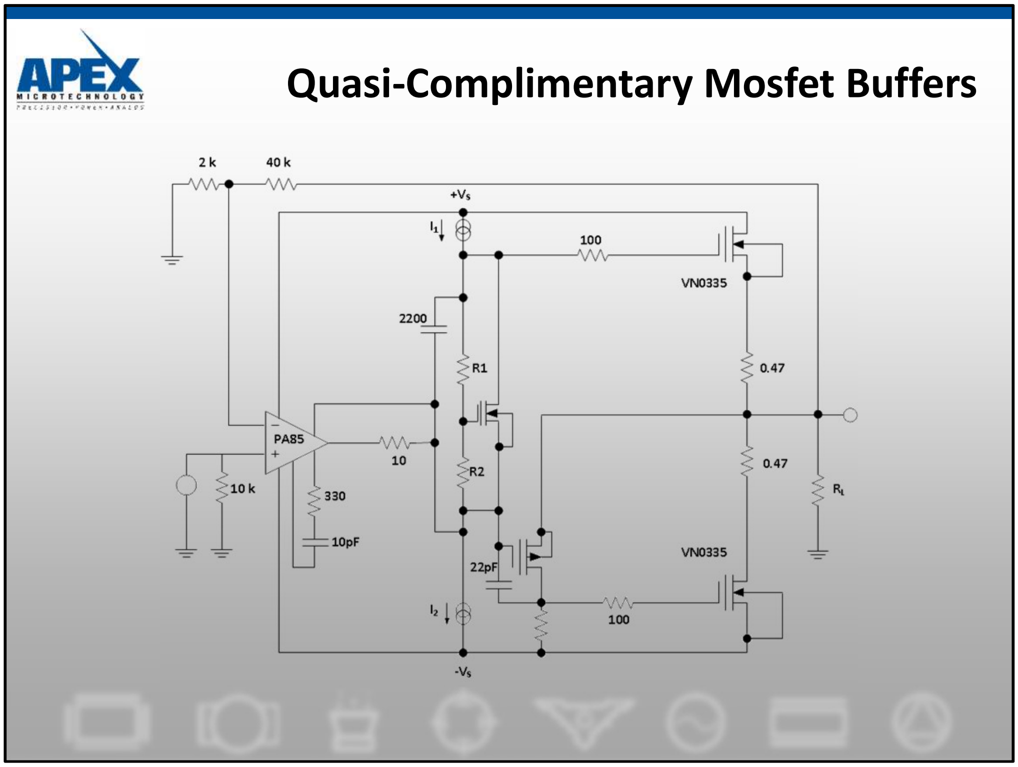


The class C circuit was able use a simplified version of this slide with no attempt to establish class A/B bias in the MOSFET output stage. In that circuit with no bias, the typical MOSFET threshold of 3V means the op amp must swing 6V during the crossover transition while the final output does not move. The additional circuitry used here will lower distortion and is increasingly important as frequency goes up. Distortion improvements better than an order of magnitude have been achieved.

As most power MOSFET data sheets provide little data on VGS variations at low currents over temperature, it facilitates the design process to have curve tracer data over the temperature range of interest. Design the VGS multiplier empirically. Current sources of 5mA and splitting the current equally between the resistors and the MOSFET area good starting points. Decreasing current in the MOSFET will increase the multiplier TC. Typical designs requiring low distortion will be set up to obtain 2mA or less bias in the output stage. The trade offs are more distortion with low current and danger of thermal runaway on the high end. Be absolutely sure to guardband your high end temperature. The circuit shown here is capable of distortion below .05% at 50KHz and is thermally stable (flat or negative TC of current in the output stage) over the range of -25°to 85°C.

Note that any multiplier voltage at all reduces distortion. Successful designs have even reduced the multiplier circuit to just a diode connected MOSFET. Do NOT use bipolar transistors or diodes for this biasing. Their TCs do not match those of the MOSFETs.

The 100Ω gate resistors prevent local output stage oscillations. It is important they be physically close to the MOSFETs. Ref. Use High-Voltage Op Amps to Drive Power MOSFETs, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.



Above 300V p-channel high power MOSFETs can be difficult to find. An alternative is to use a quasi-complementary connection on the negative side. Since the required gate drive voltage of the output device appears across RG, its value will set the maximum current through the p-channel MOSFET. Typical maximum gate drive requirements are 10V. This circuit has demonstrated a slew rate of 360V/µs. A second disadvantage of the quasi-complementary design is higher saturation voltage to the negative rail because two gate-source voltages are stacked between the rail and the output.

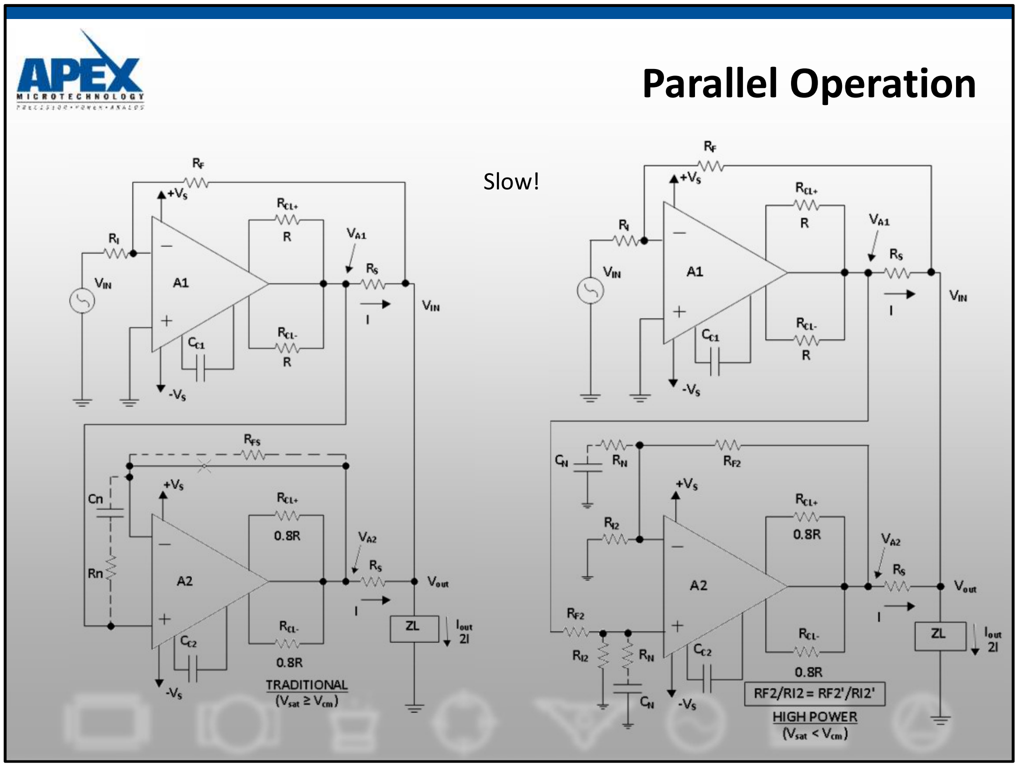
Connecting the op amp to the top side of the multiplier helps a little but both buffer design approaches can benefit from having the high voltage op amp operate on higher supply rails than the high power MOSFETs. This improves efficiency by allowing better saturation of the buffers.

Design criteria for the current sources, current limiters (not shown here) and multiplier are the same as with the complementary version. It is possible to omit one of the current sources in these circuits. However, this places an added heat burden on the high voltage op amp because the entire current of the remaining source must flow through it. When calculating this added dissipation, use the current and the total supply voltage. When both current sources are used the op amp need only make up the difference between them.

Ref. Use High-Voltage Op Amps to Drive Power MOSFETs, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.

Parallel Op Amps

- Primary Op Amp in any configuration
- Follower Op Amp – unity gain buffer
- Use sharing resistors to reduce the effects of output difference errors (offset, phase lag, etc)



Occasionally it is desired to extend the SOA of a power op amp or provide higher currents to a load than the amplifier is capable of delivering on its own. Sometimes it is more cost effective to use power op amps in parallel rather than to select a larger power op amp.

The parallel power op amp circuit will consist of a primary amplifier, A1, which sets the Vout/Vin gain and follower amplifiers, A2 et al, which act as unity gain followers from the primary amplifier. For simplicity we will review the case of two power op amps in parallel.

We will need to consider the following key areas when paralleling power op amps:

1) Input offset voltage
2) Slew rate
3) Phase compensation
4) Current limit resistors

If we attempt to hook the outputs of two power op amps directly together the difference in input offset voltages, divided by theoretically zero ohms (a connecting wire), will cause huge circulating currents between the amplifiers, which will lead to rapid destruction. To minimize circulating currents we will need to add ballast resistors, Rs, as shown. The worst case circulating currents now are Icirc = Vos/2Rs. To minimize circulating currents we want Rs to be as large as possible. However, large values of Rs will add an additional voltage drop from the power supply rails and thereby reduce output voltage swing. Large values of Rs will also result in higher power dissipations. A rule of thumb compromise is to set Rs for circulating currents of about 1% of the maximum output current from each amplifier, .01I in our example.

Notice the particular arrangement of the primary and follower amplifiers. VA1 = IRs

+ Vout. However the point of feedback for A1 is at Vout causing A1 to control the gain for Vout/Vin. VA1 then becomes the input to A2. VA2 is then Vout + IRs. But Vout = VA1 – IRs. So each amplifier, A1 and A2, put out the same voltage across Rs and ZL and currents are thereby added to force 2I through the load with each amplifier providing one-half of the total.

The slew rates of A1 and A2 must be selected to be the same or A1 must be compensated for a lower slew rate. If A1 slews faster than A2, large circulating currents will result since A1 could be close to +Vs while A2 is still at zero output or worse near –Vs. Cc1 and Cc2 must then be selected to be the same or Cc1 greater than Cc2. Even with these steps for slew rate matching it is recommended to control the slew rate of Vin such that the amplifiers are not commanded to slew any faster than 50% – 75% of the selected slew rates. This is because, even with identical compensation, no two amplifiers will have identical slew rates.

If it is decided to have A2 not compensated for unity gain, to utilize a higher slew rate, use Noise Gain Compensation, shown by the dashed RFS and Rn, Cn combination, to compensate the amplifier for AC small signal stability.

Current limit resistors, Rcl+ and Rcl- for A2 should be 20% lower in value than currrent limit resistors for A1. This is to equalize SOA stresses during a fault condition. With the primary amplifier, A1, going into current limit first it will lower its output voltage thereby commanding A2 to do the same for equal sharing of stresses during a current limit induced condition.

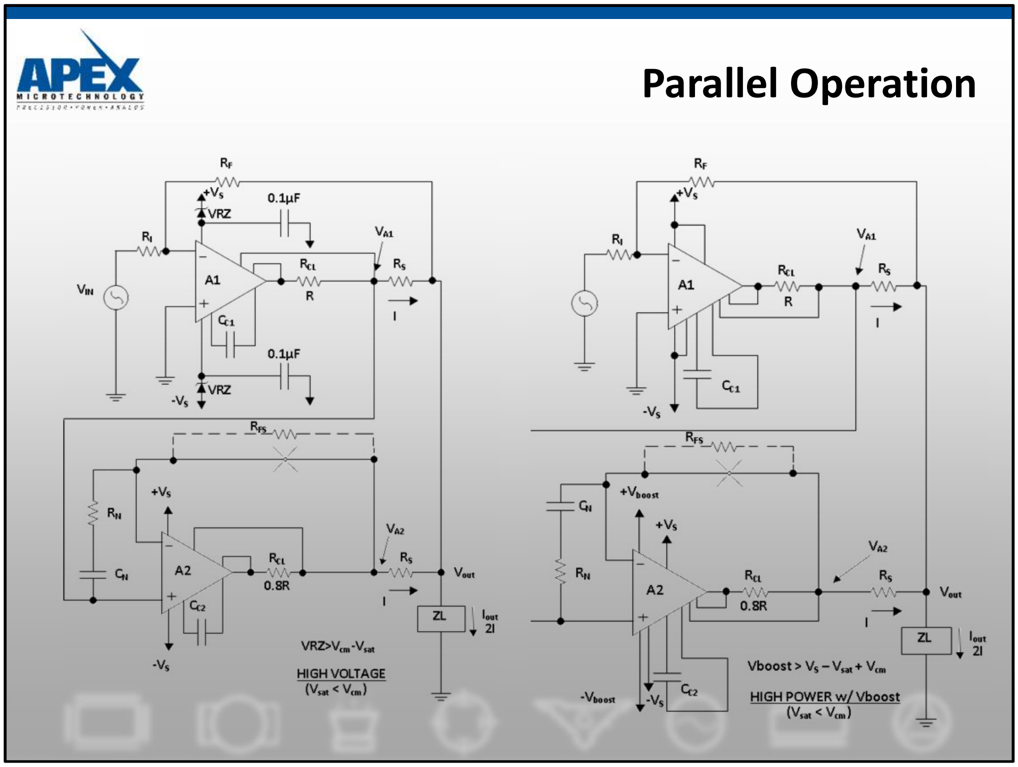
TRADITIONAL (Vsat ≥Vcm): This parallel configuration is for op amps whose saturation voltage is greater than or equal to their common mode voltage (Vsat Vcm). For example, a PA10 has a common mode voltage specification of +/- Vs-5 and a saturation voltage of +/- Vs -5. For the PA10 the output saturation voltage (5V) is equal to the common mode voltage (5V from either rail). We will not have any common mode voltage violation then if we drive the output of A1 into saturation as we will still be in compliance with the input common mode voltage specification for A2.

HIGH POWER (Vsat < Vcm): This parallel configuration is for amplifiers whose currents are greater than 200mA and whose saturation voltage is less than their common mode voltage (Vsat < Vcm).

For example, a PA02 has a common mode voltage specification of +/- Vs -6 and a saturation voltage of +/- Vs -2. For the PA02 the output saturation voltage (2V) is less than the common mode voltage (6V from either rail). If we drive the output of A1 directly into A2 in a unity gain voltage follower configuration we will have a common mode voltage violation.

The only way around this is to use a matched resistor network where the ratio of RF2/RI2 = RF2'/RI2'. The absolute value of each resistor is not as important as accurate ratio matching with temperature. If A1 and A2 are compensatible amplifiers and unity gain compensation is not desired, to use faster slew rates, then A1 can use noise gain compensation to guarantee AC small signal stability. Rn and Cn are our traditional Noise Gain Compensation components. Rn' and Cn' are essential to guarantee a flat Vout/Vin frequency response until we run out of loop gain.

Ref. AN26



All our previous “GENERAL COMMENTS” on the use of parallel power op amp circuits still apply to these configurations. Additional specific comments on each follows.

HIGH VOLTAGE (Vsat < Vcm):

This parallel configuration is for amplifiers whose currents are less than 200mA and whose saturation voltage is less their common mode voltage (Vsat < Vcm). In the APEX amplifier line this will almost always be high voltage (+/–Vs > 75V).

For example a PA85 has a common mode voltage of +/–Vs–12 and a saturation voltage of +/–Vs– 5.5 at light loads. For the PA85 the output saturation voltage (5.5V) is less than the common mode voltage (12V from either rail). If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we lower the supply voltage of A1 by about 6.5V, which we can do easily with a zener diode in each supply line of A1. For 200mA output current plus 25mA quiescent current would require at least a 2W, 6.8V zener in each supply rail. The obvious loss with this technique is output voltage swing from the rail, now limited to Vsat of 5.5 Volts plus VRZ drop of 6.8 volts for a total of 12.3V, at light loads.

HIGH POWER w/Vboost(Vsat < Vcm):

This parallel configuration is for amplifiers such as the PA04 or PA05 that are high output current and whose saturation voltage is less than their common mode voltage (Vsat < Vcm.)

For example a PA05 has a common mode voltage of +/–Vs –8 and a saturation voltage of +/–Vs -5.0 at light load. If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we utilize the Vboost function of these power op amps on A2 to run the front end of A2 at a supply voltage which is at least 3 volts above its output voltage supply (Vs). This Vboost supply need only supply quiescent current for the device and can be generated by a switching floating regulator. A less advantageous approach, which would reduce output voltage swing, is to utilize a zener diode in the Vboost supply of A1, similar to the “HIGH VOLTAGE(Vsat < Vcm)” example above.

Ref. AN26

Watch the Follower Phase Shift

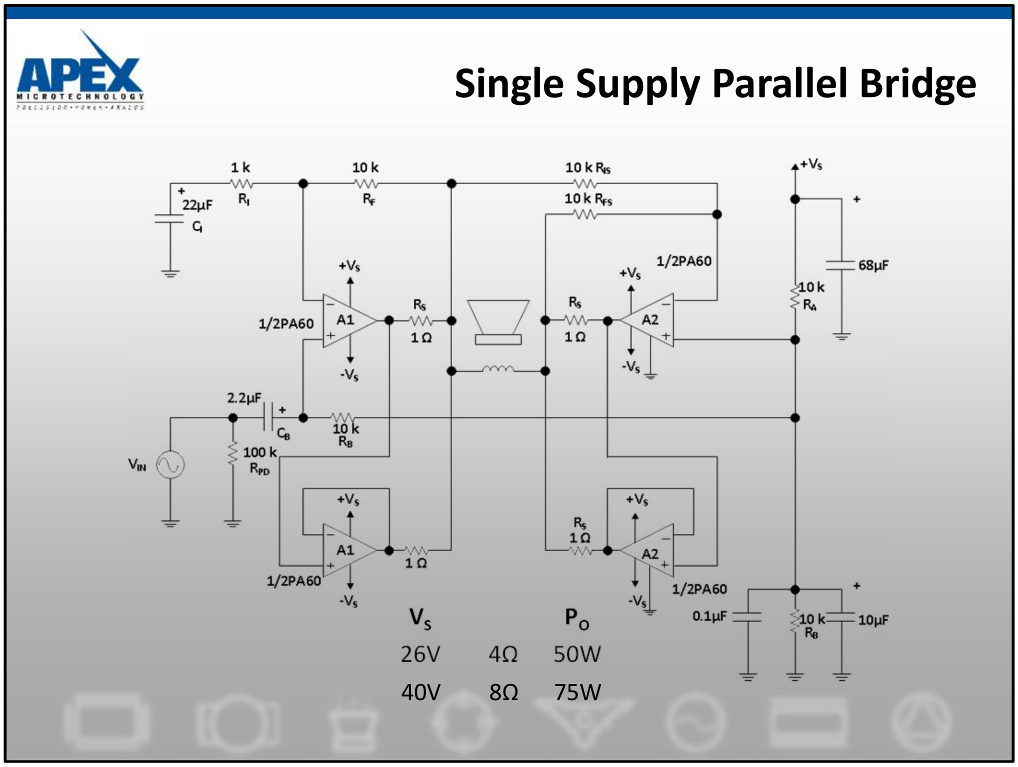
- PA85 Power Response Curve = 500KHz@400Vp-p
- Power Design suggests 86KHz for accuracy
- Power Design tells us phase shift is 7°@ 87KHz
- Sin(7°) = 0.122 * 200Vpk = 24.3V
- This voltage appears across the two Rs resistors

The power response graph says you can get to those points, however, you will usually need to increase the drive amplitude and you will probably just start seeing distortion. Another way to put it: these curves demand no loop gain and circuit accuracy is a function of the op amp rather than feedback components on the sloping portion of the power response curve (AC response limits rather than voltage saturation). The amplitude and distortion voltage errors of the follower appear across the two sharing resistors.

Phase shift grows as loop gain decreases. In the primary of the parallel circuit this does no harm locally because the follower input includes the shift. However shift in the follower produces voltage applied across the sum of the two ballast resistors where circulating current becomes a concern.

The Cload sheet of Power Design will calculate closed loop phase shift. The sine of this angle times peak voltage yields the error we are looking for.

Parallel power op amps is <u>not</u> a high speed technique.



This application utilizes two power op amp circuit tricks—single supply bridge mode to increase output peak-to-peak voltage and parallel power op amps to increase output current.

The PA60 is optimized for single supply operation with its wide input common mode voltage range and low saturation voltage. The parallel combination provides a dual advantage in that we can deliver higher output currents as well as reduce the output saturation voltage since each op amp need only supply one-half the total load current.

AC coupling of Vin provides level shifting of the input signal to swing symmetrically about 1/2Vs. AC coupling through CI ensures the maximum DC offset across the load is only 20mV. RB provides a +input DC bias path for the front end of the primary amplifier half of A1. This is due to the type of output power stage inside the monolithic PA60. A2 is configured as a traditional inverting gain amplifier for single supply bridge mode and uses one half of itself for providing extra current as a follower amplifier in the parallel configuration.

With the PA60 at $5US (1000) this is about 13 cents per watt. PA74 and PA76 offer hermetic packages at higher cost. Just imagine what you could do with PA03s in this circuit. Let’s break the KW barrier!

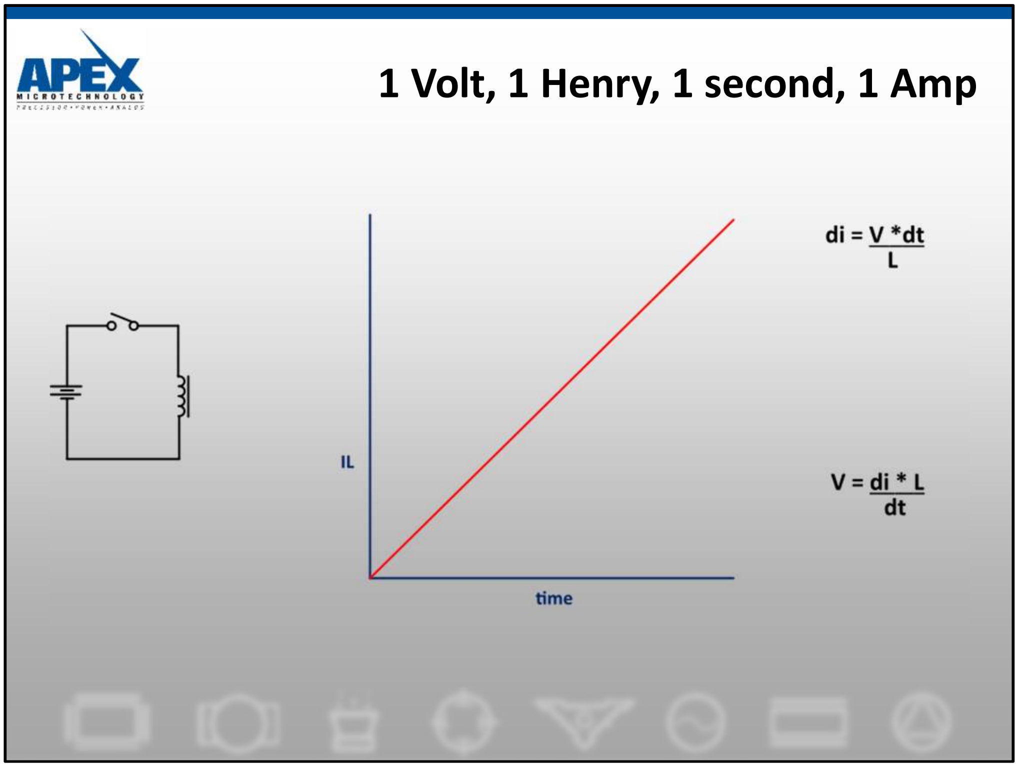
Ref. AN20

Controlling Output Current

- Removes Zload from the Iout equation
- Adds Zload to the Vout equation

- Charge Rate control
  - Batteries, capacitor plate forming power supply active loads, CD welder
- Magnetic field intensity
  - Bearings, deflection, MRI, torque, linear or angular displacement

Controlling current rather than voltage is much more common with power op amps than will small signal op amps. The current control world brings interesting applications plus some new techniques with their own equations and special points to watch.



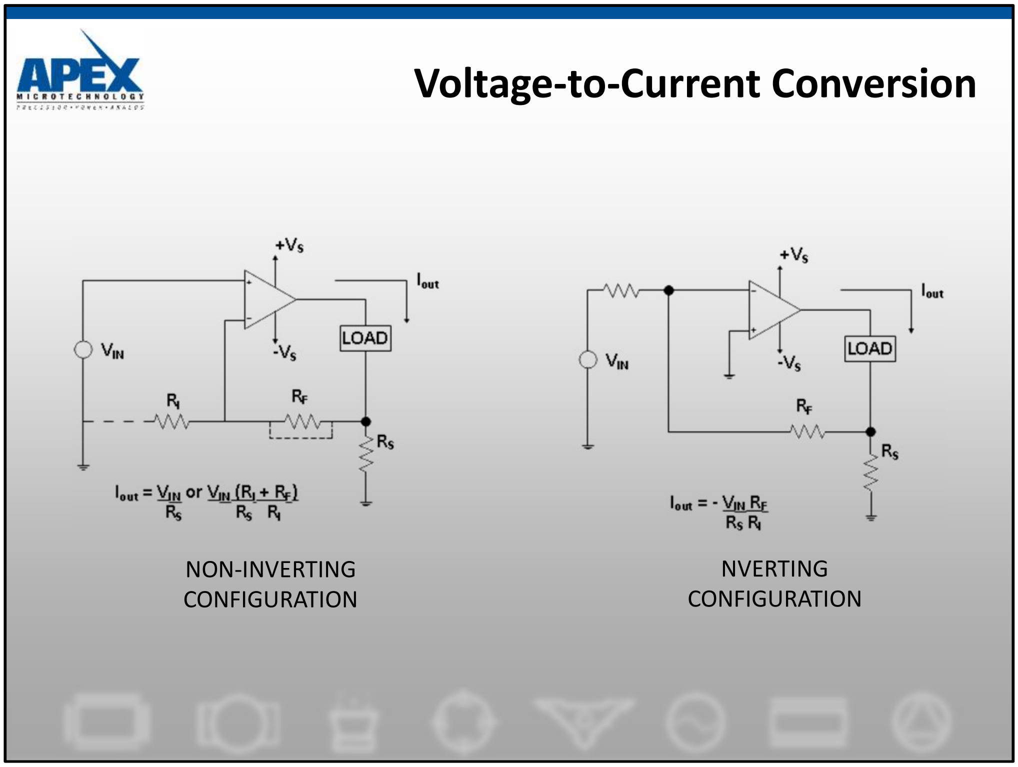
OK, so you've seen this before. It is central to current control.

Changing current a lot, in a big inductor, in a hurry, takes lots of volts.

The corollary:

Stopping a big current, in a big inductor, in a hurry, generates lots of volts.

It may require more power than first glance says; opening a current carrying line may release all the stored energy in the form of fire

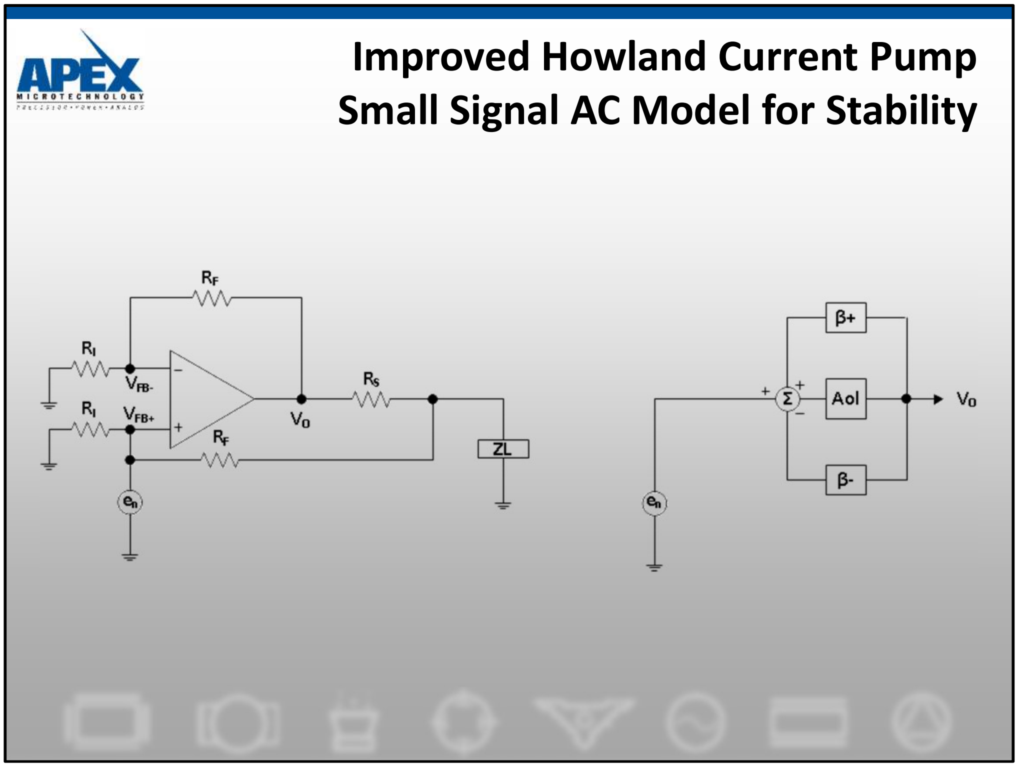


Two generic examples of voltage-to-current conversion for a floating load are shown here. The floating load circuit provides the best possible performance of any of the current output circuits with the tradeoff that the load must float.

In the basic non-inverting circuit Ri and Rf don’t exist. Load current develops a proportional voltage in Rs which is fed back for comparison to applied input. As long as voltage across Rs is lower than the input voltage, the output voltage increases. In other words the op amp impresses the input voltage on the sense resistor. Adding the resistors allows increasing the transfer function. It is also common to have Rf without Ri providing an RC stabilizing network a reasonable impedance for its AC feedback signal.

The inverting circuit works in the same manner other than polarity but does have the advantage of being able scale the transfer function up or down. This mean it is possible to have less voltage on the sense resistor than the input signal has.

Ref. AN13



$$\beta+ = \frac{Vfb}{Vo} \qquad Vo = Aol\ (en + Vo\ \beta +\ -Vo\beta -$$

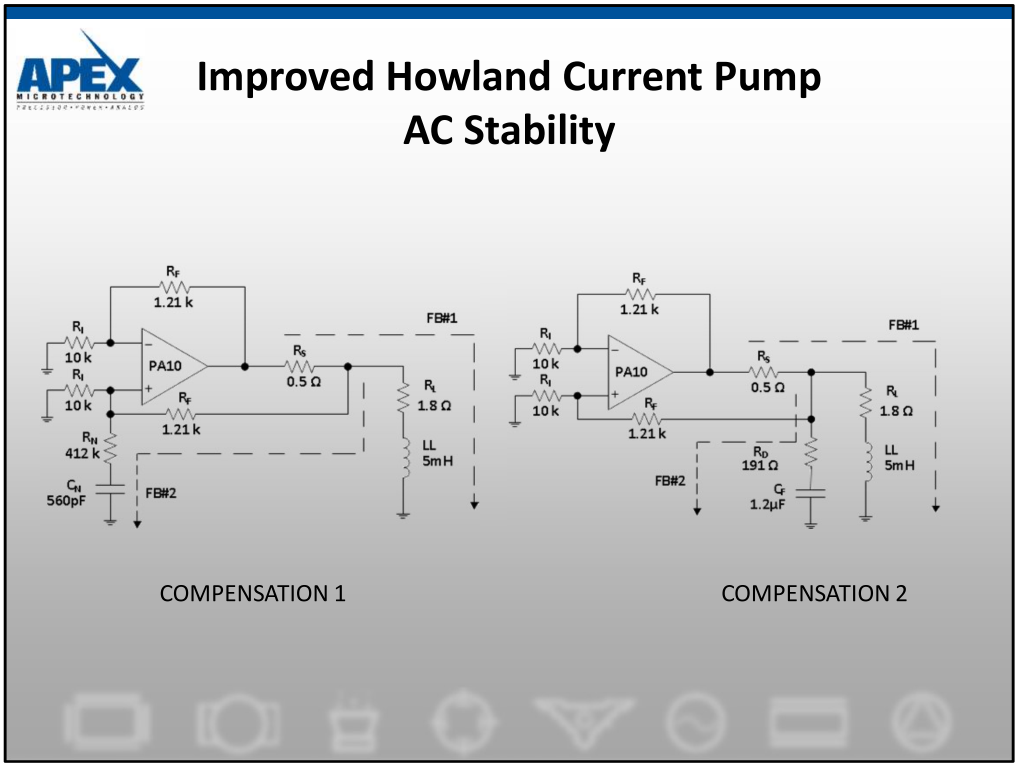
$$\beta- = \frac{Ri}{Rf} \qquad Vo\ - Aol\ Vo\ \beta +\ +Aol\ Vo\ \beta- = en\ Aol$$

$$\beta+ = \frac{[ZL||(Rf+Ri)]Ri}{[Rs+ZL||(Rf\qquad)][Rf+Ri]} \qquad \frac{Vo}{en} = \frac{1}{\beta--\beta+}$$

$$\beta =\ \beta - -\beta + \qquad \beta = B - -\beta +$$

The figure on the left above shows a typical Improved Howland Current Pump circuit. Notice the additional en voltage source on the non-inverting input node of the op amp. For AC small signal stability analysis we do not know where the input signal can be injected. We choose to inject the AC input signal at the +input since this will result in the worst case stability situation. 1/β plots then will be a representation of Vo/en .

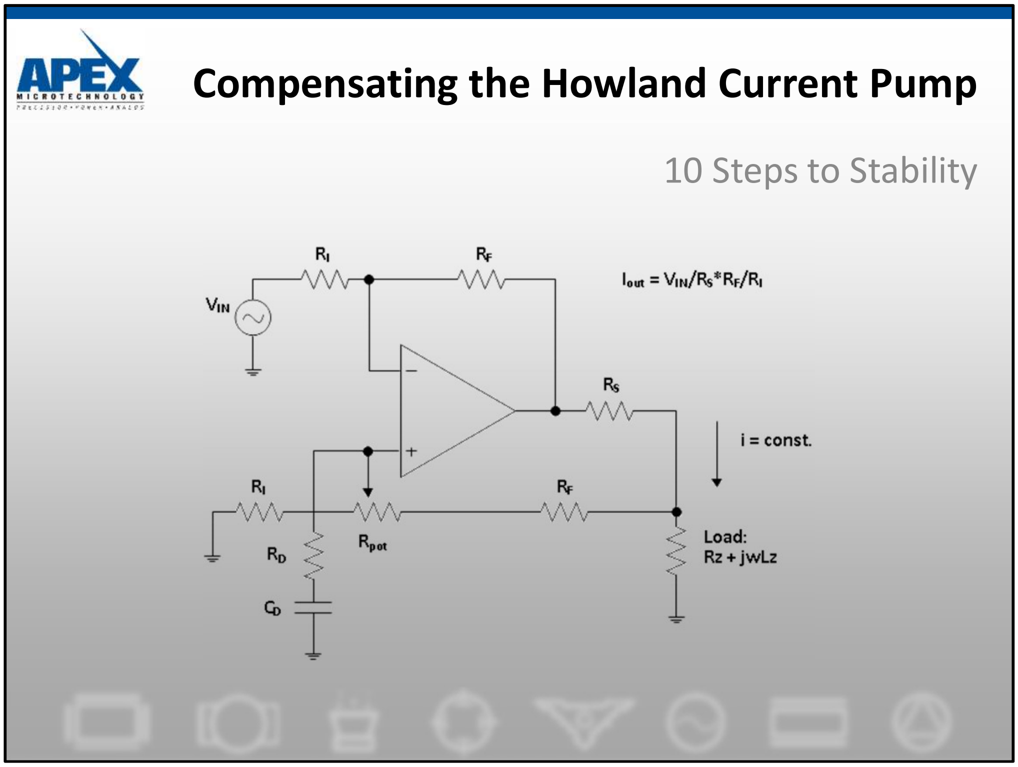
The figure on the right above is the equivalent control system block diagram from which we derive the powerful equation for β which will enable us to stabilize the Improved Howland Current Pump with the stability analysis techniques we have previously covered.



For any engineering problem there is usually more than one solution. This is true when reviewing AC stability compensation for the Improved Howland Current Pump and proposing a solution, or two!

Shown above are two compensation techniques, Compensation 1 and Compensation 2. FB#1 for both compensation techniques will be the same. Similar to V—I circuits for floating loads this β + feedback path which will cause a zero in the net 1/β plot which will result in 40dB per decade rate of closure and instability without additional compensation provided by FB#2.

FB#2 has the function of reducing the voltage fed back to the +input at higher frequencies and thereby forming a pole in the net 1/β plot which guarantees stability and a 20dB per decade rate of closure.



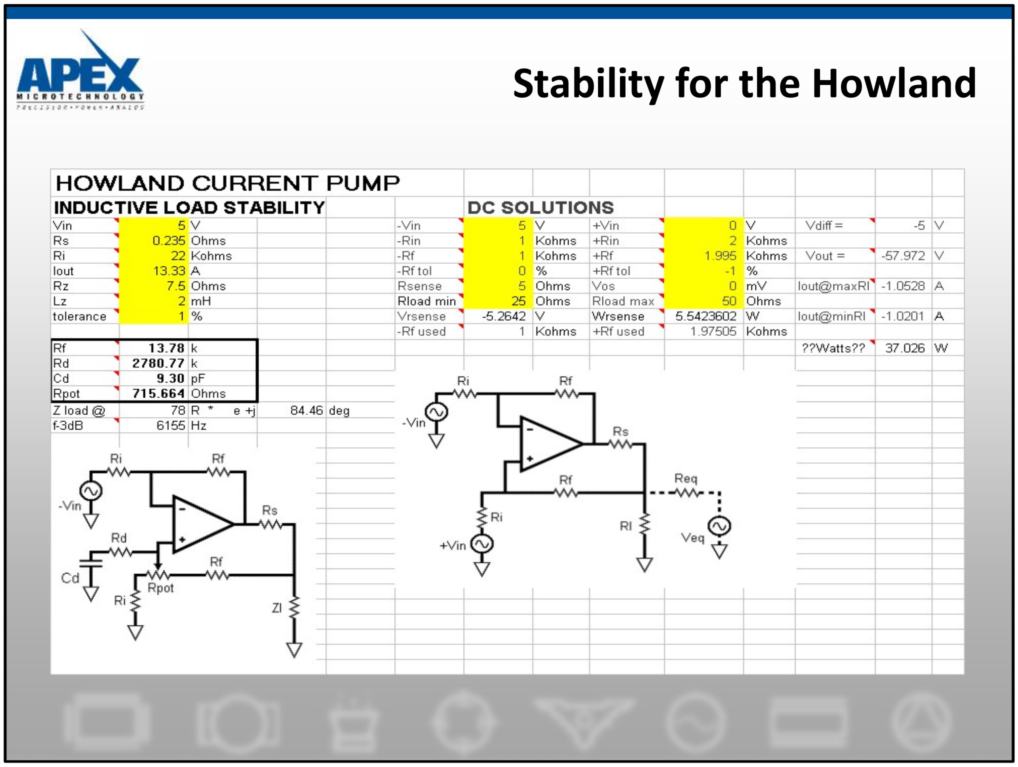
Inductive loads cause stability trouble with current source applications. Because current lags voltage in an inductor, current feedback is delayed and thus decreases the phase margin of the current amplifier. Consequently, ringing or oscillation occurs. This following procedure shows a proper compensation technique for inductive loads.

After choosing Ri, select an appropriate current sense resistor Rs. The voltage available to your load is the power supply voltage minus the voltage drop across Rs. Power dissipation of Rs calculates to Prs = Imax2 * Rs. Continue to calculate the following component values: Finally, adjust Rd and Cd values to standard values and insert a trim pot between the feedback resistor and the input resistor of the positive feedback network:

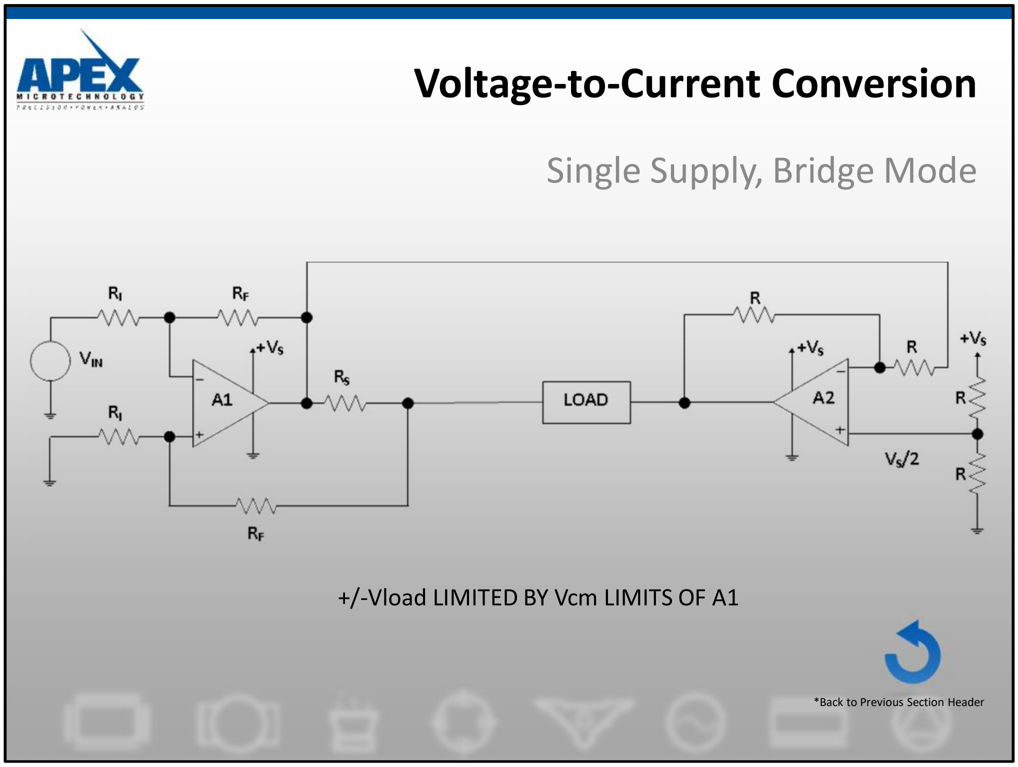
Rpot = .02*ΔR[%]*(Ri+Rf)1

The potentiometer compensates the resistance mismatch of the Rf/Ri network. Trim for maximum output impedance of the current source by observing the minimum output current variation at different load levels and maximum output current.

[1] ΔR[%]: resistor tolerance in percent



Again, Power Design eases the design burden. Cells to describe the circuit, both for stability analysis and error budget analysis. There are many other pieces of data lying outside this slide if you like to dig around. Application Note 13, Voltage to Current Conversion is the reference.



This configuration combines two previously covered techniques: single supply bridge configuration and V to I conversion using the improved Howland current pump. A2 is biased at the familiar Vs/2 mid-supply point. Rf and Ri must be ratioed such that during min and max output voltage swings of A1 the common mode input range of A1 is not violated. This imposes a max output voltage swing limit across the load. Iout through the load is given by: Iout=(Vin*Rf)/(Rs*Ri). Rs is selected as large as possible to give as much voltage feedback as possible with acceptable power dissipation. Vin is set to its most positive value. Vcm for A1 (common mode input voltage for A1) is set to comply with data sheet specifications. Usually this will be about Vs-6, which means Vcm must be at least 6.0 volts. Ri is selected to cause about .5 mA to flow through it when Vin is at its most negative voltage. This then dictates the value for Rf which is selected to complete the Vin to Iout equation given above. Vcm should then be rechecked for input common mode compliance at positive and negative swing out of A1. Recall that Vout (A2)=Vs-Vout(A1) for the given circuit. Vout (A1) must be at least Vcm to keep A1 operating in the linear region. Then Vload=(Vs-Vcm)-Vcm. In other words Vload=Vout(A2)-Vout(A1). Therefore, the maximum output peak voltage across the load for this configuration is Vs-(2*Vcm).

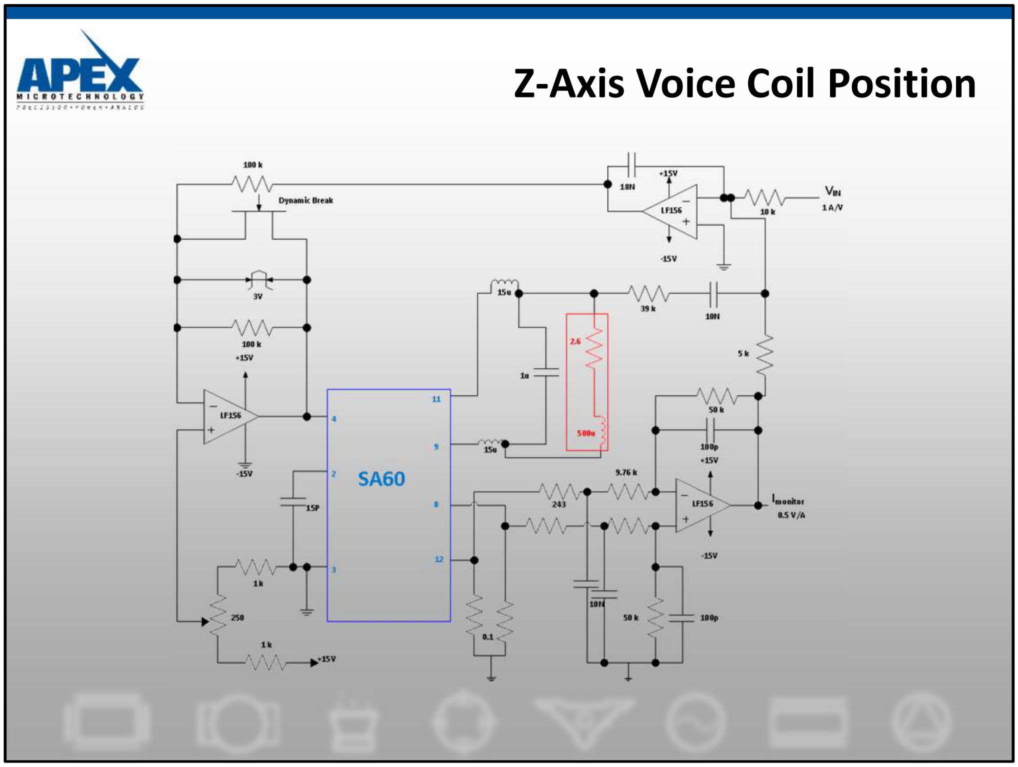
MOTION CONTROL

Motion Control

Position, Torque or Speed

- Brush
- Micro-steppers
- Linear (voice coil)
- Multi-phase AC
- Galvanometers

One of the largest applications for high power op amps is in motion control. High current high power op amps can be used for all components of motion control including speed control, position control and torque control. Their ease of use, rapid design ability and rugged hybrid construction lead to cost effective motion control systems.



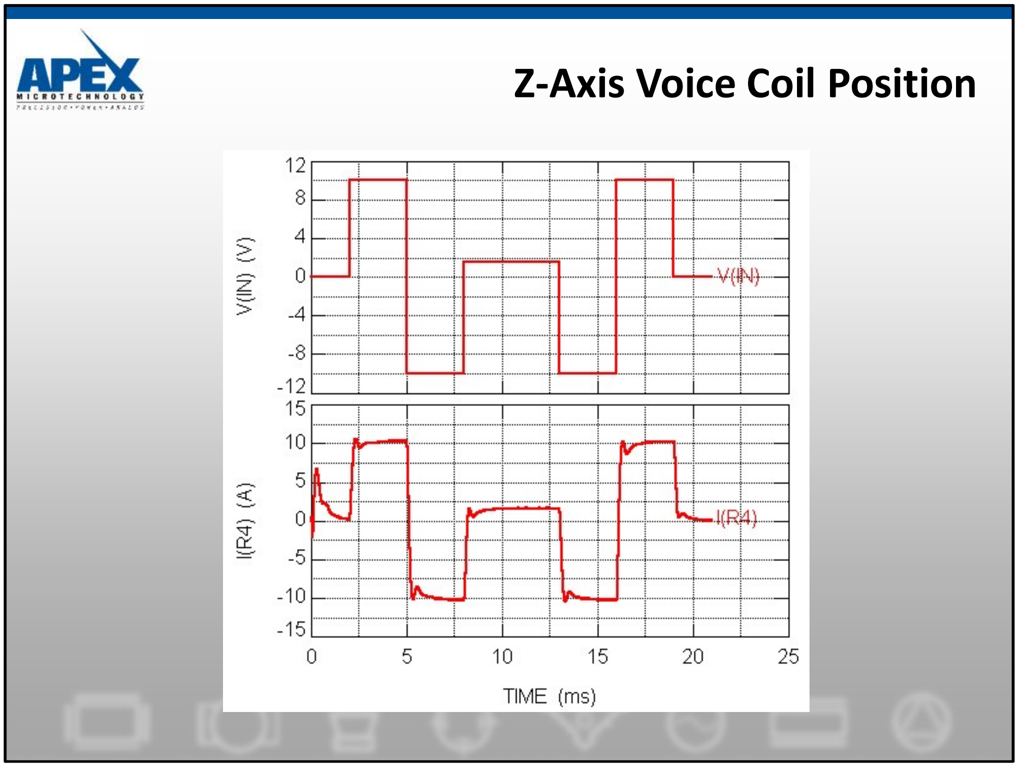
Slower versions of this machine used a PA12 linear op amp for Z-axis control. Even though currents were lower and motor impedance was higher, an exotic custom heat sink had to be designed to fit the small physical location of the amplifier. It was clear that this generation of the machine required higher efficiency in the drive circuit. The SA60 provides this and being programmed to switch at about 220KHz, it provides adequate bandwidth for the high speed servo loop.

Current sense resistors of 0.1Ω develop 1V at the 10A current peaks giving very good resolution and accuracy for the differential current monitor which provides the ½V/A feedback signal. Both poles of the differential amplifier were placed at roughly ¼ the switching frequency. This amplifier needs to be the fastest responding block of the system.

The pure integrator now reacts to any magnitude difference between feedback and input command signals. The 18nF makes the integrator significantly slower than the current monitor. The 39K/10nF network becomes the dominate feedback path just before the V-to-I phase shift of of the motor inductance brings on stability problems.

With the dynamic brake signal low, the last amplifier inverts the drive signal to the SA60 and limits drive amplitude to just greater than the peaks of the triangular ramp. When the dynamic brake is applied, this amplifier becomes a unity gain buffer for a DC level adjusted to insure the SA60 output is a low impedance, near zero voltage.

Even though the nominal motor inductance was adequate to keep ripple current in check, this inductance varied with position of the motor and a filter was used clean up the circuit.



After power up settling, the first 3msec pulse accelerates the motor toward the work piece; the second 3msec pulse decelerates the motor; a constant pressure is held for 60msec (time was compressed in this plot); the last two pulses move the motor back to home position; and at t=150msec the cycle is repeated.

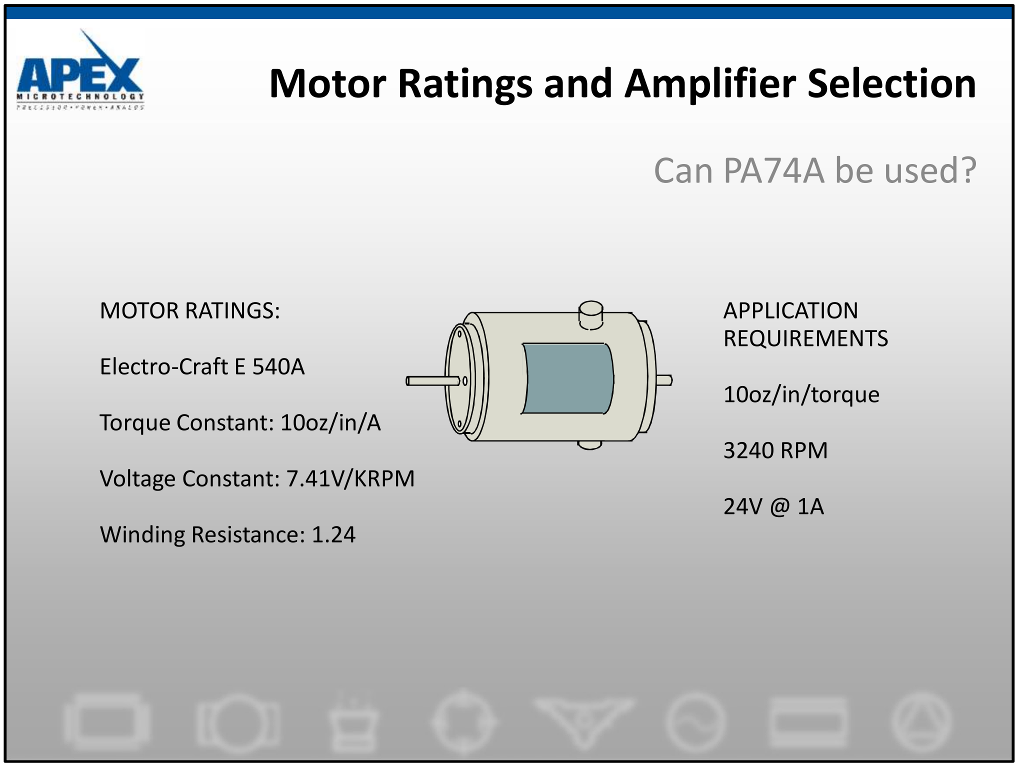
Here is a method to calculate a heatsink for this type application. First, assume a reasonable case temperature for the amplifier. We will pick 60°C. Application Note 11 tells us the temperature of a heatsink with any reasonable mass will change very little during the period of 150msec, so knowing average power dissipation over the cycle will establish a thermal rating.

Use Power Design to find the power levels for each of the three output current levels by entering a heatsink rating of .01 and adjusting ambient temperature to obtain a 60°case temperature. Enter a minimum frequency less than 60Hz to insure power is calculated for steady state. Here are the results:

I out	Ta	Power	Tj	msec	W*msec
.01	60	11.3	61	78	881
1.5	59	12.5	61	60	750
10	52	77.3	103	12	928
			Total = 2559		Divide by 150 msec = 17.1W avg.

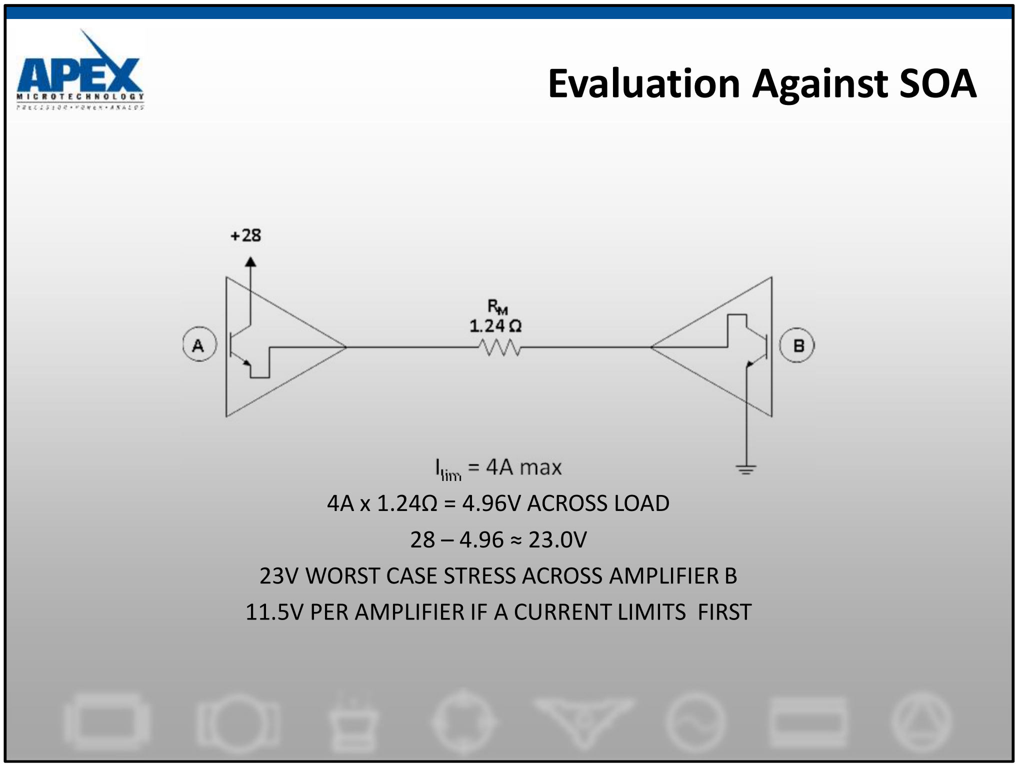
If ambient temperature is 25°C, a 2°C/W heatsink will allow a case temperature rise of about 34°, meeting the assumed 60°operating point.

While it was not shown in the schematic, it is imperative that a heatsink mounted over-temperature shutdown circuit be installed and set for less than 90°C. The over-temp limit was found in a similar manner as the previous



Will the PA74 do? It is rated 2.5A peak. This application only needs 1A normally.

Ref. AN24



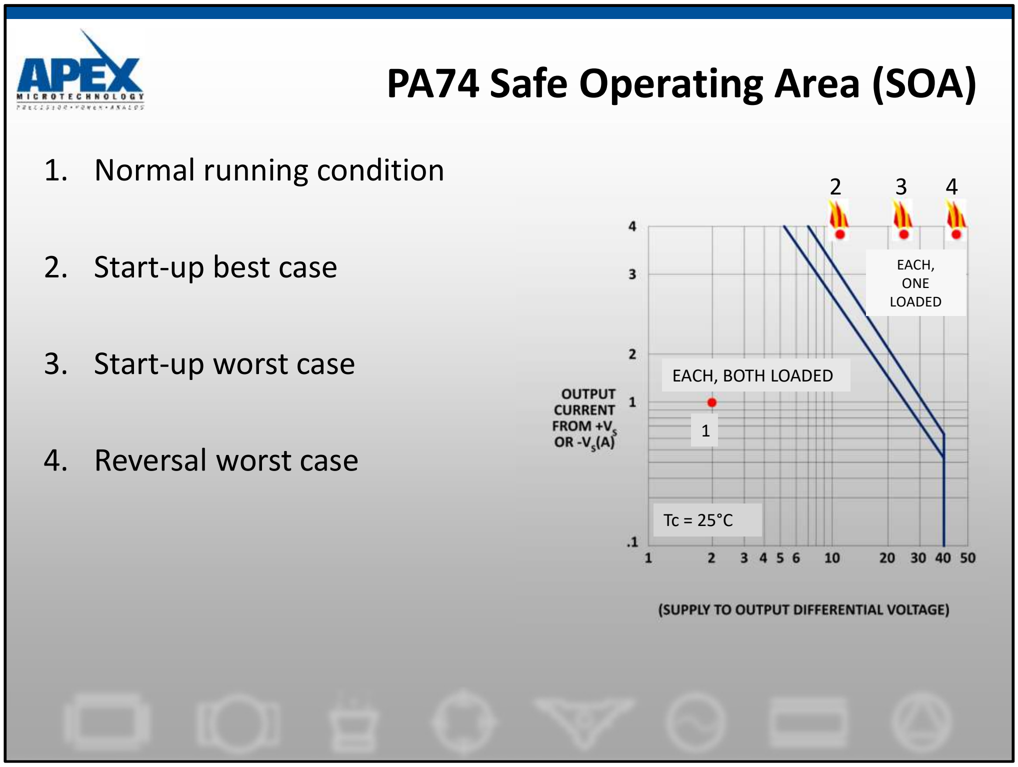
The above model provides us with a tool for analysis to examine worst case SOA stresses. This represents the condition for motor start-up or stall (not as demanding as instant motor reversal which is easily avoidable).

For this condition the motor is modeled as a 1.24 ohm resistance at stall. Assuming the PA74 current limit is at 4A results in a 4.96V drop across the load. Since it is not known which amplifier half will current limit first we must assume the worst case. If op amp B limits first all 23V of voltage stress will occur across it.

If op amp A were to current limit first or both op amp A and op amp B current limit at the same level then the voltage stresses would be equal at 11.5V across each.

For our SOA evaluation of the PA74 we will need to assume a 4A, 23V stress. In amplifiers with externally adjustable current limit we can guarantee op amp A current limits first by setting op amp B current limit 20% higher than that of op amp A and thereby equalizing voltage stresses across each op amp.

Ref. AN20,AN24



Plotted on the PA74 SOA graph are the four possible operating conditions for the PA74 when used with the Electro-Craft E540.

Point 1 is normal running condition which is well within the SOA boundaries.

Point 2 is the best case start-up condition where both op amp A and op amp B current limit at the same level or op amp A current limits first.

Point 3 is the worst case start-up condition where op amp B current limits first and bears the total voltage stress.

Point 4 is a worst case motor reversal condition with op amp B current limiting first.

It is readily apparent that with the PA74's non-adjustable internal current limit of 4A there is not sufficient SOA for driving this motor in start-up or stall conditions. Our alternatives will be either a complex soft-start circuit or power op amps with larger SOA.

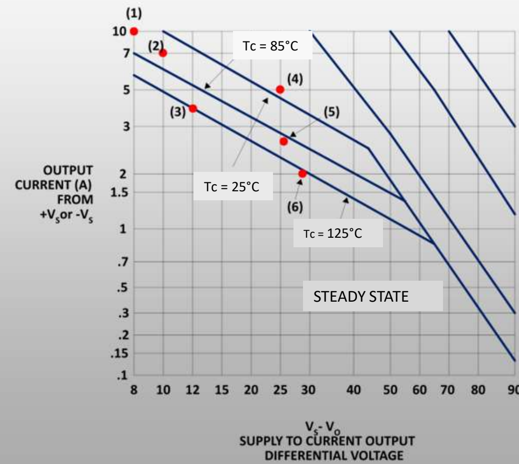
Ref. AN20,AN24

Protection Alternatives

PA61 – Improved SOA + Current Limit Adjustment

START-UP		
Ium	V_S-V_O	
10A	8V	(1)
7A	10V	(2)
4A	12V	(3)

REVERSAL		
Ium	V_S-V_O	
5A	25V	(1)
2.5A	26V	(2)
2A	27V	(3)

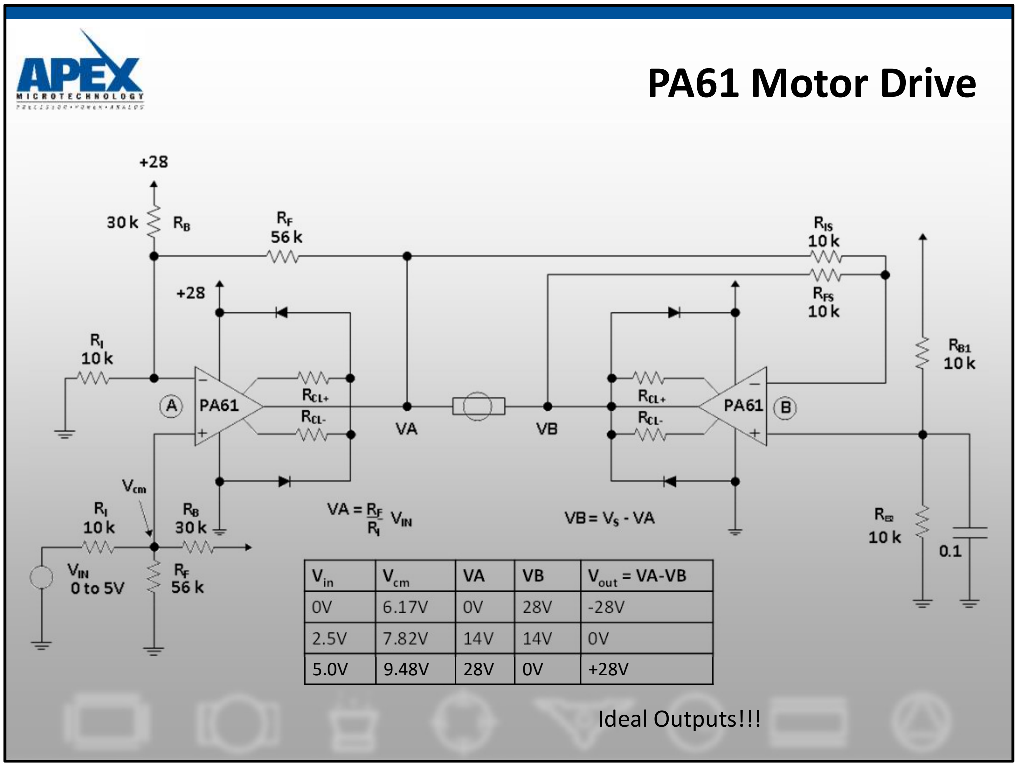


Often the only solution to the conflicting requirement of protection along with reasonable motor acceleration is simply an amplifier with a larger SOA. Not only does the PA61 provide a better SOA fit but the programmable current limit provides additional flexibility in meeting SOA requirements.

Points 1 thru 6 above on the PA61 SOA plot show a variety of operating choices depending upon what start-up current is desired, whether motor reversals are a possibility, and what heatsinking is available referenced to op amp case temperature. The following handy formulae provide a quick way for estimating these points given a properly designed bridge circuit.

START-UP: Vs– Vo(each op amp) = Vs - (Ilimit * Motor resistance)/2
REVERSAL: Vs – Vo (each op amp) = 2 * Vs - (Ilimit * Motor resistance)/2
Where: Vs = total supply voltage.

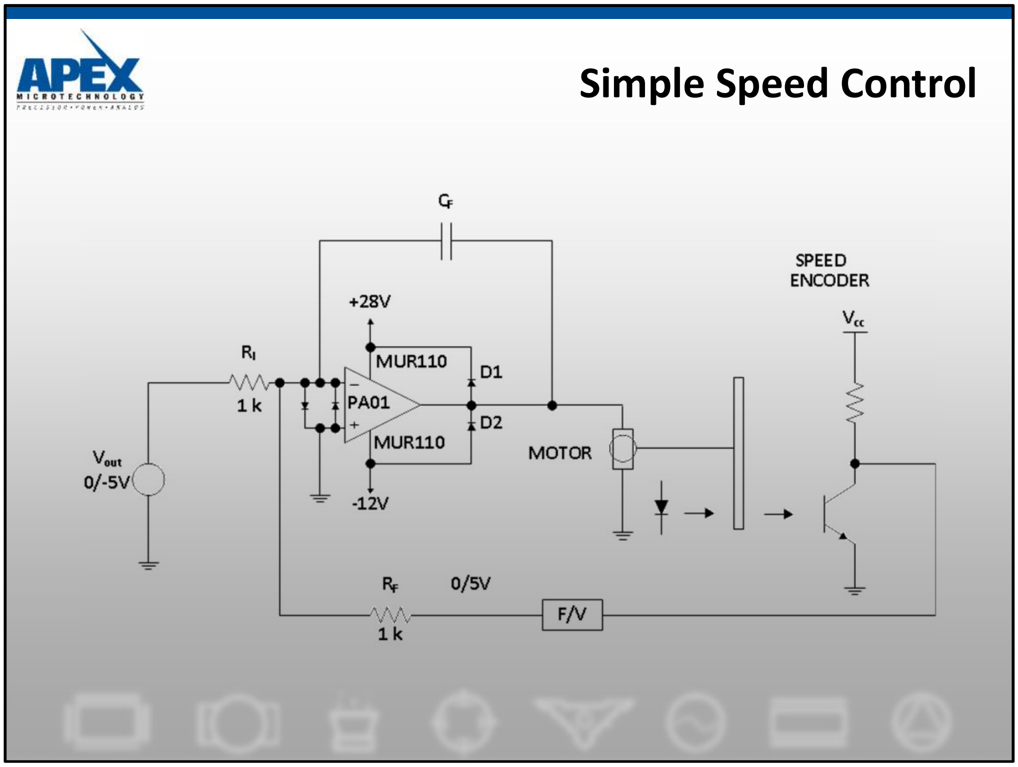
If using a single amplifier rather than a bridge, delete the “/2” term. The reversal formula makes 2 assumptions: Prior to reversal, output voltage was saturated all the way to the rail and motor back EMF = Vs. This may not be true by virtue of input signal level, and cannot be true by virtue of the output voltage swing spec of the amplifier (saturation limit) and plus it requires a zero ohm motor. Despite all this it’s a good first order approximation.



V_{in}	V_{cm}	VA	VB	V_{out} = VA-VB
0V	6.17V	0V	28V	-28V
2.5V	7.82V	14V	14V	0V
5.0V	9.48V	28V	0V	+28V

Our first alternate drive circuit for controlling the Electro-Craft motor utilizes a bridge of PA61 class “C” power op amps. Class “C” amplifiers are usually less expensive than similar class “AB” devices. While our PA61 implementation does require more components, than would our original PA21 circuit, it has the SOA to withstand start-up and even reversal conditions. Note that the PA61 has enough voltage range to handle this motor with a single amplifier. If the 28V supply is already part of the system, this may not be a good economic choice. PA73 is a 5A class “C” amplifier which would be a good candidate if high speed mechanical response is not of prime concern.

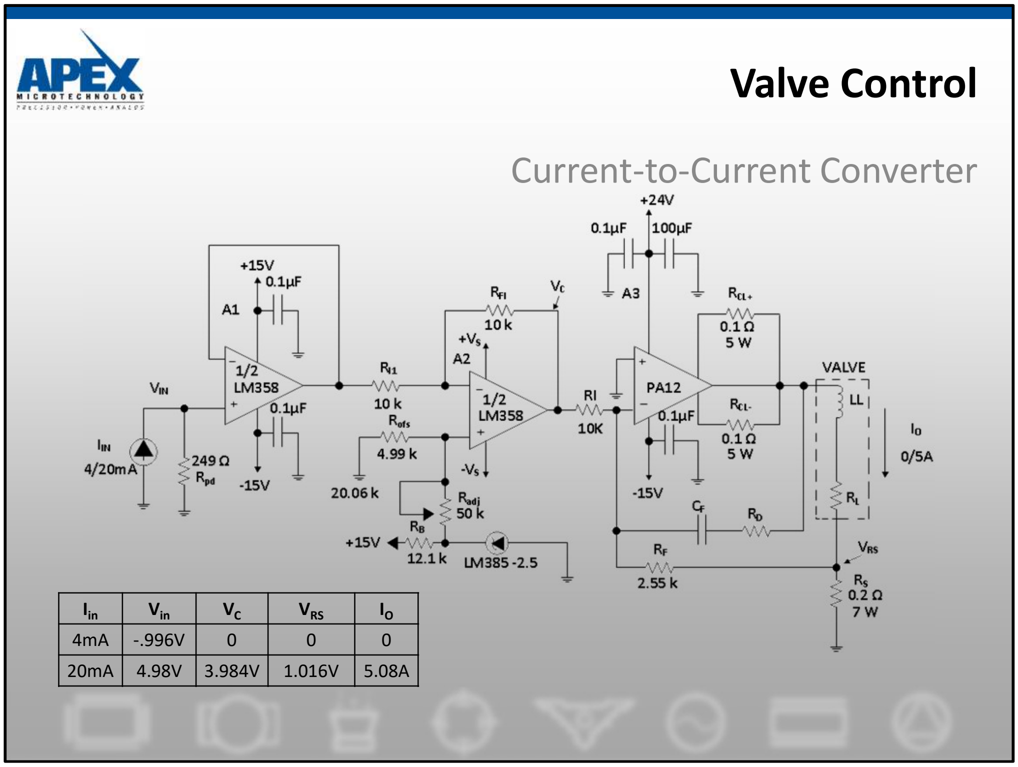
Amplifier A uses our Single Supply Non-Inverting Configuration seen previously to meet the common mode scaling requirements of the PA61. Gain scaling with this arrangement is set to try to drive the amplifier into saturation trying to achieve 0V or +28V out of the amplifier. This scaling needs to be cut back according to the saturation voltage of the specific amplifier at the specific output current level to be used. The specification is labeled Voltage Swing in the data sheet. This voltage is lost twice in a bridge circuit, once for each amplifier.



In speed control circuits the usual approach taken is to integrate the difference between an input voltage signal and a feedback signal that gives information about the speed of the motor being driven. In the application above a PA01 is being used to drive a DC motor with an integral speed encoder that outputs a pulse train whose frequency is proportional to the angular velocity of the motor. This signal is then fed to a VFC, or Voltage to Frequency Converter, that is operated in the frequency to voltage mode. The output voltage of the VFC appears across Rf to create a current into the summing node of the amplifier. Likewise, Vcntl appears across Ri to create a current out of the summing node. When: Vo(VFC) = -Vcntl, then no current is fed to Cf, the integrating capacitor. If there is a difference between the current fed into the summing node by the Vfc and the current removed out of the node by the control voltage the difference current is fed to the integrating capacitor resulting in a change in output voltage which acts to correct the error.

Note that since the PA01 is driving a DC motor which can generate a continuous train of high frequency kickback pulses external flyback protection diodes, MUR110's were added from the output to the supplies in order to protect the PA01's output stage.

Unless dynamic braking is used, the -12V supply needs to support amplifier quiescent current only; a maximum of 50mA for the PA01.

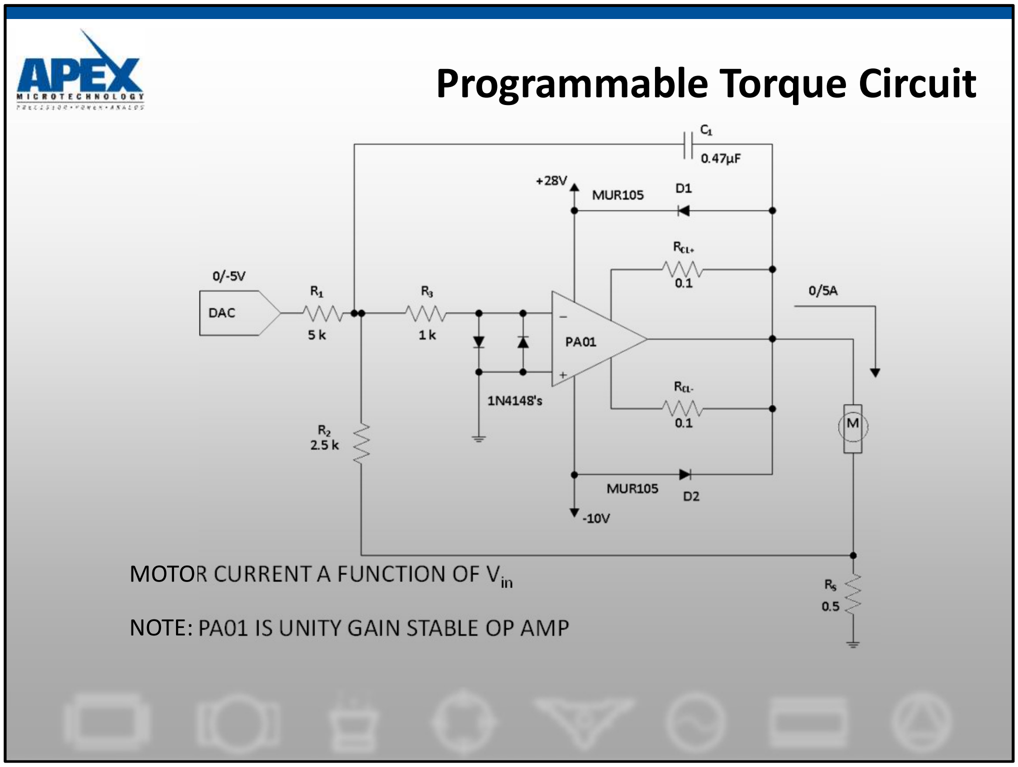


I_{in}	V_{in}	V_C	V_{RS}	I_O
4mA	-.996V	0	0	0
20mA	4.98V	3.984V	1.016V	5.08A

This circuit provides a Current-to-Current converter function through translation of a 4-20mA current transmitter to 0-5A output for linear control of a valve.

The 4-20mA is converted to a voltage through the use of a 249 ohm pull down resistor and buffered by A1. This voltage, VIN, is then offset to zero through the use of a precision voltage reference and a summing amplifier. Voltage VC then becomes the input command for the Voltage-to-Current conversion output stage using the PA12.

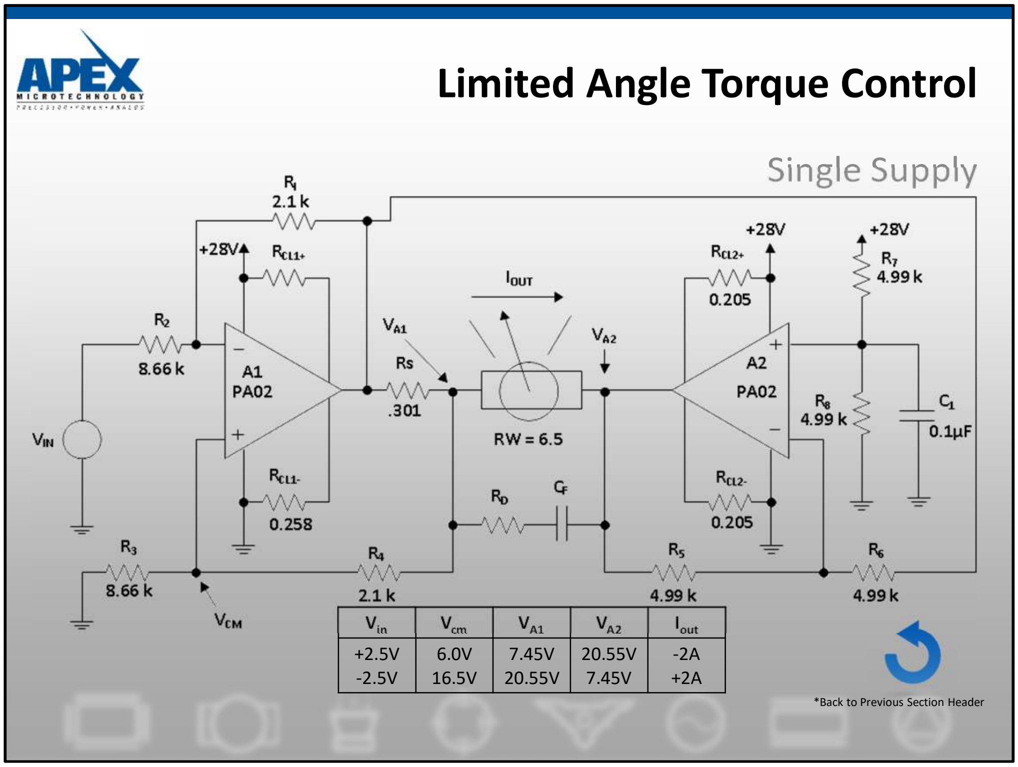
To guarantee AC small signal stability, stability analysis needs to be done using the load resistance and inductance of the actual linear valve to be used. These stability techniques we have covered previously. Be aware that valve inductance is likely a dynamic parameter changing with position of the valve.



This schematic uses several tricks that we've learned. First of all, notice that the PA01 is operating from non-symmetrical supplies. The –10 volt supply is merely to provide input common mode bias. The 28 volt supply is used to supply the load current.

In a motor, torque is directly proportional to current, so this is another form of voltage to current conversion. The inverting node of the PA01 is used as a summing node. Into the summing node flow two currents, one is the input voltage from the DAC across R1, the second is the feedback voltage (I load *Rs) across R2. These two currents are summed and the difference current is fed to C1 to be integrated. When the current through the motor is at the proper value the voltage across Rs will produce a current into the summing node that is equal to the current out of the summing node from the DAC. This results in no current flow to the integrating capacitor C1 resulting in a fixed output current.

Note that since the PA01 is driving a motor, high speed flyback diodes, MUR105s, are used to protect the amplifier's output stage against flyback voltage spikes. Also note that in integration type circuits the integration capacitor is connected directly from the output of the amplifier to the input. This means that high frequency pulses can be fed back directly to the input stage. Therefore we show 1N4148 input protection diodes and R3 in this application to prevent input stage damage to the PA01 caused by flyback coupling through C1



V_{in}	V_{cm}	V_{A1}	V_{A2}	I_{out}
+2.5V	6.0V	7.45V	20.55V	-2A
-2.5V	16.5V	20.55V	7.45V	+2A

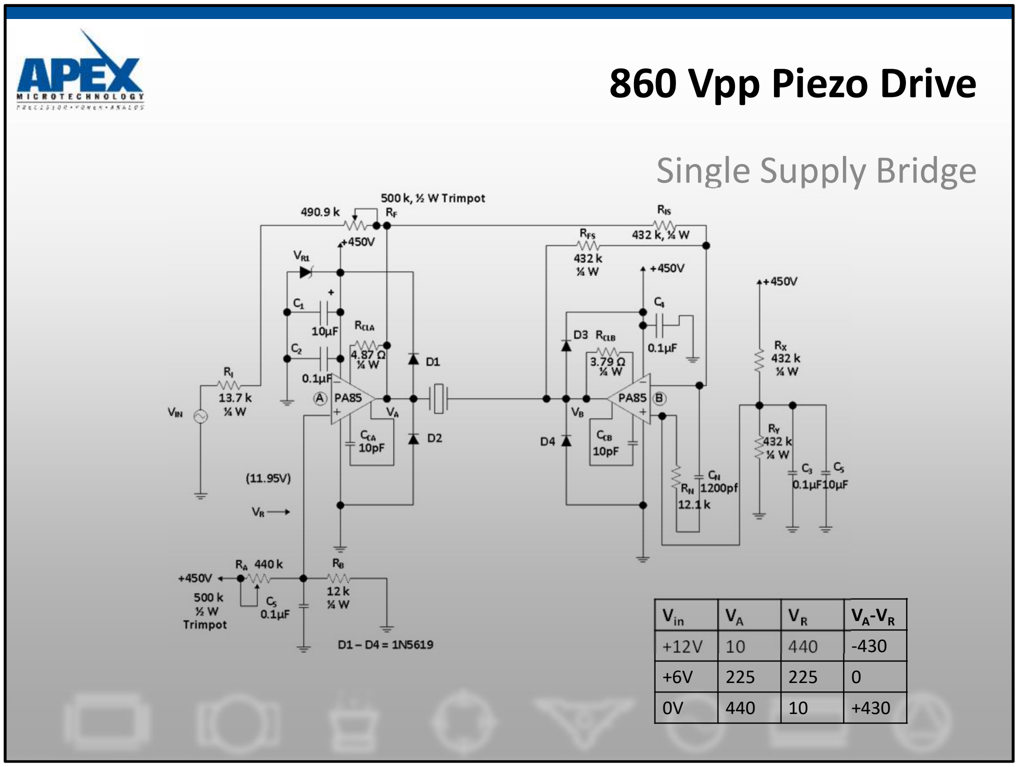
This real world application shows implementation of the generic case of V to I single supply. It combines bridge mode operation with the improved Howland current pump. The limited angle torquer will see bipolar current changes for bipolar input voltages.

Note that the Vs –6 common mode voltage range is met under both conditions of output voltage swing on A1. Also note that the peak output voltage swing is limited to less than Vs –(2 *Vcm) as was mentioned in the generic case for this configuration.

Although we are driving an inductive load we need no external flyback diodes since the PA02 has internal fast reverse recovery diodes. A full plus and minus 2 Amps is available for position control of the limited angle torquer despite the availability of only a single supply.

Ref. AN21

PIEZO DRIVE APPLICATIONS



V_{in}	V_A	V_R	V_A-V_R
+12V	10	440	-430
+6V	225	225	0
0V	440	10	+430

1. Vout = VA-VB

   Max Vout = Vs-V_{SATA} – V_{SATB}

2. Gain = $Vout_{p\text{-}p}$ /$Vin_{p\text{-}p}$ = $(VA\text{-}VB)_{p\text{-}p}$/$Vin_{p\text{-}p}$

   $860V_{p\text{-}p}/12V_{p\text{-}p}$ = 71.67

   Gain = 2 RF/RI since we have a bridge configuration. That is the voltage gain across the load is twice that of the primary amplifier, A, since +1V out of amplifier A yields -1V out of amplifier B, relative to the mid point power supply reference of +225V.

   Therefore RF/RI = 71.67/2 = 35.833

3. Offset:

   $$VA-VB = Vs\,(2(1+RF/RI)(\frac{RB}{RA+RB})-1) - 2\,(RF/RI)\,Vin$$

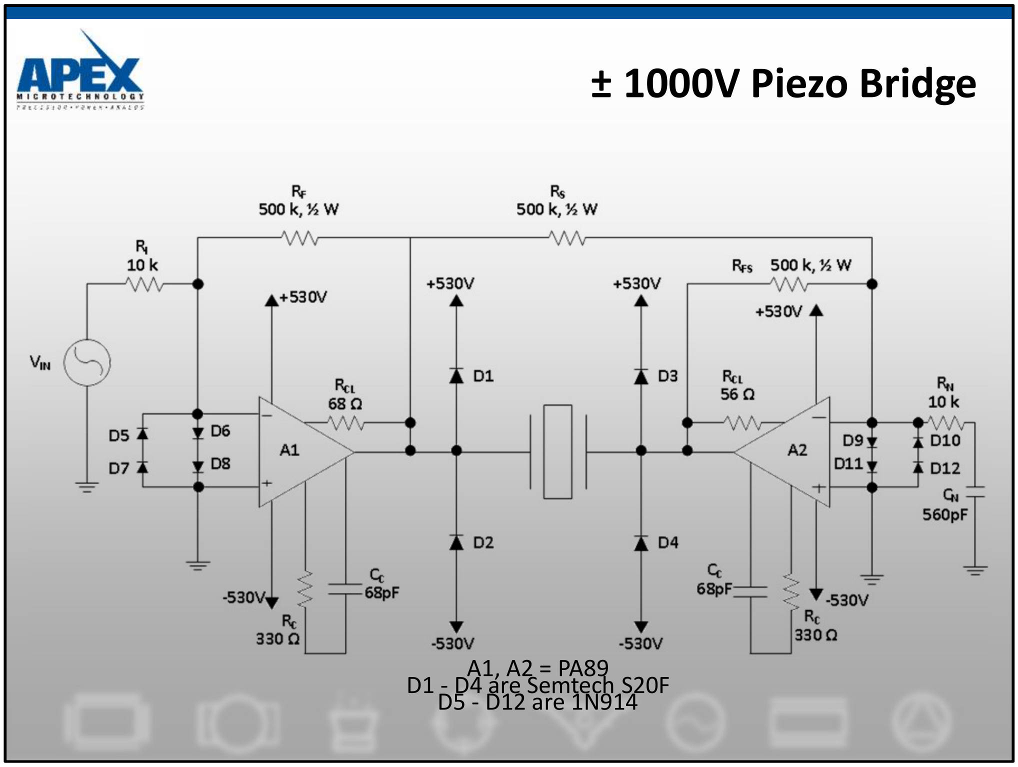
   When Vin= 0 then VA-VB = +430V

   Using RF/RI = 35.833 and solving above yields RA = 36.669RB

   Choosing RB = 12K implies RA = 440K

4. Check for commong mode voltage compliance: 11.95 V > 10V; OK.

Ref. AN25



Piezo users appear to never have enough voltage. As soon as it was introduced the PA89 found its way into bridge circuits to drive piezos at +/1100V and beyond.

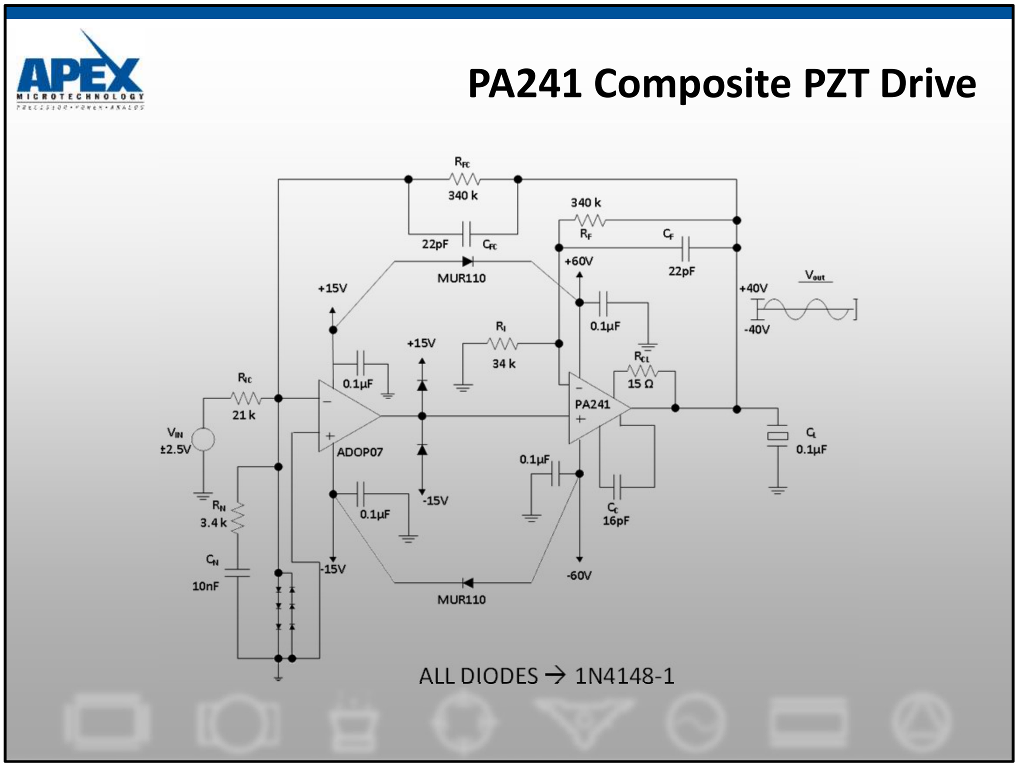
In this application we use the dual supply bridge configuration to deliver up to almost twice the supply voltage of 530V across the load. A1 operates in a gain of 50 to translate the +/–10Vinput to +/–500V out of A1. A2 then inverts this output to add an additional –/+500V across the Piezo to yield a net +/–1000V.

A2 uses noise gain compensation to allow its Vo/Vin transfer function to remain at –1, though its compensation capacitor Cc is set for a gain of 50. The noise gain will allow AC stability as well as a balanced bridge since both amplifiers are now compensated identically for the same slew rate.

Input protection diodes, output flyback diodes and proper component selection enhance reliability. Remember to select Cc capacitors with a voltage rating of at least 1100V, RI, RF, RIS, and RFS with proper power dissipation and voltage coefficient of resistance, and D1 - D4 with a PIV of at least 1100V.

As a final note remember to check the amplifiers for AC stability due to capacitive loading depending upon the capacitance of the piezo being driven.

Ref. AN25



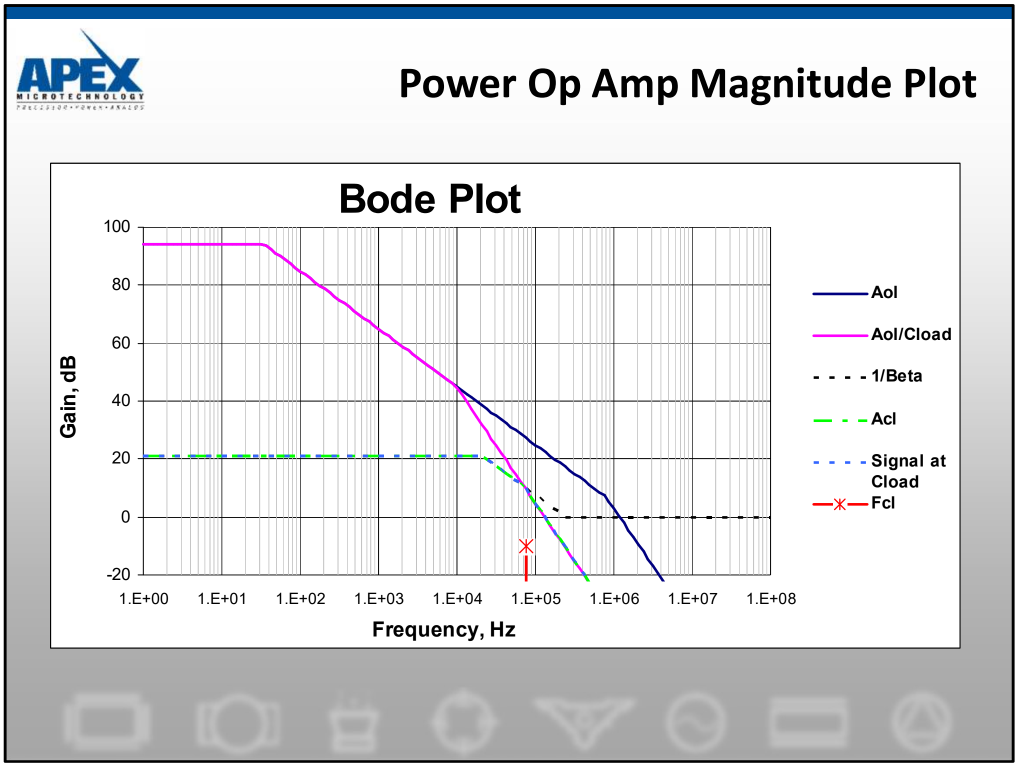
This circuit is included as an example in Power Design.xls. It is different from most power op amps in that current limit from positive side to negative side does not match well at all.

We will start by stabilizing the power stage, then the composite. Then we will examine current limit and frequency limitations imposed by this current limit.

1N4148 diodes on the input of the OP07 provide differential and common mode over voltage protection for transients through Cfc. Diodes on the output of the OP07 prevent over voltage transients that can occur through Cf,through the PA241 input protection diodes to the OP07 output through the PA241 internal input protection diodes.

Fast recovery diodes between pairs of supplies ensure that the PA241 input stage is protected from over voltage in the event the ±15V supplies are up before the high voltage supplies.

Ref. AN19,AN25



In any composite amplifier, make sure the power output stage is stable first. Any of the techniques we learned earlier can be used.

Ref. AN19, AN25

Composite Amplifier Set-up

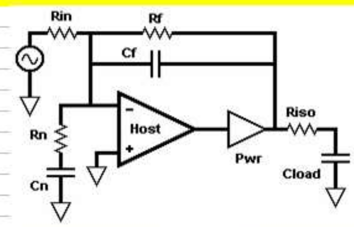
Composite Circuits

38 Goto Main Circuit

MODEL	OP07	READ ME				Estimated Closure Frequency =	56.23413	KHz
Aol =	135	dB	Pole 1 =	0.1	Hz	Suggested maximum bandwidth	5.623413	KHz
Pole 2 =	7.00E+05	Hz	Pole 3 =	7.00E+06	Hz	Estimated Closure Rate =	20.0	dB/decade
Rin	21	Kohms	Rn	3.4	Kohms	Estimated Phase Margin =	50.625	Degrees
Rf	340	Kohms	Cn	10	nF	Load Host Data		
Cf	22	pF	Using Look-Up data					
Notes:								

R-C Pole Calculator:			
3.4	Kohms	47	Kohms
5	KHz	10	nF
9.36206	nF	0.338627538	KHz

1/Beta (DC)	24.7	dB
Noise Gain	16.7	dB
Pole Noise Gain	4.681027677	KHz
Zero Noise Gain	0.68665214	KHz
Pole Cf/Rf	21.27739871	KHz
Zero Rf/Cf	2493.508487	KHz

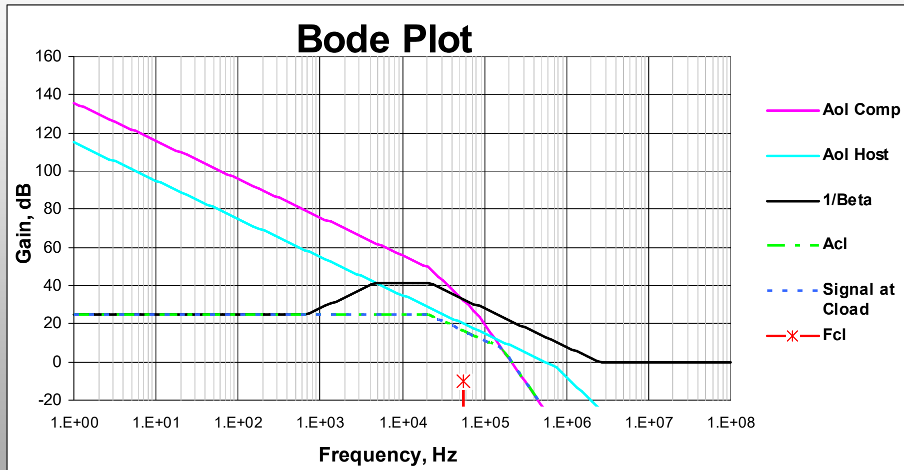


30 Print Data, Bode & Phase

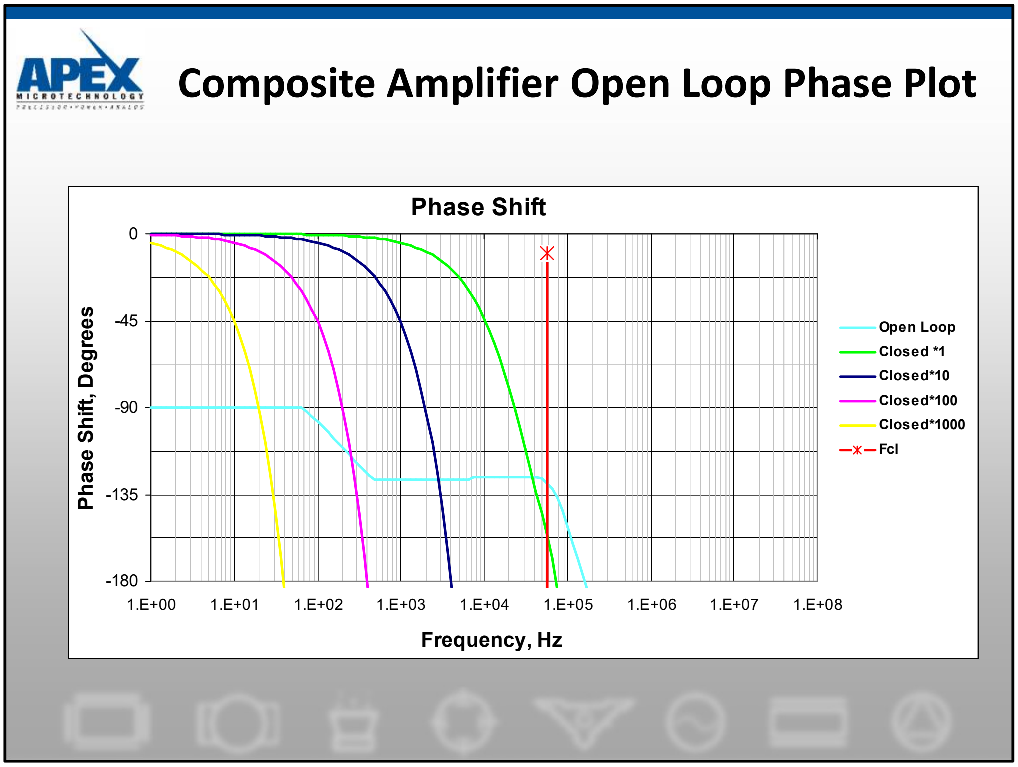
31 Print Data, Bode, Phase & Parts

Ref. AN19, AN25, AN38

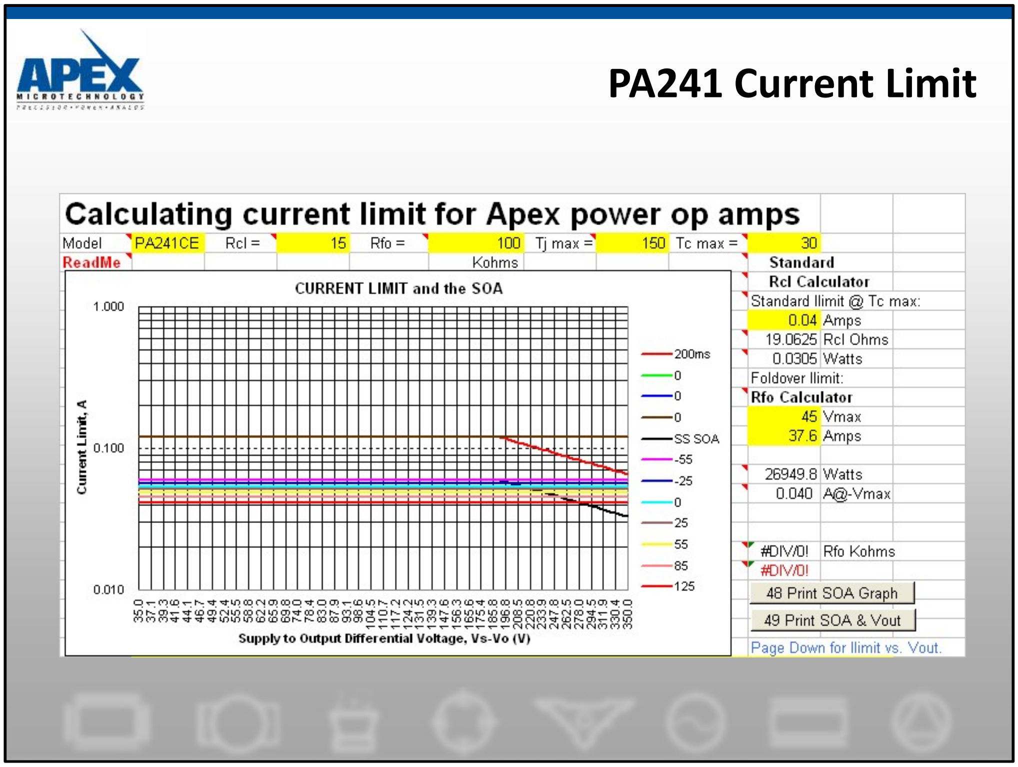
Composite Amplifier Magnitude Plot



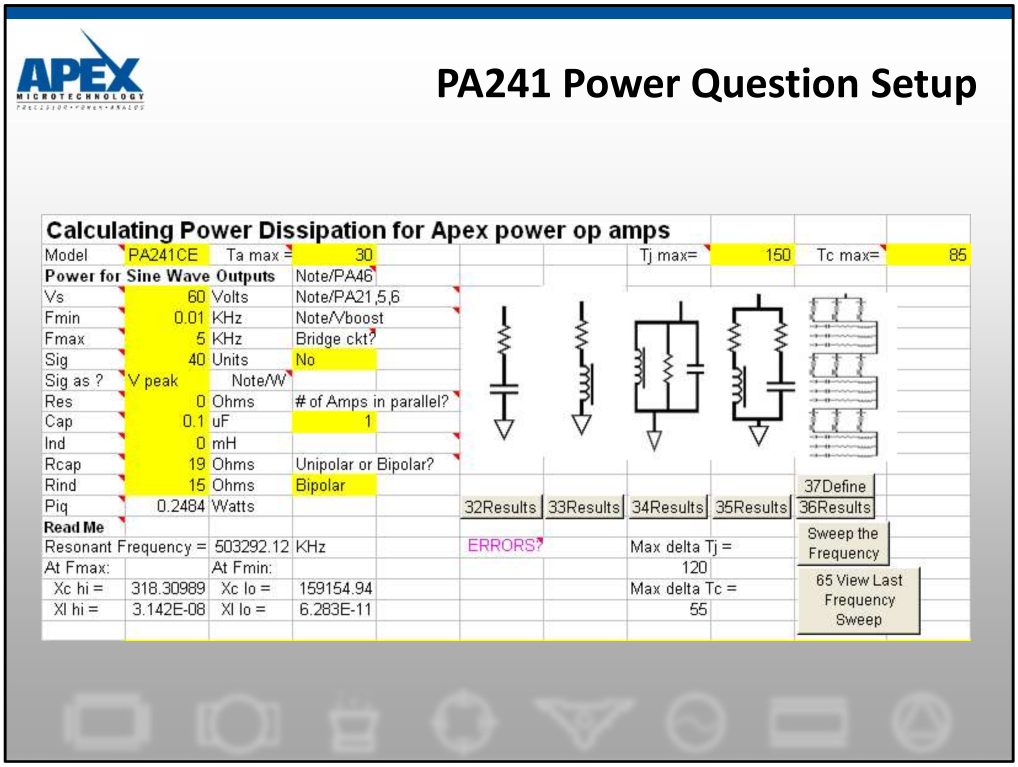
Ref. AN19, AN25, AN38



Ref. AN19, AN25, AN38



The amplifier selection, load and voltages have all been given. The only frequency that matters is the maximum (no current into a C load at DC). Our stability analysis suggested a maximum of about 10KHz (the Rf-Cf pole frequency).
Ref. AN37



The amplifier selection, load and voltages have all been given. The only frequency that matters is the maximum (no current into a C load at DC). Our stability analysis suggested a maximum of about 10KHz (the Rf-Cf pole frequency).

Ref. AN37

Speed is Limited by Iout

	At Fmin:	At Fmax:
Z in Ohms	159154.94	318.30989
Phase angle	-90.00	-90.00
RMS Amperes	0.0001777	0.0888577
Peak Amperes	0.0002513	0.1256637
RMS Volts	28.284271	28.284271
Peak Volts	40	40
RMS Power	0.0050265	2.5132741
Peak Power	0.0100531	5.0265482
Power factor	0.000	0.000
Input power	0.01	4.80
True power	0.00	0.00
Percent Efficiency =	1.95	49.78
Vpk capability =	51.65	40.23
Op amp internal dissipation:		
Input power	0.01	4.80
Dissipation RMS	0.0095998	4.80
Dissipation Peak	0.02	8.76
Total in heatsink	0.27	5.05
WC watts & Rth	5.048313	6.5
Readme		

38 Data Input

39 Print Results

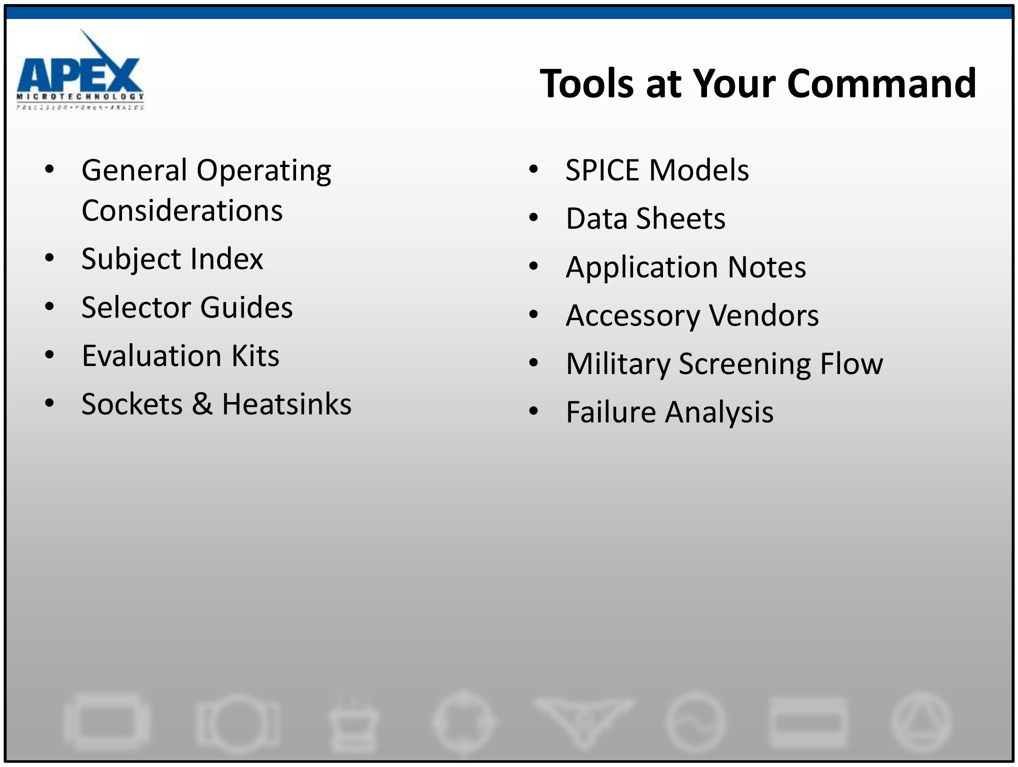
At Fmin:	At Fmax:			
Maximum AC Pint				
60	60	Vpk		
42.426407	42.426407	Vrms		
0.0002666	0.1332865	Arms		
0.0113097	5.6548668	Wrms		
7.108E-15	1.777E-09	Wtrue		
0.0143997	7.1998695	Pin		
Minimum HS:		9.89	°C/W	
Actual HS:		5.2	°C/W	
Results in Tjmax =		92.68	°C	
Results in Tcmax =		61.2995407	°C	
				1
				0
CURRENT TOO HIGH!				0
HS/Tcase	HS/Tj	Larger		1
9.8947286	16.55461	9.89472857		

*Back to Previous Section Header

255mA would be required to drive the .1µF load at 10Kz! Notice the “CURRENT TOO HIGH!” flag at the lower right. This is based on data sheet maximum, not the current limit resistor used. Since this is 10x our capability, 1KHz will be the limit with a 75Ω current limit resistor. When this is plugged in, we will find normal operation with no heatsink is possible. To analyze fault conditions, find the lowest impedance to be encountered, assume the current limit (47mA in this case) is driven into the load and calculate the output voltage. Subtract this from the supply voltage, compare to the SOA of the amplifier and calculate a larger heatsink as required.

Ref. AN37

CONCLUSION



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Unless you're an old hand at power design, check out AN1, General Operating Considerations. It is the most important document in the entire book. While there is no substitute for actually reading it, at a very minimum, take note of the paragraph titles and look at the pictures.

In the back of the book is a Subject Index which may just point you to the specific information you need. Here's a sample of entries: Package drawings and marking information (Where's pin 1?), Load lines, Feedback zero compensation and Thermal capacity. You can also find many phone numbers, fax numbers and if you are inclined to visit Apex, a map.

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- Value of 8 solder joints vs. 80?
  - Size, weight
  - Reliability
    - First pass yield, troubleshoot, rework, retest times
    - Field failure rate & serviceability
  - Logistics costs
    - Component spec, buying, stocking, managing obsolescence

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Apex Operational Amplifiers

Document	Date
AN23 Heat Sinking Options and Techniques(PDF, AN23UREVB: 1023 Kb)	10/2012
AN01 General Operating Considerations(PDF, AN01UREVJ: 995 Kb)	10/2012
AN02 Optoelectronic Position Control(PDF, AN02UREVD: 291 Kb)	10/2012
AN03 Bridge Circuit Drives(PDF, AN03UREVE: 354 Kb)	10/2012
AN05 Precision Magnetic Deflection(PDF, AN05UREVF: 369 Kb)	10/2012
AN06 Applying the Super Power PA03(PDF, AN06UREVD: 432 Kb)	10/2012
AN07 Programmable Power Supplies(PDF, AN07UREVE: 344 Kb)	10/2012
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AN16 SOA Advantages of MOSFETS(PDF, AN16UREVD: 287 Kb)	10/2012
AN17 Wideband Low Distortion Techniques(PDF, AN17UREVD: 287 Kb)	10/2012
AN19 Stability for Power Amplifiers(PDF, AN19UREVF: 535 Kb)	08/2013
AN20 Bridge Mode Operation of Power Amplifiers(PDF, AN20UREVF: 395 Kb)	10/2012
AN21 Single Supply Operation of Power Amplifiers(PDF, AN21UREVD: 480 Kb)	10/2012
AN22 SOA and Load Lines(PDF, AN22UREVF: 424 Kb)	10/2012
AN23 Heat Sinking Options and Techniques for Thermally Enhanced SMT Packages(PDF, AN23UREVB: 1023 Kb)	10/2012
AN24 Brush Type DC Motor Drive(PDF, AN24UREVD: 241 Kb)	10/2012
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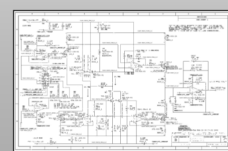

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Apex precision power products provide complex circuit designs in a single package, enabling high density designs with a reduced time to market
We serve markets that require a long term source of supply. This is reflected in the extensive lifetimes of our products and the lengthy tenure of our customer relationships.

So think of Apex Microtechnology the next time you are challenged with a power analog design project. Remember, Apex is not going to be just another supplier. Apex gives you access to leading edge analog solutions and technical support excellence that will prove to be instrumental to the success of your project. Contact us at sales@apexanalog.com to get started.